A Tribute to Jim Williams

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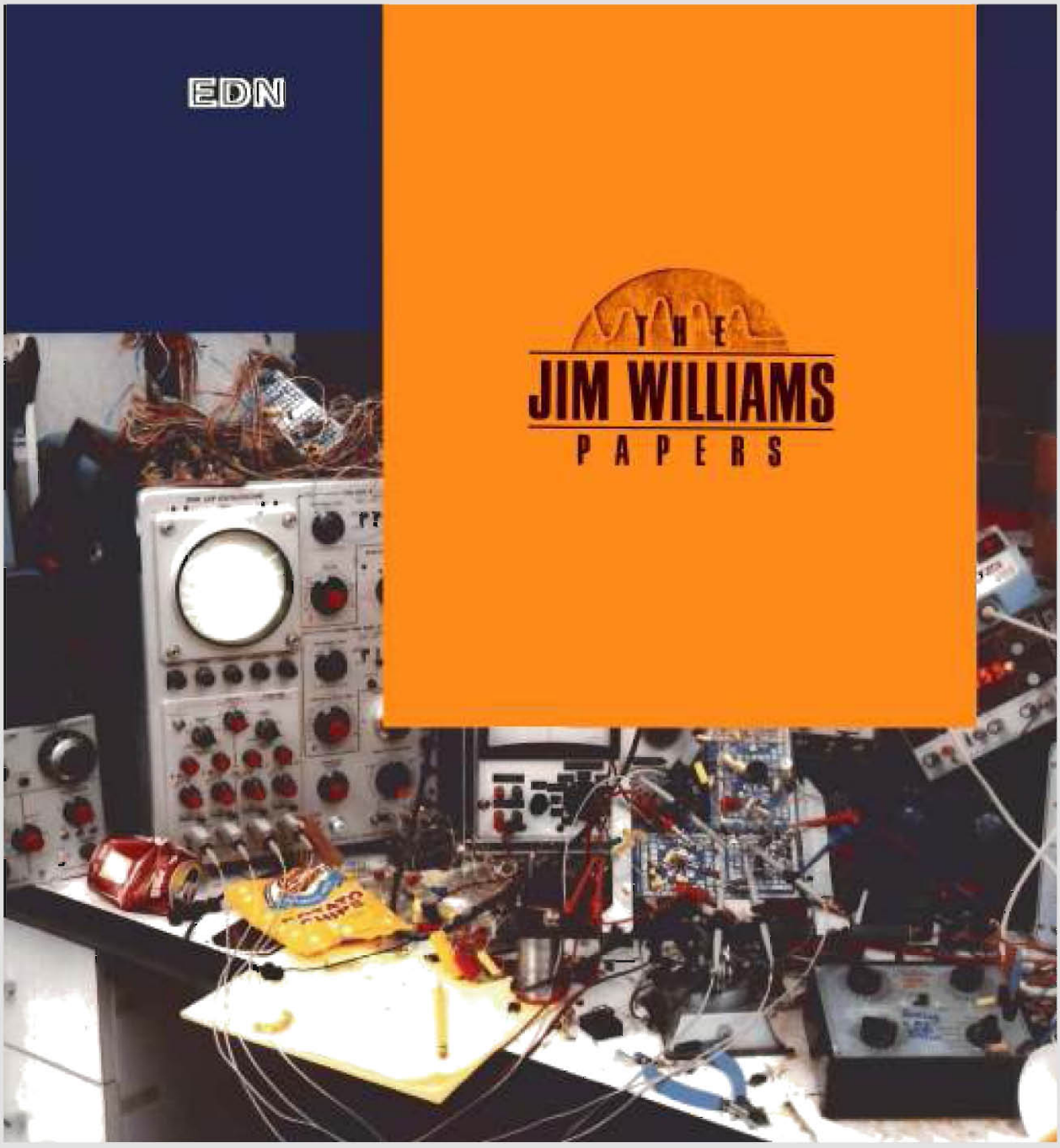


 By Jim Williams and Todd Owen, Linear Technology Corp

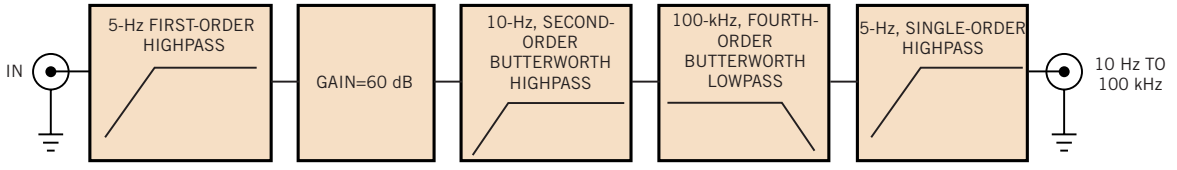
ALTHOUGH VERIFYING THAT A LOW-DROPOUT REGULATOR MEETS ITS DROPOUT SPECIFICATION IS STRAIGHTFORWARD, VERIFYING ITS NOISE PERFORMANCE PROVES MORE DIFFICULT. YOU HAVE TO PAY CAREFUL ATTENTION TO THE TEST SETUP, INCLUDING THE VOLTMETER YOU USE.

Exacting noise test ensures low-noise performance of low-dropout regulators

TELECOMMUNICATIONS, NETWORKING, audio, and instrumentation applications increasingly require low-noise power supplies. Low-noise, low-dropout linear regulators interest designers who work in these application areas. These components may exclusively power noise-sensitive circuitry, circuitry that contains only some noise-sensitive elements, or both. Additionally, to conserve power, particularly in battery-driven apparatus, such as cellular telephones, the regulators must operate with low input-to-output voltages. New devices meet the concurrent requirements for low noise, low dropout, and small quiescent current. For example, the LT1761 has noise of 20 μV_{RMS}, a dropout of 300 mV at 100 mA, and a quiescent current of 20 µA. Clearly, all designs have different low-noise and low-dropout needs. For some help in selecting the right device, see **sidebar** "Selecting a low-noise, low-dropout regulator." For some more background on low-dropout-regulator architecture, see **sidebar** "The architecture of a low-noise low-dropout regulator."

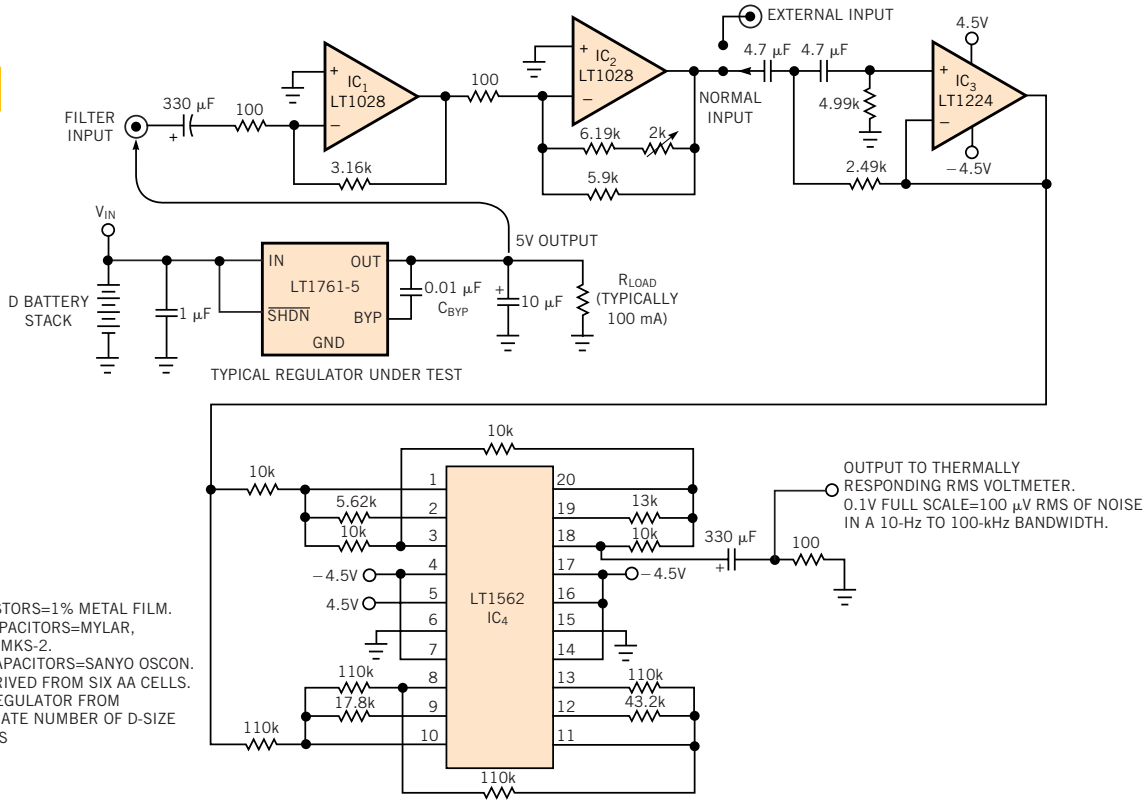
Testing such low-noise devices takes great care. Fortunately, establishing and specifying low-dropout performance is easy. Verifying that a regulator meets dropout specification is similarly straightforward. However, accomplishing the same missions for noise and noise testing involves more effort. The manufacturer or whoever is performing the testing must clearly call out the noise bandwidth of interest along with the operating conditions. Operating conditions can include regulator input and

Figure 1



In this filter structure for noise testing of low-dropout regulators, Butterworth-filter sections provide the steep slopes and flat passband in the desired frequency range of 10 Hz to 100 kHz.

Figure 2



NOTES:
ALL RESISTORS=1% METAL FILM.
4.7-µF CAPACITORS=MYLAR, WIMA MKS-2.
330-µF CAPACITORS=SANYO OSCON.
±4.5V DERIVED FROM SIX AA CELLS. POWER REGULATOR FROM APPROPRIATE NUMBER OF D-SIZE BATTERIES

Low-noise amplifiers IC_1 and IC_2 provide gain and initial highpass shaping. IC_4's filter IC implements a fourth-order-Butterworth lowpass characteristic.

output voltage, load, and the characteristics of assorted discrete components. Numerous subtleties can affect low-noise performance, and changes in operating conditions can cause unwelcome surprises. Thus, manufacturers must quote low-dropout- regulator noise performance under specified operating and bandwidth conditions for the specification to be meaningful. Misleading data and erroneous conclusions result when you fail to observe this precaution.

DETERMINE THE NOISE BANDWIDTH FOR TEST

Before testing, you have to determine the noise bandwidth of interest. For most systems, the range of 10 Hz to 100 kHz is the information-signal-processing area of concern. Additionally, linear regulators produce little noise energy outside this region. Switching regulators are a different proposition and require a broadband noise measurement (**Reference 1**). These considerations suggest a measurement bandpass of 10 Hz to 100 kHz with steep slopes at the bandlimits. **Figure 1**

continued on pg 152

SELECTING A LOW-NOISE, LOW-DROPOUT REGULATOR

Any design has requirements for a low-noise, low-dropout regulator, and you should carefully examine each situation for specific needs. However, some general guidelines apply in selecting a low-noise, low-dropout regulator. Consider the following significant issues:

Current capacity: Ensure that the regulator has adequate output-current capacity for the application, including worst-case transient loads.

Power dissipation: The device must be able to dissipate whatever power is necessary, which affects package choice. Usually, the $V_{IN}-V_{OUT}$ differential is low in low-dropout-regulator applications, obviating this issue. Prudence dictates checking to be sure.

Package size: Package size is important in limited-space applications. Current capacity and power-dissipation constraints dictate the package size.

Noise bandwidth: Ensure that the low-dropout regulator meets the system's noise requirement over the entire bandwidth of interest; 10 Hz to 100 kHz is realistic, because information usually occupies this range.

Input-noise rejection: Ensure that the regulator can reject input-related disturbances originating from clocks, switching regulators, and other power-bus users. If the regulator's power-supply rejection is poor, its low-noise characteristics are useless.

Load profile: Know the load characteristics. Steady-state drain is important, but you must also evaluate transient loads. The regulator must maintain stability and low-noise characteristics under all such transient loads.

Discrete components: The choice of discrete components, particularly capacitors, is important. The wrong capacitor dielectric can adversely affect stability, noise performance, or both.

ARCHITECTURE OF A LOW-NOISE, LOW-DROPOUT REGULATOR

Figure A shows a design scheme for a low-noise, low-dropout regulator that the LT176X through LT196X family of regulators uses. This scheme minimizes noise transmission within the loop and minimizes noise from an unregulated input. The bypass capacitor, C_{BYP}, filters the internal voltage reference's noise. Additionally, the scheme shapes the error amplifier's frequency response to minimize noise contribution while preserving transient response and power-supply rejection ratio. Regulators that do not shape this response have poor noise rejection and transient performance.

Achieving an extremely low dropout voltage requires careful design of the pass element. The pass element's on-impedance limits its set dropout limitations. The ideal pass element has zero impedance between the input and the output and consumes no drive energy.

A number of design and technology options offer various trade-offs and advantages. **Figure B** shows some pass-element candidates. Followers (**Figure Ba**) offer current gain, ease of loop compensation because the voltage gain is below unity, and drive current that ends up going to the load. Unfortunately, saturating a voltage follower requires overdriving the input, at the base or gate, for example. Generating the overdrive is difficult because the regulator usually derives the drive directly from V_{IN}. Practical circuits must either generate the overdrive or obtain it elsewhere. Without voltage overdrive, the V_{BE} sets the saturation loss in the bipolar case, and channel on-resistance sets the saturation loss for MOS. MOS-channel on-resistance varies under these conditions; you can more easily predict bipolar losses. Voltage losses in driver stages, such as Darlington stages, add directly to the dropout voltage. The follower output of conventional three-terminal IC regulators combines with drive-stage losses to set dropout at 3V.

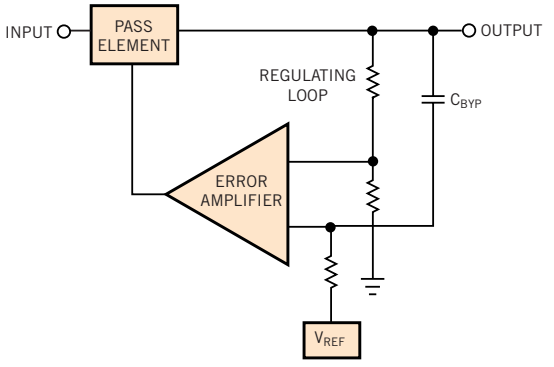
The common emitter/source is another pass-element option (**Figure Bb**). This configuration removes the V_{BE} loss in the bipolar case. The pnp version is easy to fully saturate, even in IC form. The trade-off is that the base current never arrives at the load, which wastes power. At higher currents, base drive losses can negate a common emitter's saturation advantage. As in the follower example, Darlington connections exacerbate the problem. Achieving low dropout in a monolithic pnp regulator requires a pnp structure that attains low dropout while minimizing base drive loss. This requirement becomes the case at higher pass currents. Designers of the LT176X through LT196X regulators expended considerable effort in this area.

Common-source-connected p-channel MOSFETs are also candidates (**Figure Bb**). They do not suffer the drive losses of bipolar devices but typically require volts of gate-channel bias to fully saturate. In low-voltage applications, this bias may require generating negative potentials. Additionally, p-channel devices have poorer saturation than equivalent-size n-channel devices.

The voltage gain of common-emitter and -source configurations is a loop-stability concern but is manageable.

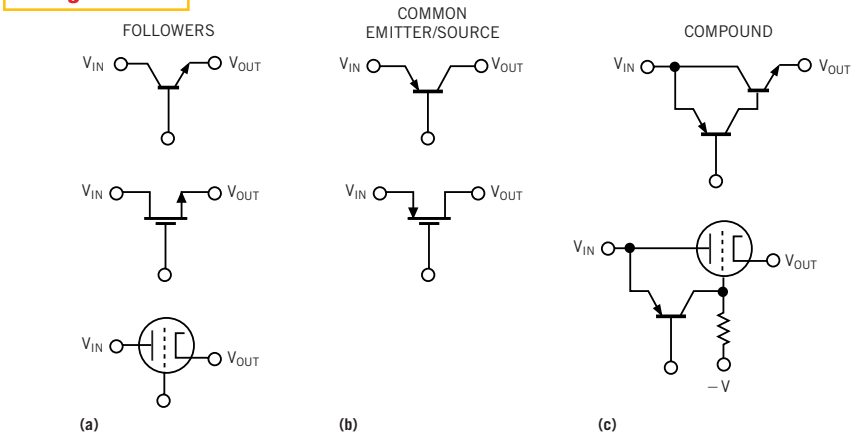
Compound connections using a pnp-driven npn (**Figure Bc**) are a reasonable compromise, particularly for high power—beyond 250 mA—IC construction. The trade-off between the pnp V_{CE} saturation term and reduced drive losses over a conventional pnp structure is favorable. Also, the major current flow is through a power npn, which is easy to realize in monolithic form. The connection has voltage gain, necessitating attention to loop-frequency compensation. Regulators that use this pass scheme, such as the LT1083 through LT1086, can supply as much as 7.5A with dropouts below 1.5V.

Figure A



A low-dropout-regulator design scheme minimizes noise within the loop and minimizes noise from an unregulated input.

Figure B



Pass-element candidates include followers (a), common-emitter/source types (b), and compound types (c).

shows a conceptual filter for low-dropout-regulator-noise testing. Steep slopes and flatness in the passband require the Butterworth-filter sections. The small input level requires 60 dB of low-noise gain to provide an adequate signal for the Butterworth filters.

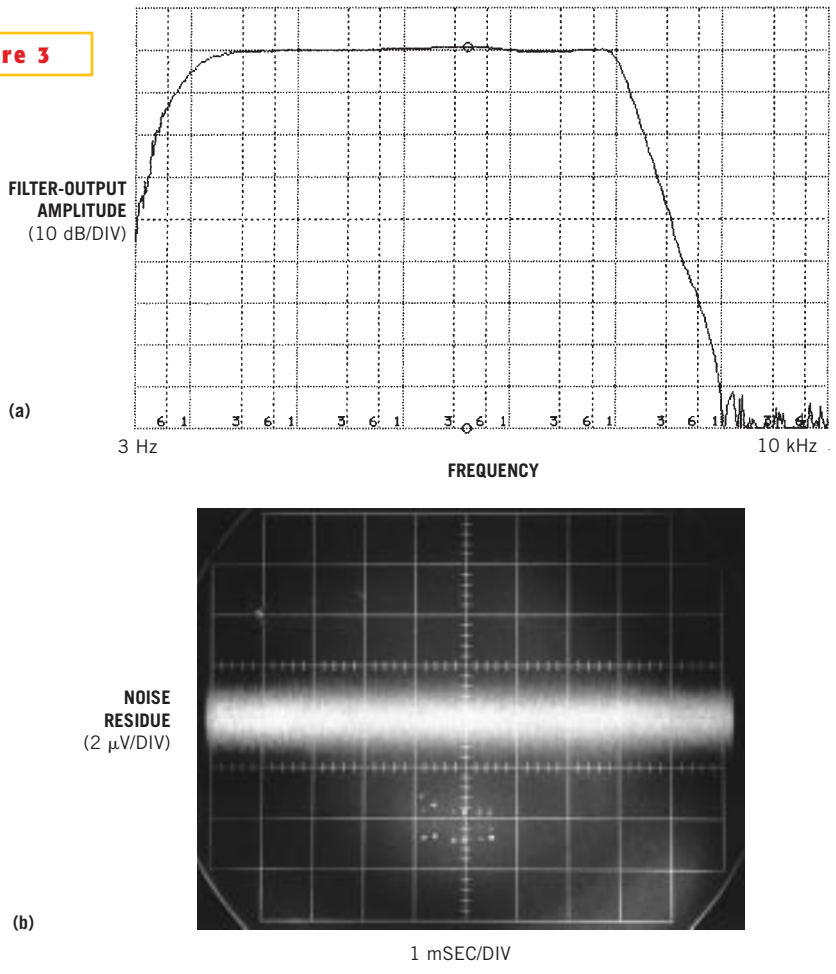
Figure 2 details the filter scheme for the LT1761-5 regulator under test. IC_1 to IC_3 make up a 60-dB-gain highpass section. IC_1 and IC_2, which are extremely low-noise amplifiers (<1 nV/$\sqrt{\text{Hz}}$), comprise a 60-dB gain stage with a 5-Hz highpass input. IC_3 provides a 10-Hz, second-order-Butterworth, highpass characteristic. The design configures IC_4's filter IC as a fourth-order-Butterworth, lowpass filter. The circuit delivers the output of this filter to the output via the 330-μF/100Ω highpass network. The circuit's output drives a thermally responding rms voltmeter. Obtaining meaningful measurements depends greatly on your choice of an rms voltmeter (see "Understanding and selecting rms voltmeters" on page 54.) Batteries furnish all power to the circuit, which precludes ground loops from corrupting the measurement.

VERIFY INSTRUMENTATION PERFORMANCE

Good measurement technique dictates verifying the noise test instrumentation's performance. **Figure 3a**'s spectral plot of the filter section shows an essentially flat response in the 10-Hz to 100-kHz passband with abrupt slopes at the band extremes. Some flatness deviation exists, but the response stays well within 1 dB throughout nearly the entire passband. Grounding the filter's input determines the tester's noise floor. **Figure 3b** shows noise of less than 4 μV p-p , corresponding to a 0.5-μV-rms voltmeter reading. This noise level is only about 0.5% of full scale, contributing negligible error. These results give you the confidence to proceed with regulator-noise measurement.

Regulator-noise measurement begins with attention to test-setup details. The extremely low signal levels require attention to shielding, cable management, layout, and component choice. **Figure 4** shows the bench arrangement; to obtain faithful noise measurements you need a completely shielded environment. The

Figure 3

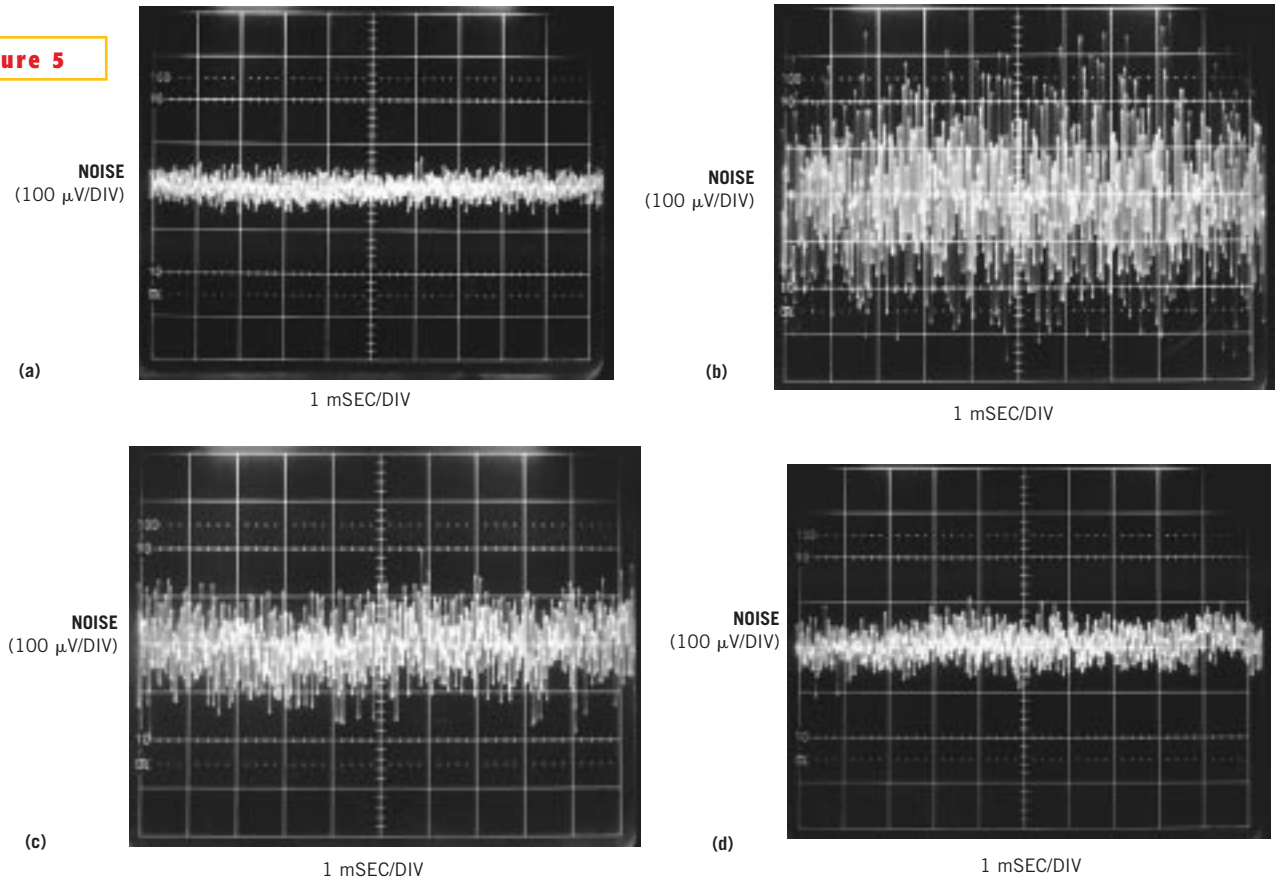


A spectrum analyzer plot (HP-4195A) of the test circuit's filter characteristics (a) verify a nearly flat response over the desired 10-Hz to 100-kHz frequency range with a steep roll-off outside the bandpass region. The test setup's noise residue of less than 4 mV p-p corresponds to approximately a 0.5 μV-rms measurement-noise floor (b).

Figure 4

A shielded can contains the regulator, and the noise filter circuitry occupies the small black box. The oscilloscope and rms voltmeter never connect to the test set simultaneously, precluding a ground loop from corrupting the measurement.

Figure 5



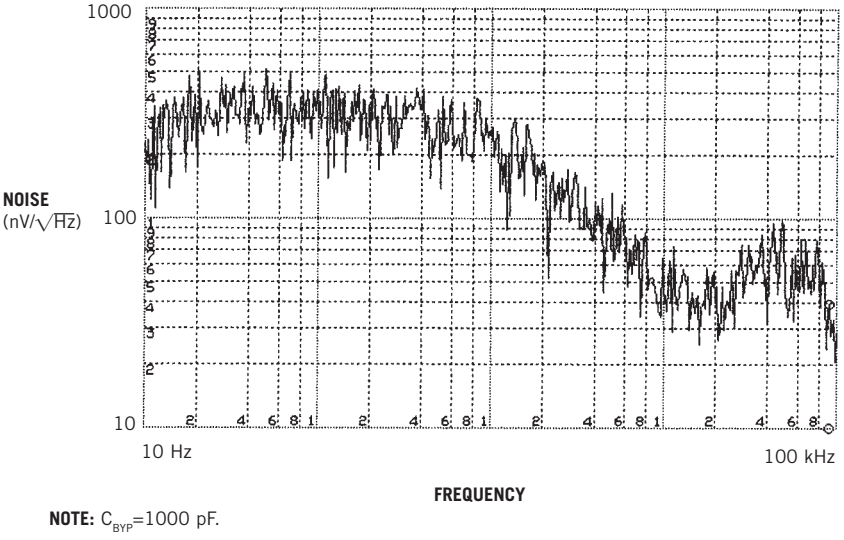
The regulator's output noise (a) corresponds to an rms voltmeter reader of 20 µV rms. Three other regulators (b, c, and d) are supposedly low-noise types, but the photos do not indicate low-noise performance. Ambiguity in test methods or specifications may cause the contradiction.

metal can encloses the regulator under test and an internal battery power supply. A BNC fitting connects the regulator's output to the noise-filter test circuit in the black box. This fitting eliminates triboelectric disturbances—extremely low-level disturbances that result when adjacent conductors move and charge "rubs" off—that a cable might contribute (**Reference 2**). The monitoring oscilloscope and voltmeter never connect to the output at the same time, precluding ground loops that would corrupt the measurement.

COMPARE NOISE RESULTS

Figure 5a shows an LT1761 regulator's noise measured at the filter output of **Figure 2**. Monitoring this point with the rms voltmeter shows a 20-µV-rms reading. **Figure 6**'s spectral plot of this noise indicates diminished power above 1 kHz in accordance with expected regulator noise density. This plot also verifies that

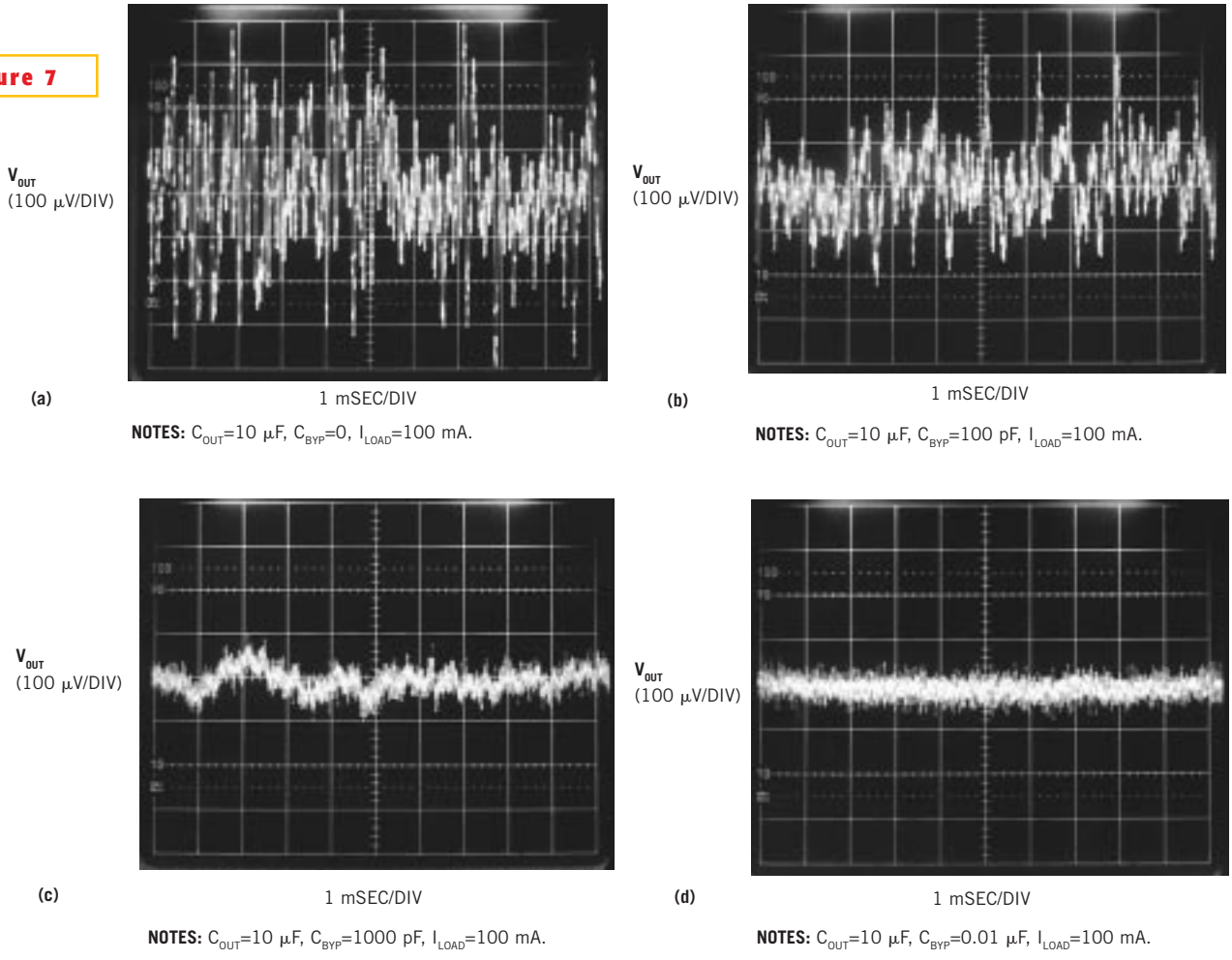
Figure 6



NOTE: C_{BYP}=1000 pF.

A spectral plot of Figure 2's output indicates diminished power above 1 kHz, which is in agreement with the expected regulator-noise density.

Figure 7



Bypass-capacitor values have a great impact on the measured noise level. Noise is very high when C_{BYP}=0 (a), nine times lower when C_{BYP}=0.01 µF (d), and at intermediate levels when equal to 100 and 1000 pF (b and c).

a 10-Hz to 100-kHz bandwidth is appropriate for the measurement.

Figure 5 also shows the output noise of three other regulators. The manufacturers specify these devices for low-noise performance, but the photos do not indicate low noise. Ambiguity in testing methods or specifications results in the seeming contradiction. For example, an inappropriate choice of test equipment or measurement bandwidth can easily cause as great as five times the errors. This uncertainty mandates noise testing to ensure realistic conclusions.

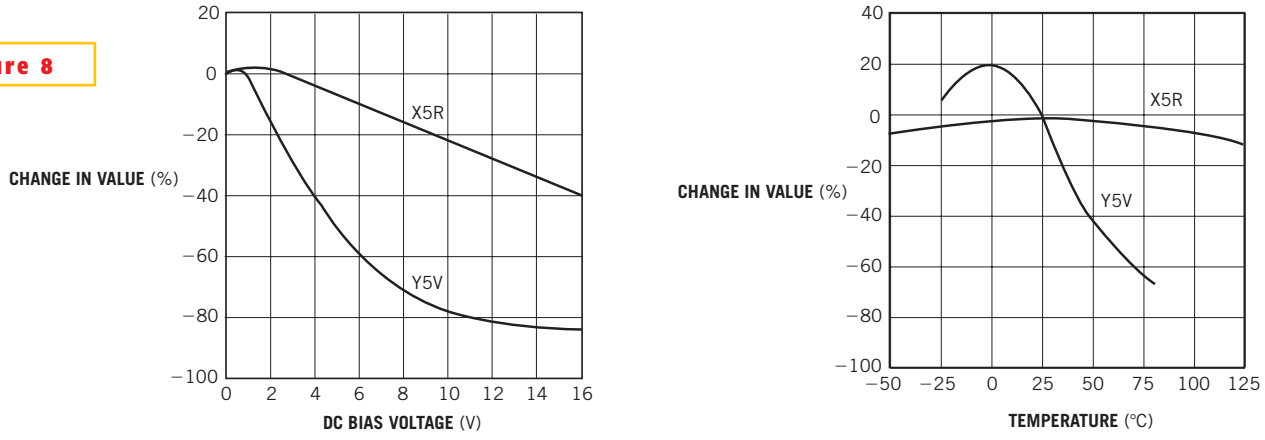
The noise that **Figure 5a** depicts results when the bypass capacitor, C_{BYP}, has a value of 0.01 µF. The regulator's internal voltage reference contributes most of the device's noise. The bypass capacitor filters reference noise by adding a low-frequency noise pole and precludes the noise from appearing in amplified form at the output. Thus, adding a capacitor from the regulators V_{OUT} to BYP pin lowers output noise. **Figure 7** shows regulator noise versus various values of C_{BYP}. **Figure 7a** shows substantial noise for C_{BYP}=0 µF, and **Figure 7d** displays nearly nine-times improvement with C_{BYP}=0.01 µF. Intermediate values of 100 and 1000 pF (**figures 7b** and **c**) produce commensurate results.

Your best choice for C_{BYP} is a good-quality low-leakage capacitor. Using a bypass capacitor also improves transient response. With no bypassing and a 10-µF output capacitor, a 10- to 500-mA load step settles to within 1% of final value in less than 100 µsec. With a 0.01-µF bypass capacitor, the output settles to within 1% for the same load step in less than 10 µsec, and total output deviation is within 2.5%. Regulator start-up time is inversely proportional to bypass-capacitor size, slowing to 15 msec with a 0.01-µF bypass capacitor and 10-µF capacitance at the output. Also, prudent selection of C_{BYP} reduces transient peak-to-peak amplitude by more than a factor of five.

CHOOSE CAPACITORS WITH CARE

The regulator in **Figure 2** is stable with a range of output capacitors. Output-capacitor ESR affects stability, most notably with small capacitors. A minimum output value of 3.3 µF with an ESR of 3Ω or less prevents oscillation. Transient response is a function of output capacitance. Larger values of output capacitance decrease peak deviations, providing improved transient response for large-load current changes. Bypass capacitors, which you use to decouple individual components powered by the regulator, increase the effective output-capacitor

Figure 8



NOTE:
BOTH CAPACITORS ARE 16V, 1210 CASE SIZE, 10 µF.

(a) (b)

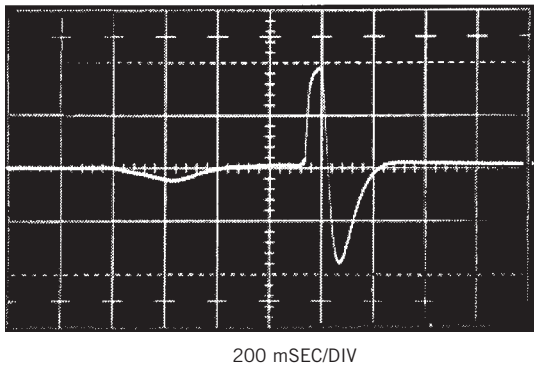
Ceramic capacitors exhibit strong voltage (a) and temperature (b) coefficients.

value. Larger values of bypass capacitance dictate larger output capacitors. For a 100-pF bypass capacitor, the recommended output-capacitor value is 4.7 µF. With 1000 pF of bypass capacitor or larger, a 6.8-µF output capacitor is necessary.

Ceramic capacitors require extra consideration. Manufacturers use a variety of dielectrics, each with different behavior across temperature and applied voltage to construct these capacitors. The most common dielectrics are Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics provide high capacitance in a small package but exhibit strong voltage and temperature coefficients (**Figure 8**). With a 5V regulator, a 10-µF Y5V capacitor shows values as low as 1 to 2 µF over the operating-temperature range. The X5R and X7R dielectrics have more stable characteristics and better suit output-capacitor use. The X7R type has better stability over temperature; the X5R costs less and comes in higher values.

Voltage and temperature coefficients are only two sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor, vibrations in the system or thermal transients can induce the stress. The resulting voltages can cause appreciable amounts of noise, especially when you use a ceramic capacitor for noise bypassing. A ceramic capacitor produced the trace that **Figure 9** depicts is a response to light tapping of a pencil. Similar vibration-induced behavior can masquerade as increased output-voltage noise.□

Figure 9



The vibration that results from simply tapping a ceramic capacitor with a pencil can cause appreciative amounts of noise.

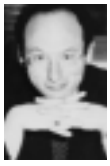
References

1. Williams, J, "A monolithic switching regulator with 100 µV output noise," Linear Technology Corp, Application Note 70, October 1997.

2. *Low-level Measurements*, Keithley Instruments, Cleveland, OH.

3. Williams, Jim, and Todd Owen, "Performance verification of low noise, low dropout regulators," Application Note 83.

Authors' biographies



Jim Williams, a staff scientist at Linear Technology Corp (Milpitas, CA, www.lineartech.com), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

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how it works

FAILING TO VERIFY AC-VOLTMETER ACCURACY BEFORE CONDUCTING RMS-NOISE MEASUREMENTS MAY CAUSE HIGHLY MISLEADING RESULTS.

Understanding and selecting rms voltmeters

Jim Williams and Todd Owen, Linear Technology Corp

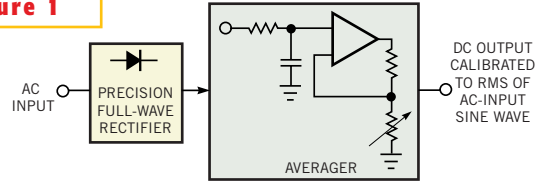
CHOOSING THE RIGHT ac voltmeter is crucial for meaningful noise measurements of low-noise, low-dropout regulators (see "Exacting noise test ensures low-noise performance of low-dropout regulators" on pg 149 in this issue). The ac voltmeter not only must have adequate bandwidth, but also must faithfully respond to the rms value of the measured noise. Similarly, the voltmeter must have the crest-factor capability to capture the noise signal's dynamic range. Crest factor is the ratio of the peak-to-rms value of the input signal. Unfortunately, most ac voltmeters, including digital voltmeters with ac ranges and instruments with "true- rms" ac scales, cannot be accurate under these measurement conditions. Thus, selecting an appropriate instrument requires care. The selection process begins with a basic understanding of ac-voltmeter types.

The basic ac-voltmeter types are rectify-and-average, analog-computing, and thermal. The thermal approach is the only one that is inherently accurate for all input waveshapes. This feature is relevant to determining the amplitude of rms noise. A fourth method for measuring the rms value of an input waveform—one that is uncommon for making noise measurements and therefore not part of this discussion—uses sampling techniques. This sampling technique involves taking a large number of samples of the input waveform and computing the rms value using digital techniques. Achievable accuracy for any given bandwidth varies with sampling rate and computational capability.

The rectify-and-average scheme applies the ac input to a precision rectifier (**Figure 1**). The rectifier output feeds a simple gain-scaled RC-averaging circuit to provide the output. In practice, you set the gain so that the dc output equals the rms value of a sine-wave input. If the input remains a pure sine wave, accuracy can be good. However, nonsinusoidal inputs cause large errors. This type of voltmeter is accurate only for sine-wave inputs with errors increasing as the input departs from sinusoidal.

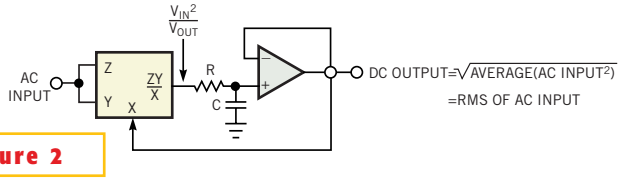
Figure 2 shows a more sophisticated ac-voltmeter method. In this case, an analog computational loop (ideally) continuously computes the instantaneous value. The dc output follows the equation in the **figure**, resulting in much better accuracy than the rectify-and-average method when the input waveshape varies. Almost all commercial implementations of this approach use logarithmically based analog-computing techniques. Unfortunately, dynamic lim-

Figure 1



A rectify-and-average-based ac/dc converter works well only for sinusoidal inputs.

Figure 2

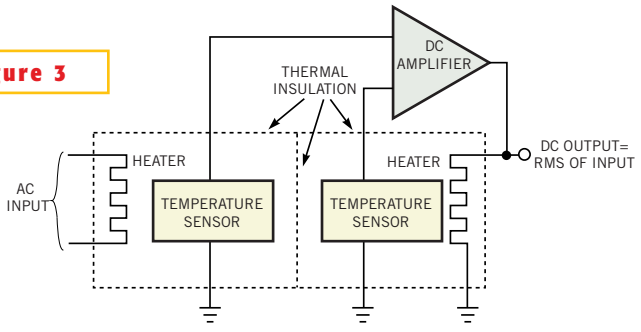


In an analog-computer-based, usually logarithmic, ac/dc converter, the loop continuously computes the input's rms value.

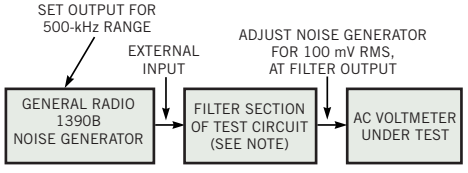
itations in the ZY/X block dictate bandwidth restrictions. These circuits typically develop significant errors beyond 20 to 200 kHz.

The thermally based ac voltmeter is inherently insensitive to input waveshape, making it suitable for measuring the amplitude of rms noise. Additionally, thermally based meters can achieve high accuracy at bandwidths exceeding 100 MHz. **Figure 3** shows the classic thermal scheme. (See **references 1** and **2** for more background on thermal ac-to-dc conversion.) This thermal converter comprises matched heater-temperature sensor pairs and an amplifier. The ac input drives a heater, warming it. The temperature sensor associated with this heater responds by biasing the amplifier. The amplifier closes its feedback loop by driving the output heater to warm its associated temperature sensor. When the loop closes, the heaters are at the same temperature. As a result of this "force-balance" action, the dc output equals the input heater's rms heating value, which is the fundamental definition of rms. Changes in waveshape have no effect because the scheme effectively downconverts any waveshape into heat. This "first-principles" nature of operation makes thermally based ac voltmeters ideal for quantitative rms-noise measurement. (The fundamental definition of an rms value is "the equivalent heating in a load.")

Figure 3



A thermally based ac/dc converter, which has extraordinarily low error, converts the ac input to heat and determines the dc output value necessary to produce identical heating.



NOTE: FOR FILTER SCHEMATIC, SEE **FIGURE 2** OF "EXACTING NOISE TEST ENSURES LOW-NOISE PERFORMANCE OF LOW-DROPOUT REGULATORS" ON PG 150 IN THIS ISSUE.

Figure 4

The setup for evaluating ac voltmeters includes a noise generator and a filter.

NOISE-DRIVEN AC VOLTMETERS

The wide performance variation of these three conversion methods, even within a method, mandates caution in selecting an ac voltmeter. Comparing ac voltmeters intended for use in rms-noise measurements is illuminating. **Figure 4** shows a simple evaluation arrangement. The noise generator drives a filter circuit, which produces a suitably bandpass-filtered input at the voltmeter under test. (You can find a schematic for the filter circuit in "Exacting noise test ensures low-noise performance of low-dropout regulators," pg 150.) In this application, you attach the noise generator, instead of a regulator under test, to the filter input. (For more information on noise generators, see **references 3** and **4**.)

Table 1 shows noise-test results for 20 voltmeters. Four of the voltmeters are thermal types; the remainder use logarithmic analog computing or rectify-and-average ac-to-dc conversion. The four thermal types agreed well within 1%. Three of the thermal types were within 0.2%. The fourth (the HP3400A), a metered instrument, is readable only to 1%. The other 16 voltmeters showed maximum errors of 48% relative to the thermal group. The errors cause lower readings than are warranted. In other words, a poorly chosen voltmeter gives unfairly optimistic readings.

The lesson here is clear: It is essential to verify ac-voltmeter accuracy before proceeding with rms-noise measurements. Failure to do so may cause highly misleading results.

BUILD A THERMAL-VOLTMETER CIRCUIT

You may want to construct, rather than purchase, a thermal voltmeter. **Figure 5**'s circuit is applicable to noise measurement. As in **Figure 4**'s block diagram, the input to this circuit also comes from the previously mentioned filter circuit in "Exacting noise test ensures low-noise performance of low-dropout

TABLE 1—VOLTMETER COMPARISONS

Voltmeter	Reading (mV)	Error (%)	AC/DC-conversion method
HP3403C	100	0	Thermal
HP3400A	100	0	Thermal
Fluke 8920A	100	0	Thermal
Figure 5's circuit	100	0	Thermal
Bench DVM	84	-16	Log
Bench DVM	85	-15	Rectify-average
Bench DVM	84	-16	Rectify-average
Fluke 8800A	90	-10	Rectify-average
HP3455	100	0	Log
HP334	92	-8	Rectify-average
Handheld DVM	52	-48	Rectify-average
HP3478	100	0	Log
Inexpensive handheld DVM	56	-44	Rectify-average
HP403B	93	-7	Rectify-average
HP3468B	93	-7	Log
Bench DVM	80	-20	Rectify-average
Bench DVM	72	-28	Rectify-average
Bench DVM	62	-38	Rectify-average
Fluke 87	95	-5	Log
HP34401A	93	-7	Log

regulators," pg 150. IC_1's output biases IC_2, which provides additional ac gain. The LT1088-based rms/dc converter comprises matched pairs of heaters and diodes and a control amplifier. IC_2 drives R_1, producing heat, which lowers D_1's voltage. Differentially connected IC_3 responds by driving R_2 via Q_3 to heat D_2, closing a loop around the amplifier. Because the diodes and heater resistors match, IC_3's dc output is related to the rms value of the input regardless of input frequency or waveshape. In practice, residual LT1088 mismatches necessitate a gain trim, which you can implement using IC_4. IC_4's output is the circuit output.

Start-up or input overdrive can cause IC_2 to deliver excessive current to the LT1088 with resultant damage. Comparators IC_{5A} and IC_{5B} prevent this damage. Overdrive forces D_1's voltage to an abnormally low potential. IC_{5A} triggers low under these conditions, pulling IC_{5B}'s negative input low. This action causes IC_{5B}'s output to go high, which puts IC_2 into shutdown and terminates the overload. After a time that the RC network at IC_{5B}'s input determines, the circuit enables IC_2. If the overload condition still exists, the loop almost immediately again shuts down IC_2 . This oscillatory action continues, protecting the LT1088 until the removal of the overload condition.

To trim this circuit, connect the input to a 10-mV rms, 100-kHz signal. Set the 500Ω zero-trim potentiometer for a dc output of exactly 100 mV. Next, apply a 100-kHz, 100-mV rms input and adjust the 10-kΩ full-scale-trim potentiometer for a dc output of 1V. Repeat this sequence until the adjustments do not interact. Two passes should be sufficient.□

References

1. "1968 Instrumentation. Electronic—Analytical—Medical," AC voltage Measurement, Hewlett-Packard Co, pg 197.
2. Williams, Jim, "A monolithic IC for 100-MHz rms/DC conversion," Application Note 22, Linear Technology Corp, September 1987.
3. Williams, Jim, "Practical circuitry for measurement and control problems;" "Broadband random noise generator;" "Symmetrical white Gaussian noise;" Appendix B, Application Note 61, Linear Technology Corp, August 1994, pg 24 and 38.
4. General Radio Co, Type 1390B, Random-noise-generator operating instructions, October 1961.

Authors' biographies

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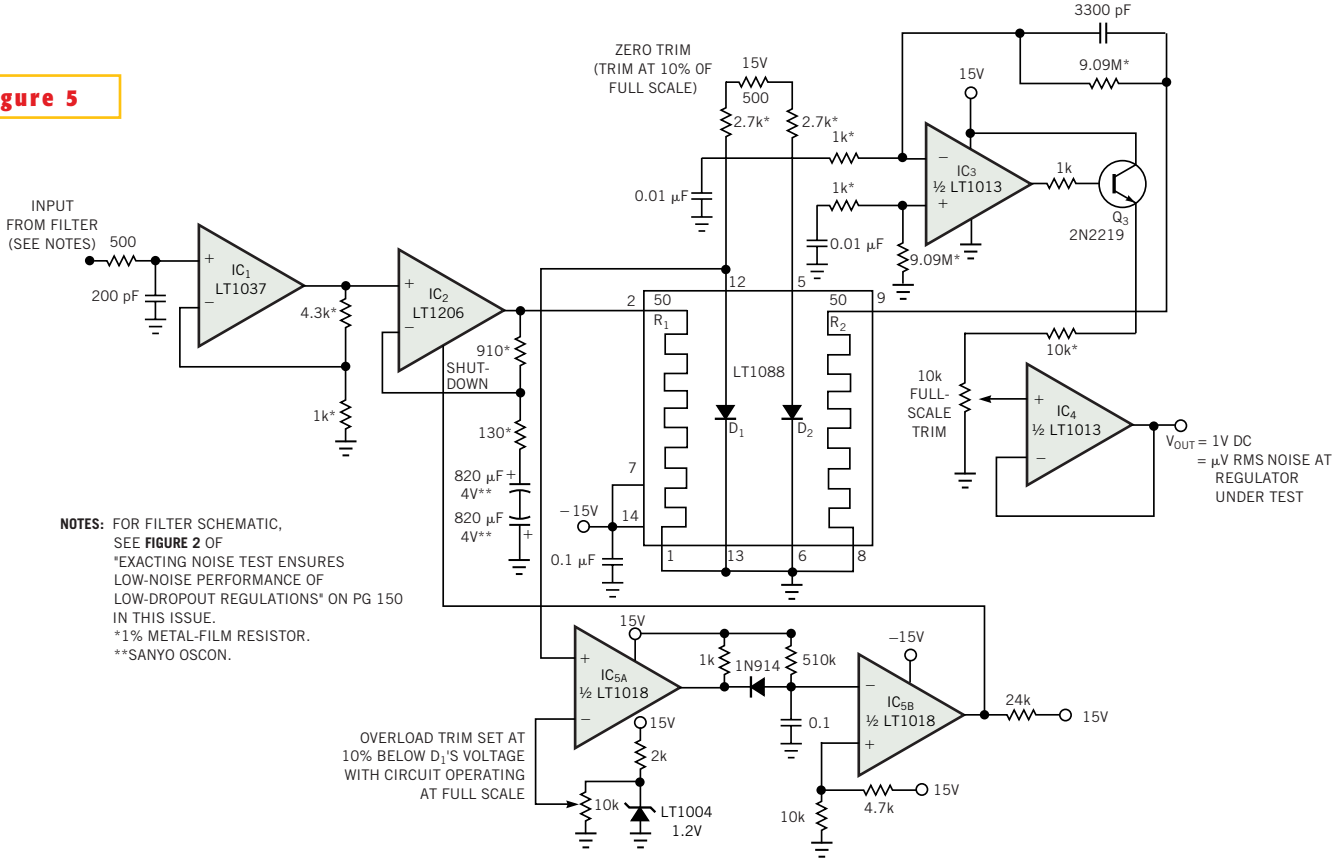
Todd Owen is a design engineer at Linear Technology, where he has worked for six years. He designs low-dropout linear regulators and has a BSEE from California Polytechnic State University (San Luis Obispo, CA). He enjoys skydiving with his wife.

Figure 5



This inexpensive thermally based rms voltmeter circuit is suitable for low-dropout-regulator noise measurements.

design ideas

Edited by Bill Travis and Anne Watson Swager

Filter design uses image parameters

Richard Kurzrok, RMK Consultants, Queens Village, NY

Reference 1 gives low-cost image-parameter design techniques for LC lowpass filters. Filter design using a low number of circuit elements results in reduced costs for both parts procurement and manufacturing. The technique applies to highpass filters. You derive a composite highpass filter by using m-derived terminating half-sections with one or more constant-k interior full sections. Classic image-parameter design used m-derived half-sections with m=0.6 for best passband impedance matching (in other words, high input and output return losses). The design uses a value of m=0.5 for the terminating half-sections. This value provides sharper close-in selectivity while maintaining passband return losses that are satisfactory for most applications. **Figure 1** shows the normalized schematic for the composite highpass filter. It uses midseries, m-derived, terminating half-sections with m=0.5, plus two interior constant-k full sections. The 3-dB cutoff frequency, f_0, is 31.2 MHz, and source and load impedances, Z_0, are 50Ω. Reference levels of filter inductance

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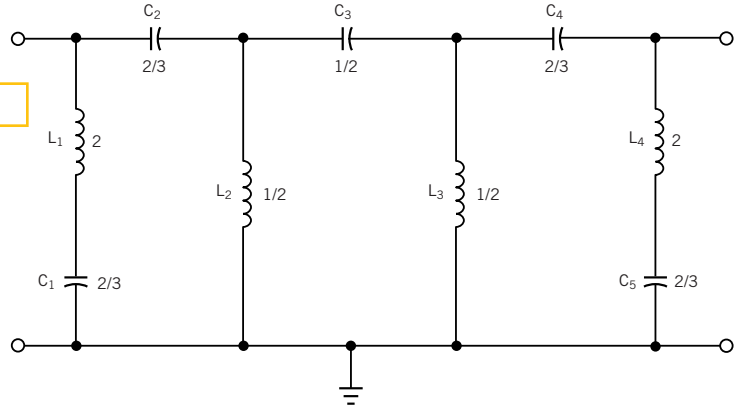
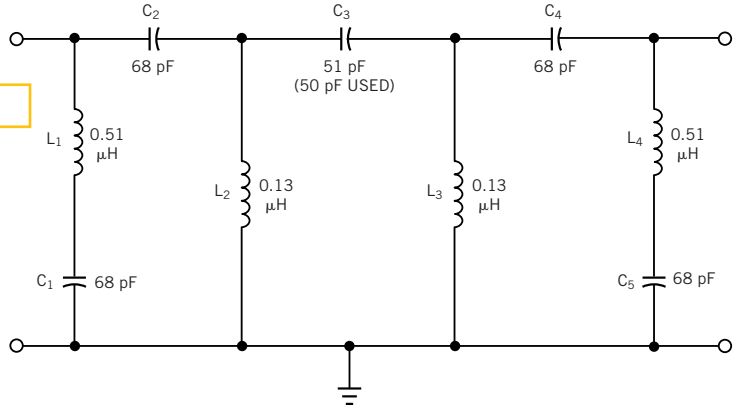
Figure 1



Using image parameters results in a low number of circuit elements in a filter.

Figure 2



Multiplying the normalized filter in Figure 1 by the reference inductance and capacitance values yields this 31.2-MHz, 50V filter.

TABLE 1–FILTER PARTS LIST

Function	Value	Type	Quantity
L_1, L_4	0.51 µH	Micro-Metals T 25-10 14T- #26	Two
L_2, L_3	0.13 µH	Micro-Metals T 25-10 14T- #26	Two
C_1, C_2, C_4, C_5	68 pF	CD-15 Series dipped mica	Four
C_3	50 pF	DC-15 Series dipped mica	One
Connectors	BNC female	Pomona 2447 panel receptacle	Two
Enclosure	Aluminum box	Hammond 1590A/Bud CU-123	One
Board	Cut by hand	Vector board 169P44C1	One
Standoffs	Male/female	Amatom 9794-SS-0440	Four

Note: all fixed capacitors have ±15% tolerance.

and capacitance are as follows:

$$L_0 = \frac{Z_0}{2\pi f_0} = 0.255\ \mu H;$$

$$C_0 = \frac{10^6}{2\pi f_0 Z_0} = 102\ pF.$$

You obtain the actual inductance and capacitance values for the highpass filter by denormalization; in other words, by multiplying the normalized inductances and capacitances in **Figure 1** by L_0 and C_0, respectively. **Figure 2** shows the actual component values for a dissipationless highpass filter. **Table 1** gives the parts list for the filter. **Table 2** gives the measured amplitude response for the composite highpass filter. The results indicate inductor unloaded Qs of approximately 100. As the passband frequency approaches 100 MHz, some modest shape degradation occurs. You can reduce the degradation by using microstrip construction with surface-mount components. You can trim the filter's cutoff frequency by spreading or squeezing the turns of the toroidal inductors. (DI #2533)

TABLE 2–MEASURED AMPLITUDE RESPONSE

Frequency (MHz)	Insertion loss (dB)
29	23.7
30	12.8
31	3.7
31.5	1.8
32	1
33	0.6
35	0.5
40	0.5
45	0.4
50	0.2
55	0.2
60	0.2
70	0.4
100	0.5
130	0.6

REFERENCE

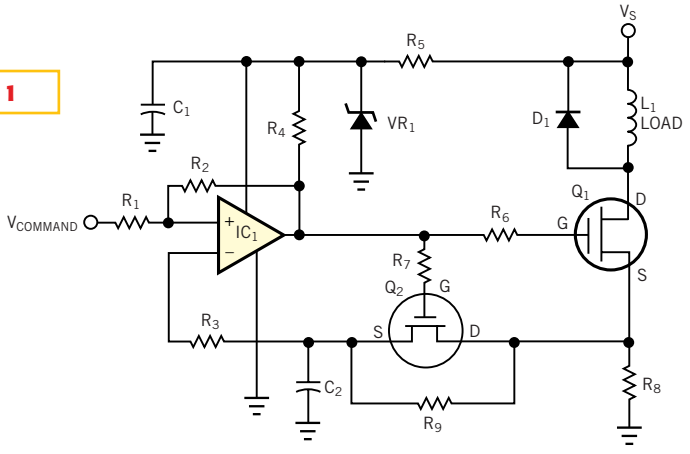
1. "Low Cost Lowpass Filter Design Using Image Parameters," *Applied Microwave & Wireless*, February 1999, pg 72, plus correction May 1999, pg 12.

Circuit efficiently drives inductive loads

Carlisle Dolland, Honeywell Engines and Systems, Torrance, CA

IN THE DRIVER CIRCUIT in **Figure 1**, the system controller provides the $V_{COMMAND}$ signal. $V_{COMMAND}$ equals the desired load current multiplied by R_8. When the controller applies this voltage to R_1, the output of IC_1 goes high, applying voltage to the gates of Q_1 and Q_2. These transistors turn on, allowing load current to flow to ground through Q_1 and R_8. The current in the load ramps up, and a voltage proportional to the load current, sensed by R_8, feeds back to the inverting input of the comparator IC_1. When this voltage exceeds the voltage at the noninverting input, the output of IC_1 goes to ground. Q_1 and Q_2 then switch off. The load current now circulates around the loop comprising D_1 and L_1. During this time, the slope of the load current becomes negative because of the dissipation in D_1 and the load resistance. The duration of this phase of the circuit's operation is a function of the hysteresis (set by R_1, R_2, and R_4) and the decay of the voltage across C_2 (essentially a function of R_9). C_2 and R_9 determine the ripple current in the load. The circuit cannot use a power MOSFET for Q_2, because of the intrinsic drain-to-source diode. You must use a device without the intrinsic diode, such as a 3N71. (DI #2535)

Figure 1



Inductive loads are tricky to drive. This circuit provides efficient drive to relays and solenoids.

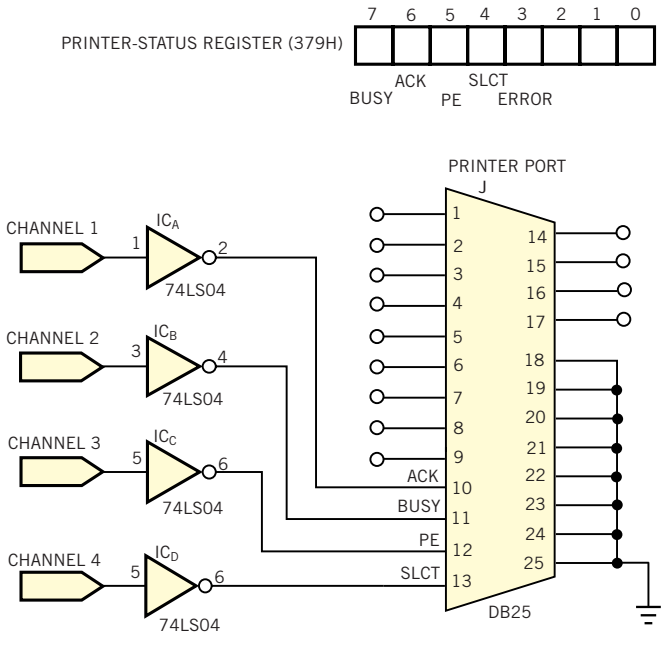
Use a PC to record four-channel waveforms

Dean Chen, Dycam Inc, Chatsworth, CA

THIS DESIGN IDEA is a sequel to a previous one, "Use a printer port to record digital waveforms," *EDN*, June 18, 1998, pg 136. Both ideas are similar: Use the PC's printer port to sample waveforms, and use the PC's memory to store data. The technique presented here expands the capability to four channels. The advantage is that you can see the relationships of the waveforms in the four channels. **Figure 1** depicts the sampling circuit. It uses printer-port pins ACK, BUSY, PE, and SLCT to record signals. The 74LS04 is a buffer between the sampled signals and the printer port. **Listing 1** is the sampling program, written in assembly language. Because there are four channels, every sample needs 4 bits (one nibble) to record. One byte can store two samples: odd and even samples. To accurately record signals, the sampling program needs exclusive access to the CPU.

Execution of the program must take

Figure 1



Use your PC's printer port to record four-channel waveforms.

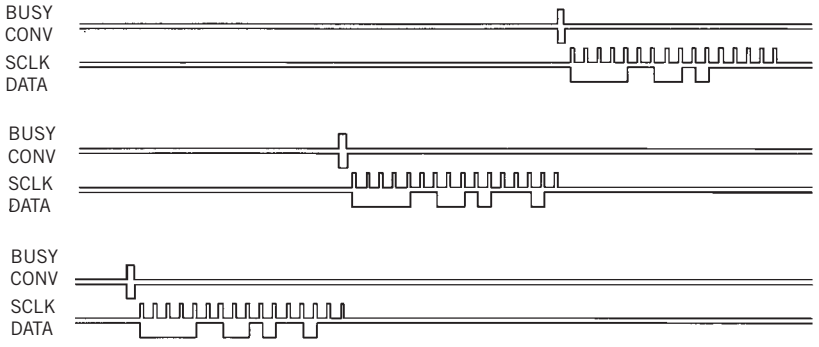
LISTING 1—FOUR-CHANNEL PC-PORT WAVEFORM-SAMPLING ROUTINE

```
;                Printer Status Register
;
;                7  6  5  4  3  2  1  0
;                 -------------------------
;                 |  |  |  |  |  |  |  |
;                 -------------------------
;                 |  |  |  |  |------------ ERROR
;                 |  |  |  |---------------- SLCT
;                 |  |  |------------------- PE
;                   |  |---------------------- ACK
;                   |------------------------- BUSY
;
;
;sta_reg          equ   0379h
;mask_reg         equ   021h
;
code             segment para    public 'code'
                 assume  cs:code
                 org     100h
begin:             jmp main
file_name   db     'samsig.dat',0
msg         db     'Sample Signal is saved in samsig.dat ! $'
;
main             proc near
                lea di,buffer
                mov dx,sta_reg
pe_l:           in al,dx                        ; PE is as Trigger Signal
                and al,20h
                jz  pe_l                        ; When PE from 0 to 1,
pe_h:           in al,dx
                and al,20h                      ; Start Sampling.
                jz  pe_h
                mov dx,mask_reg
                in al,dx
                or al,01h               ; Mask Time Interrupt
                out dx,al
                mov dx,sta_reg
                mov cx,0f000h                   ; Sample Size
sam_lp:
                in al,dx                        ; Even Sample
                shr al,1
                shr al,1
                shr al,1
                shr al,1
                shr al,1
                xchg al,ah              ; high nibble save in ah
                nop
                nop
                nop
                in al,dx                ; Odd Sample
                and al,0f0h             ; get low nibble
                or al,ah                ; 2 nibble form 1 byte
                xor al,077h                     ; correct bits polarity
                stosb


                loop sam_lp
                mov dx,mask_reg
                in al,dx
                and al,0feh                     ; Allow Time Interrupt
                out dx,al
create_file:
                lea dx,file_name                ; memory is full,
                mov cx,0                        ; save data to 'samsig.dat' file
                mov ah,3ch
                int 21h
                mov bx,ax
write_data:
                mov cx,0f000h
                lea dx,buffer
                mov ah,40h
                int 21h
close:                  mov ah,3eh
                int 21h
                lea dx,msg
                mov ah,9
                int 21h
                int 20h
main                endp
;
buffer:
code            ends
                end begin
```

place in pure MS-DOS mode, and not in a Windows multitasking environment. Second, it does not allow interrupts to occur during sampling. You must thus mask interrupts during the sampling procedure. Moreover, you need to equalize the odd and even sampling periods. Because the even sampling period is shorter then the odd one, the routine adds three nonoperation (NOP) instructions in the even sampling period. When the sampled data attains approximately 60 kbytes, the program restores the interrupt-mask register and generates a file named samsig.dat. **Listing 2** is a QBasic program for displaying the recorded waveforms. The program reads and then displays the samsig.dat file. **Figure 2** provides an example, a recording of the command and data signals from an Analog Devices AD7896 A/D converter. You can increase the sampling period by inserting some NOP instructions in the sampling routine. You can download **listings 1** and **2** from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2536. (DI #2536)

Figure 2



Four channels of data from an AD7896 and the timing relationships thereof are visible.

LISTING 2–DISPLAY PROGRAM FOR SAMPLED WAVEFORMS

```
KEY 20, CHR$(0) + CHR$(72):     ON KEY(20) GOSUB UpLine
KEY 21, CHR$(0) + CHR$(80):     ON KEY(21) GOSUB DownLine
KEY 15, CHR$(0) + CHR$(73):     ON KEY(15) GOSUB UpPage
KEY 16, CHR$(0) + CHR$(81):     ON KEY(16) GOSUB DownPage
KEY 22, CHR$(0) + CHR$(75):     ON KEY(22) GOSUB Left
KEY 23, CHR$(0) + CHR$(77):     ON KEY(23) GOSUB Right
KEY 17, CHR$(0) + CHR$(1):      ON KEY(17) GOSUB Finish

SCREEN 12
DIM chr AS STRING * 1
DIM prv(3) AS INTEGER
DIM ptr AS LONG
OPEN "samsig.dat" FOR BINARY AS #1
 GET #1, 1, chr: lo% = ASC(chr) MOD 16
 FOR k% = 0 TO 3
  prv(k%) = lo% MOD 2: lo% = lo% \ 2
 NEXT k%
 d% = 12: dd% = 16: fl% = 0: ptr = 0
 KEY(17) ON

WHILE fl% = 0
 KEY(15) ON: KEY(16) ON: KEY(20) ON
 KEY(21) ON: KEY(22) ON: KEY(23) ON
 LOCATE 1, 36: PRINT ptr
 FOR i% = 0 TO 255: FOR j% = 0 TO 128: NEXT j%
 NEXT i%
 KEY(15) STOP: KEY(16) STOP: KEY(20) STOP
 KEY(21) STOP: KEY(22) STOP: KEY(23) STOP
 FOR i% = 0 TO 4
  y% = i% * 96 + 32
  FOR j% = 1 TO 320
   GET #1, ptr + j% + i% * 320, chr
   lo% = ASC(chr) MOD 16: hi% = ASC(chr) \ 16
   x% = 2 * j%
   FOR k% = 0 TO 3
    IF prv(k%) <> lo% MOD 2 THEN
     LINE (x%, y% + k% * dd%)-(x%, y% + k% * dd% + d%)
    ELSE
     IF (lo% MOD 2) THEN
      PSET (x%, y% + k% * dd%)
     ELSE PSET (x%, y% + k% * dd% + d%)
     END IF
    END IF
    prv(k%) = lo% MOD 2: lo% = lo% \ 2
   NEXT k%
   x% = x% + 1
   FOR k% = 0 TO 3
    IF prv(k%) <> hi% MOD 2 THEN
     LINE (x%, y% + k% * dd%)-(x%, y% + k% * dd% + d%)
    ELSE
     IF (hi% MOD 2) THEN
      PSET (x%, y% + k% * dd%)
     ELSE PSET (x%, y% + k% * dd% + d%)
     END IF
    END IF
    prv(k%) = hi% MOD 2: hi% = hi% \ 2
   NEXT k%
  NEXT j%
 NEXT i%
WEND
 KEY(15) OFF: KEY(16) OFF: KEY(20) OFF
 KEY(21) OFF: KEY(22) OFF: KEY(23) OFF
CLOSE #1
END

UpLine:
 IF ptr < 61120 THEN
  CLS 1: ptr = ptr + 320
 END IF
RETURN
Left:
 IF ptr < 61440 THEN
  CLS 1: ptr = ptr + 1
 END IF
RETURN
UpPage:
 IF ptr < 59840 THEN
  CLS 1: ptr = ptr + 1600
 END IF
RETURN
DownLine:
 IF ptr >= 320 THEN
  CLS 1: ptr = ptr - 320
 END IF
RETURN
Right:
 IF ptr >= 1 THEN
  CLS 1: ptr = ptr - 1
 END IF
RETURN
DownPage:
 IF ptr >= 1600 THEN
  CLS 1: ptr = ptr - 1600
 END IF
RETURN
Finish:
 fl% = 1
RETURN
```

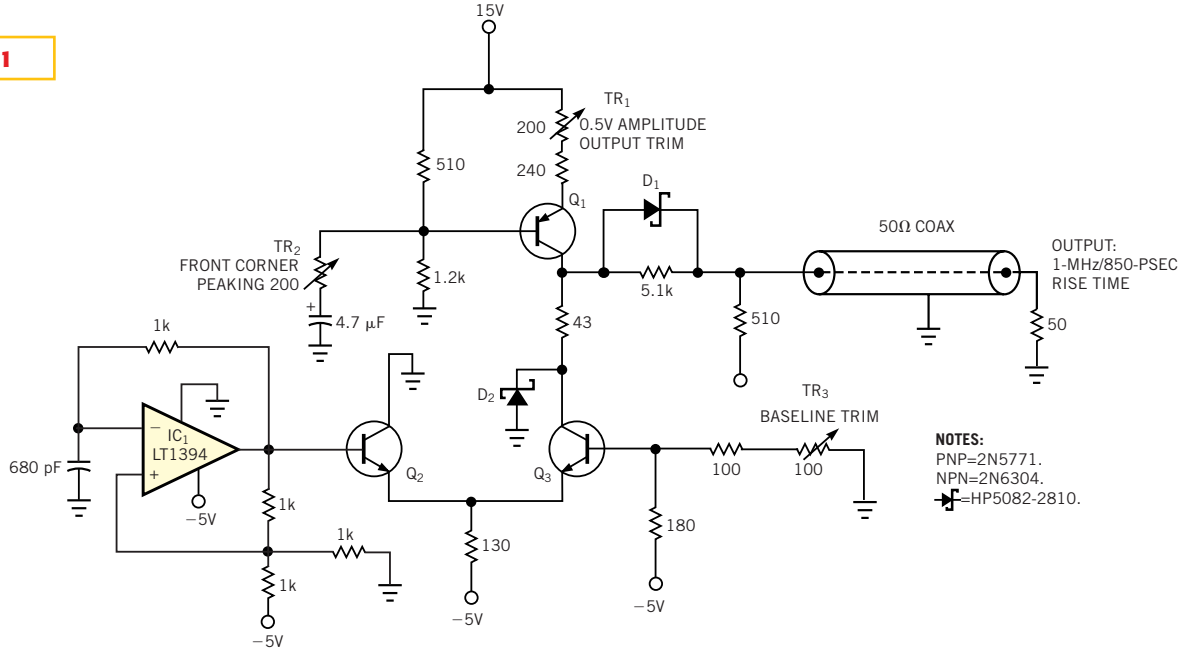
Pulse generator has low top-side aberrations

Jim Williams, Linear Technology Corp, Milpitas, CA

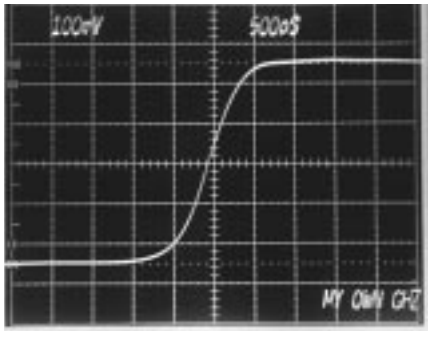
Impulse-response and rise-time testing often require a fast-rise-time source with a high degree of pulse purity. These parameters are difficult to achieve simultaneously, particularly at subnanosecond speeds. The circuit in **Figure 1**, derived from oscilloscope calibrators (**Reference 1**), meets the speed and purity criteria. It delivers an 850-psec output with less than 1% pulse-top aberrations. Comparator IC_1 delivers a 1-MHz square wave to current-mode switch Q_2-Q_3. Note that IC_1 obtains power between ground and −5V to meet the transistors' biasing requirements. Q_1 provides drive to Q_2 and Q_3. When IC_1 biases Q_2, Q_3 turns off. Q_3's collector rises rapidly to a potential determined by Q_1's collector current, D_1, and the output resistors combined with the 50Ω termination resistor. When IC_1 goes low, Q_2 turns off, Q_3 turns on, and the output settles to 0V. D_2 prevents Q_3 from saturating.

The circuit's output transition is extremely fast and singularly clean. **Figure 2**, viewed on a 1-GHz real-time-bandwidth oscilloscope, shows 850-psec rise

Figure 1



Need a fast, clean pulse? This simple circuit provides 500-mV, 850-nsec pulses with a high degree of purity.

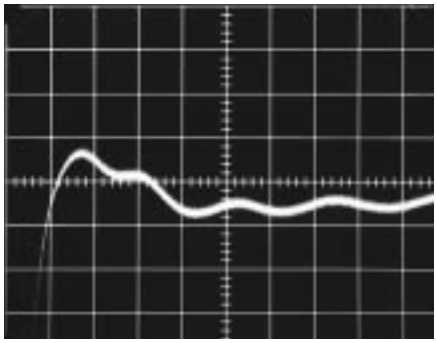


0.1V/DIV

500 pSEC/DIV

Figure 2

Viewed with 1-GHz bandwidth, pulses are free of discontinuities and anomalies.



5 mV/DIV

500 pSEC/DIV

Figure 3

Pulse tops exhibit less than 64 mV, or less than ±1%, aberrations.

time with exceptionally pure pretransition and post-transition characteristics. **Figure 3** details the pulse-top settling. The photo shows the pulse-top region immediately following the positive 500-mV transition. Settling occurs within 400 psec of the edge's completion with all activity within ±4 mV. The 1-mV, 1-GHz ringing undoubtedly stems from breadboard-construction limitations; you can probably eliminate it by using stripline-layout techniques. The level of performance of this circuit requires some trimming. The oscilloscope you use should have at least 1-GHz bandwidth. You adjust trimmers TR_2 and TR_3 for the best pulse presentation. TR_1 sets the output amplitude at 500 mV across the 50Ω termination. The trims are somewhat interactive, although not unduly so, and converge quickly to give the results described. (DI #2530)

REFERENCE

1. 485 Oscilloscope Service and Instruction Manual, "Calibrator," pg 3 to 15, Tektronix Inc, 1973.

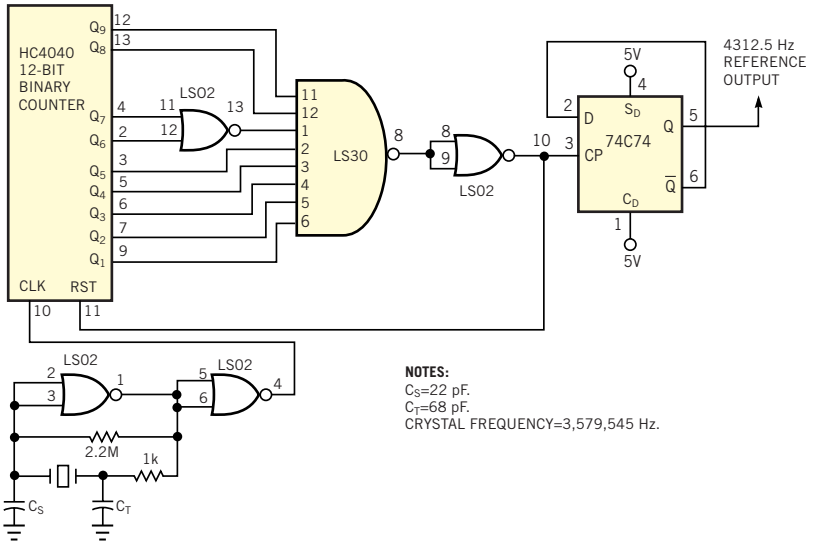
Circuit provides ADSL frequency reference

Bert Erickson, Fayetteville, NY

THE DISCRETE-MULTITONE (DMT) frequencies that asymmetrical-digital-subscriber lines (ADSL) use are integral multiples of a common frequency, and the symbol period is the inverse of this frequency. Integration over the symbol period allows the sine and cosine orthogonal waveform products to vanish for all multiples of the common frequency except for those having the same frequency. As the ADSL standards (TI.413) specify, the 256 channels are separated by 69/16 kHz. You can generate the midchannel frequencies with a PLL, but the reference frequency differs from that of crystals for computers and clocks. However, by using the circuit in **Figure 1**, you can generate the frequency by using a 3.58-MHz crystal to control the horizontal scanning rate in television sets. A typical 3.58-MHz crystal has a tolerance of ±50 ppm and a load capacitance of 18 pF. This tolerance provides a frequency of 3.579366 to 3.579724 MHz. If you multiply this common DMT frequency by 830, the result is 830×69/16 kHz, or 3.579375 MHz, which is 9 Hz above the crystal's lower tolerance limit. Assuming that you can select the C_S and C_T capacitors at either side of the crystal to tune the frequency near the lower tolerance limit, you can also select them for the desired frequency.

In other words, reduce the oscillator frequency with bistable flip-flops and combine the outputs in a NAND gate to divide by 830. For the 3.58-MHz crystal, design values for C_S and C_T were 23.6 and 75.7 pF, respectively. We chose 22 pF for C_S and 68 pF for C_T. A trimmer capacitor in parallel with C_T reduces the frequency. When C_T increased from 22 to 90 pF, the frequency decreased by 448 Hz and handily bridged the 3.579545- and 3.579375-MHz frequencies. Tests showed that the lower frequency was more than 100 Hz below 3.579357 MHz, but the exact number depends on the calibration of the counter. Because 830 is a 10-bit binary number, the circuit divides by 415 first to permit combining with an eight-input NAND gate. A strobe applied to a flip-flop then creates a square wave for the reference-frequency output. (DI #2531)

Figure 1



Using a common TV crystal, you can generate the reference frequency for ADSL systems.

ActiveX control brings bit manipulation to Windows

Steve Hageman, Agilent Technologies, Santa Rosa, Ca

Nothing compares with the C language for working with bits. C provides a rich set of signed and unsigned number formats, along with many intrinsic bit-manipulation operators. However, most of the popular rapid-application-development Windows languages lack C's ability to easily work with bits. Visual Basic is such a language. Although it's hard to find a faster language to develop a small to midsized application in Windows, Visual Basic starts to show its weakness when it comes time to talk to hardware. Hardware programming is usually bit-oriented. That is, it's necessary to turn bits on and off or shift out serial streams to get the hardware to operate correctly. The ActiveX control serves just these types of bit-manipulation needs (**Figure 1**). The control includes functions for changing binary strings to numbers, a hex-output function, the ability to set and clear bits in a word, and the ever-needed shift-left and -right functions. As an example, many of the three-wire serial devices need to have a setup word shifted to them. Suppose you need to shift the setup word 0111 1101 first to an A/D converter to initiate a conversion on some channel. You can use the functions in the ActiveX control to easily effect the shift operation, as follows:

```
Setup_word = Bits ("01111101")
`Returns 125
For i = 0 to 7
    Val = ShiftRight_8(setup_word,0)
    `write val to the A/D here
next i
```

In the above example, val has the values 1, 0, 1, 1, 1, 1, 1, 0 during each iteration of the loop. The routine can then clock these bits to the A/D converter as required by the hardware. If the operation requires MSB first, you can use the ShiftLeft function. The SetBit and ClearBit functions are useful when using a port as clock and data lines, because you can set individual bits as needed instead of doing entire port writes. Any modern programming language that can use ActiveX controls, such as Agilent VEE, Visual Basic, Delphi, and others, can use the functions given here. You can download the ActiveX control from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2534. The routine includes all the functions listed in **Figure 1**, plus a few more, with application examples. (DI #2534)

Figure 1

```
Function GetBit(ByVal x As Long, ByVal n As Integer) As Integer
Returns the value of bit n in input value x. Returns 1 or 0 if bit
is set or not. x = 1 to 16 bit, n = 0 = LSB.
Example: GetBit(16,5) returns 1.

Function Bits(ByVal inval As String) As Long
Given a  representation of a binary string, returns the
value. inval may be any length from 1 to 16 bits
Example: Bits("101") returns 5.

Function BitsStr(ByVal inval As Long, ByVal sizeof As Integer) As String
Given a number, returns with a representation of a binary string.
sizeof is the width of the return field (1 to 16 bits).
Example: BitsStr(82,8) returns "01010010"

Function HexStr(ByVal inval As Long, ByVal sizeof As Integer)
Given a number, returns with a representation of a hex string.
sizeof is the width of the return field (1 to 16 bits).
Example: HexStr(179,8) returns "B3"

Function ClearBit(ByVal x As Long, ByVal n As Integer) As Long
Clears bit position n in input x. Returns new x value.
x may be 1 to 16 bits, n = 0 = LSB
Example: ClearBit(16,4) returns 0.

Function SetBit(ByVal x As Long, ByVal n As Integer) As Long
Sets bit n in input value x. Returns new  x. x may be any
width 1 to 16 bits, n = 0 = LSB.
Example: SetBit(0,4) returns 16

Function ShiftRight_8(ByRef x As Integer, ByVal y As Integer) As Integer
Shifts the 8 bit value x right by 1 place. Bit shifted in is y.
Returns bit shifted out.
Example: ShiftRight_8(129,1) Returns 1 and the new value for x (was 129)
is 192.

Function ShiftRight_16(ByRef x As Long, ByVal y As Integer) As Integer
Shifts the 16 bit value x right by 1 place. Bit shifted in is y.
Returns bit shifted out.
Example: ShiftRight_16(1,1) Returns 1 and the new value for x (was 1)
is 32768.

Function ShiftLeft_8(ByRef x As Integer, ByVal y As Integer) As Integer
Shifts the 8 bit value x left by 1 place. Bit shifted in is y.
Returns bit shifted out.
Example: ShiftLeft_8(1,0) returns 0 and the new value for x (was 1)
is 2.

Function ShiftLeft_16(ByRef x As Long, ByVal y As Integer) As Integer
Shifts the 16 bit value x left by 1 place. Bit shifted in is y.
Returns bit shifted out.
Example: ShiftLeft_16(32768,1) returns 1 and the new value for x
(was 32768) is 1

Function RotateRight_8(ByVal x As Integer) As Integer
Rotates the 8 bit value x right by 1 place. Returns new value.
Example: RotateRight_8(1) returns 128.

Function RotateRight_16(ByVal x As Long) As Long
Rotates the 16 bit value x right by 1 place. Returns new value.
Example: RotateRight_16(1) returns 32768.

Function RotateLeft_8(ByVal x As Integer) As Integer
Rotates the 8 bit value x left by 1 place. Returns new value.
Example: RotateLeft_8(64) returns 128

Function RotateLeft_16(ByVal x As Long) As Long
Rotates the 16 bit value x left by 1 place. Returns new value.
Example: RotateLeft_16(32769) returns 3.

End.....
```

An ActiveX control offers many handy functions for bit manipulation.

Circuit breaker handles voltages to 32V

Greg Sutterlin and Craig Gestler, Maxim Integrated Products, Sunnyvale, CA

The simplicity of low-side current monitoring can mask the advantages of a high-side approach. You can monitor load currents in a power supply, a motor driver, or another power circuit on either the high or the low side (ground). However, don't let the ease of low-side monitoring cause you to overlook its dangers or the advantages of a high-side approach. Various fault conditions can bypass the low-side monitor, thereby subjecting the load to dangerous and undetected stresses. On the other hand, a high-side monitor connected directly to the power source can detect any downstream failure and trigger the appropriate corrective action. Traditionally, such monitors required a precision op amp, a boost power supply to accommodate the op amp's limited common-mode range, and a handful of precision resistors. Now, the MAX4172 IC can sense high-side currents in the presence of common-mode voltages as high as 32V (**Figure 1**). IC_1 provides a ground-referenced current-source output proportional to the high-side current of interest. This output current, equal to the voltage across an external sense resistor divided by 100, produces a voltage output across a load resistor.

IC_1 and a few external parts form a low-cost circuit breaker. R_{SENSE} senses load currents, and Q_1 controls the currents. The design accepts inputs of 10 to 32V; you can easily modify it to operate from voltages as low as 6.5V. The initial application of V_{IN} and V_{CC} places the breaker in its trip state. Pressing S_1 resets the breaker and connects power to the load, thereby activating Q_1, Q_3, and Q_{4B}. Q_3 powers IC_1, and Q_{4B} establishes the overcurrent threshold, $V_{THRESH}=V_{CC}-V_{BE(4B)}$. Because V_{CC} (2.7 to 5.5V typical) equals 5V and the base-emitter voltage of Q_{4B} is approximately 0.7V, V_{THRESH} is typically 4.4V. The circuit trips at a nominal load current of 1A. The values for R_{SENSE}, R_{THRESH}, and R_{OUT} are functions of the system's accuracy and power-dissipation requirements. First, select $R_{SENSE}=50\ m\Omega$ and $R_{THRESH}=10\ k\Omega$. Then, calculate $R_{OUT}=V_{CC}/I_{LOAD}R_{SENSE}G_m$, where I_{LOAD} is the trip point (1A) and G_m (IC_1's typical transconductance) equals 0.01A/v. Thus, $R_{OUT}=10\ k\Omega$.

Applying power to Q_3 and Q_{4B} causes Q_{4B} to conduct, which establishes V_{THRESH} and activates Q_3 to power IC_1. A fraction of the load current through R_{SENSE} mirrors to the IC_1 output and appears as a voltage, V_{OUT}, across R_{OUT}. Q_{4B} turns off when V_{OUT} increases above $(V_{THRESH}+V_{BE(4BA)})$, turning off Q_3 and causing a drop in V^+ (IC_1, pin 8). When V^+ reaches 2.67V (typical), $\overline{PG}$ goes high, thereby tripping the breaker by turning off Q_1. Q_2 adds feedback to ensure a clean turn-off at the trip level. Current draw in the tripped state is minuscule and equals the V_{CC} load current, 0.5 mA typical. Press S_1 to reset the breaker. The design is intended for low-cost applications in which the absolute accuracy of the trip current is not critical. The accuracy, which depends on variations in V_{CC} and the base-emitter voltages of Q_{4A} and Q_{4B} and on the error current through R_4, is approximately ±15% at a trip current of 1A. (DI #2532)

To Vote For This Design,
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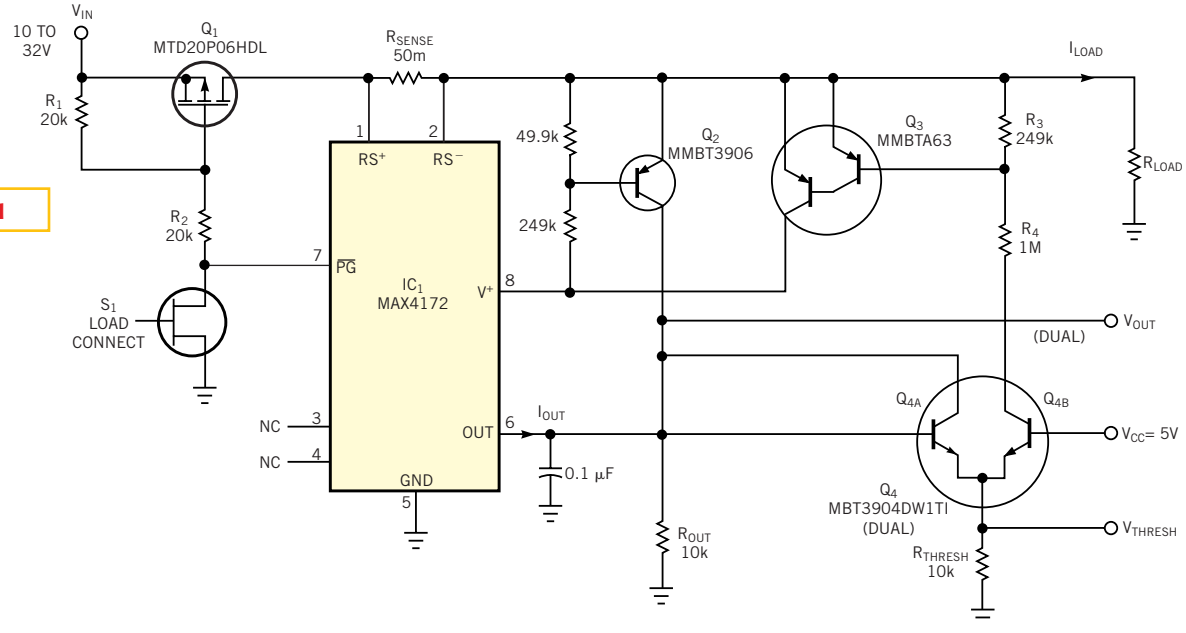
Figure 1



A current-sense amplifier and a few transistors form a low-cost circuit breaker.

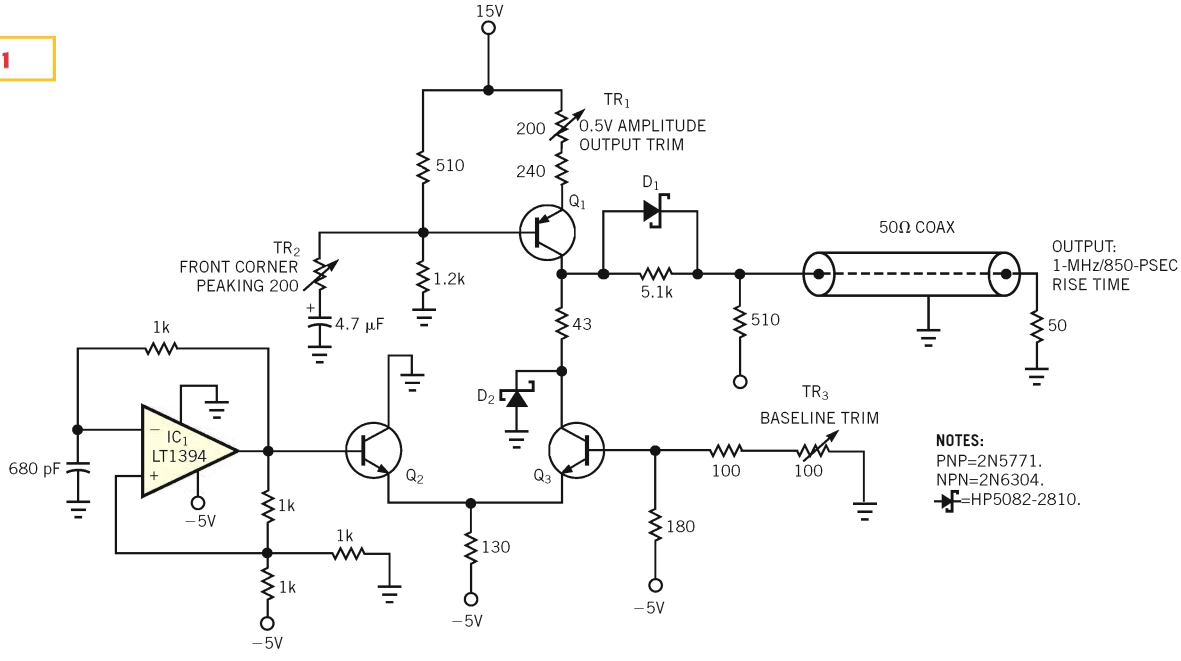
Pulse generator has low top-side aberrations

Jim Williams, Linear Technology Corp, Milpitas, CA

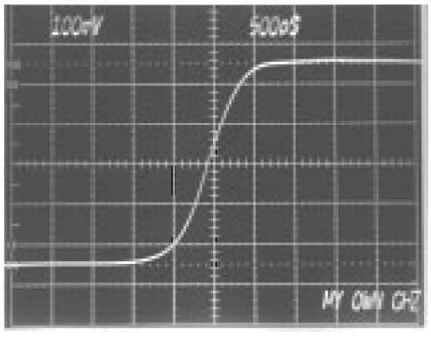
Impulse-response and rise-time testing often require a fast-rise-time source with a high degree of pulse purity. These parameters are difficult to achieve simultaneously, particularly at subnanosecond speeds. The circuit in **Figure 1**, derived from oscilloscope calibrators (**Reference 1**), meets the speed and purity criteria. It delivers an 850-psec output with less than 1% pulse-top aberrations. Comparator IC_1 delivers a 1-MHz square wave to current-mode switch Q_2-Q_3. Note that IC_1 obtains power between ground and −5V to meet the transistors' biasing requirements. Q_1 provides drive to Q_2 and Q_3. When IC_1 biases Q_2, Q_3 turns off. Q_3's collector rises rapidly to a potential determined by Q_1's collector current, D_1, and the output resistors combined with the 50Ω termination resistor. When IC_1 goes low, Q_2 turns off, Q_3 turns on, and the output settles to 0V. D_2 prevents Q_3 from saturating.

The circuit's output transition is extremely fast and singularly clean. **Figure 2**, viewed on a 1-GHz real-time-bandwidth oscilloscope, shows 850-psec rise

Figure 1



Need a fast, clean pulse? This simple circuit provides 500-mV, 850-nsec pulses with a high degree of purity.

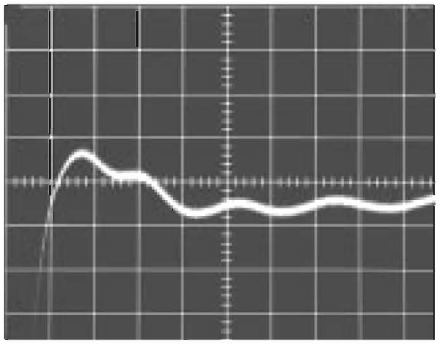


0.1V/DIV

500 pSEC/DIV

Figure 2

Viewed with 1-GHz bandwidth, pulses are free of discontinuities and anomalies.



5 mV/DIV

500 pSEC/DIV

Figure 3

Pulse tops exhibit less than 64 mV, or less than ±1%, aberrations.

time with exceptionally pure pretransition and post-transition characteristics. **Figure 3** details the pulse-top settling. The photo shows the pulse-top region immediately following the positive 500-mV transition. Settling occurs within 400 psec of the edge's completion with all activity within ±4 mV. The 1-mV, 1-GHz ringing undoubtedly stems from breadboard-construction limitations; you can probably eliminate it by using stripline-layout techniques. The level of performance of this circuit requires some trimming. The oscilloscope you use should have at least 1-GHz bandwidth. You adjust trimmers TR_2 and TR_3 for the best pulse presentation. TR_1 sets the output amplitude at 500 mV across the 50Ω termination. The trims are somewhat interactive, although not unduly so, and converge quickly to give the results described. (DI #2530)

Reference

1. 485 Oscilloscope Service and Instruction Manual, "Calibrator," pg 3 to 15, Tektronix Inc, 1973.

 By Jim Williams and David Beebe, Linear Technology Corp

LOW-VOLTAGE SYSTEMS OFTEN NEED A LOCALLY GENERATED HIGH VOLTAGE. EVEN FOR AN APPLICATION AS NOISE-SENSITIVE AS VARACTOR-DIODE BIASING, A CAREFULLY PLANNED SWITCHING-REGULATOR-BASED DESIGN AND LAYOUT CAN PROVIDE THE NECESSARY BIAS VOLTAGE.

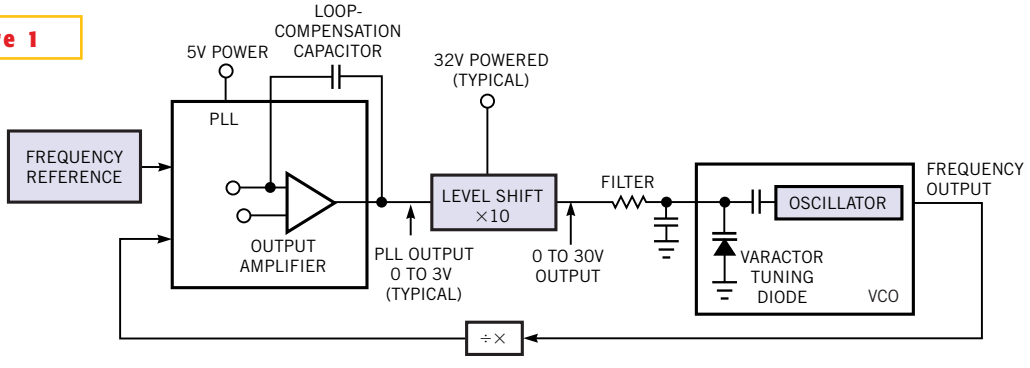
Switching-regulator supply provides low-noise biasing for varactor diodes

Telecommunication, satellite links, and set-top boxes require tuning of a high-frequency oscillator. The actual tuning element is a varactor diode, which is a two-terminal device that changes capacitance as a function of reverse-bias voltage (see **sidebar** "Variable-capacitance diodes"). The oscillator is part of a frequency-synthesizing loop (**Figure 1**). A PLL compares a divided-down representation of the oscillator with a frequency reference. The circuit level shifts the PLL's output to provide the high voltage necessary to bias the varactor, which closes a feedback loop by voltage tuning the oscillator. This loop forces the VCO (voltage-controlled oscillator) to operate at a frequency determined by the frequency reference and the divider's division ratio.

The high-voltage bias is necessary to achieve wide-range varactor operation. **Figure 2** shows varactor-capacitance versus reverse-voltage curves for a family of devices. A 10-to-1 capacitance shift is available, although a 0.1 to 30V swing is necessary. The curves in **Figure 2** are characteristic of typical hyperabrupt devices. Response modification is possible with compromises in performance, particularly with linearity and sensitivity.

Designers traditionally meet the bias-voltage requirement using the existing high-voltage rails. However, the current trend toward low-voltage-powered systems means that you must locally generate the high-voltage bias. Local generation of a high voltage implies the presence of some form of voltage-step-up switching regulator. You can use a step-up approach, but varactor-noise sensitivity complicates the design. In particular, the varactor responds to any form of amplitude variation of its bias,

Figure 1

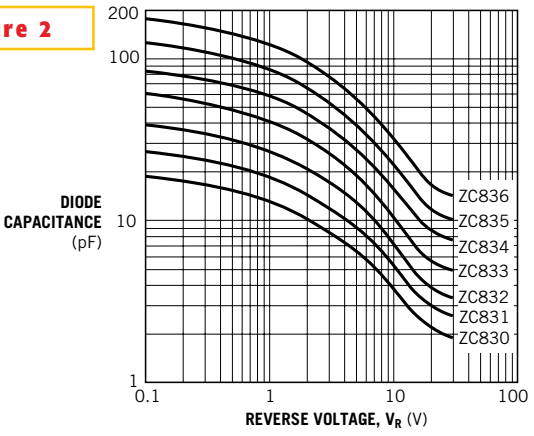


In this typical PLL-based frequency synthesizer, a level shift, which requires a 32V supply, furnishes a 0 to 30V bias for the VCO's varactor.

which results in an undesired capacitance shift. Such a shift causes VCO-frequency movement, resulting in spurious oscillator outputs. The PLL's loop action removes dc and low-frequency shifts, but activity outside the loop's passband causes undesired outputs. Most applications require that any spurious oscillator outputs, or spurs, are at least 80 dB below the nominal output frequency.

All of these requirements necessitate a low-noise, high-voltage supply and mandate caution in the switching-regulator design. Switching regulators are often associated with noisy operation, which makes a varactor-bias application seem hazardous. Careful preparation can eliminate this concern and allows for a practical switching-regulator-based approach to varactor biasing.

Figure 2



The most important characteristic of a varactor diode is the capacitance-voltage relationship. For the varactors and their associated curves in this figure, a 0.1 to 30V swing results in approximately a 10-times capacitance shift.

SIMPLE BOOST REGULATOR

In theory, a simple flyback regulator works for this application, but component choice and attention to layout are critical to achieving low noise. Additionally, component count, size, and cost are usually considerations in varactor-bias applications. **Figure 3a** shows a step-up switching regulator that, properly incarnated, permits low-noise varactor biasing. The circuit is a simple boost regulator. L_1, in conjunction with the SW pin's ground-referred switching, provides voltage step-up. D_1 and C_2 filter the output to dc. D_2 clips possible L_1 negative excursions. The feedback resistor ratio sets the loop servo point and, hence, the output voltage. C_3 tailors the loop's frequency response, minimizing switching-frequency ripple components at the output. C_1 and C_2 exhibit low-loss dynamic characteristics, and the 1.7-MHz switching frequency of the regulator IC allows miniature, small-value components. The relatively high switching frequency also means that ancillary downstream filtering is possible with similarly miniature, small-value components.

Layout is the most crucial design aspect for obtaining low noise. **Figure 3b** shows a suggested layout. The layout distributes ground, V_{IN}, and V_{OUT} in planes to minimize impedance. The IC's GND pin, pin 2, carries high-speed, switched current; this current's path to the circuit's power exit should be direct and highly conductive at all frequencies. R_2's return current should not mix with pin 2's large dynamic currents. The location of C_1 and C_2 should be close to pin 5 and D_1, respectively. The grounded ends of these capacitors should tie directly to the ground plane. L_1 has a low-impedance path to V_{IN}; the driven end of L_1 returns directly to pin 1 of the IC. D_1 and D_2 should have short, low-inductance runs to C_2 and pin 2, respectively. Also, the common connection of D_1 and D_2 should mate tightly with pin 1 and L_1. Pin 1 has a small area, which minimizes radiation. Note that planes operating at ac ground enclose pin 1, thereby forming a shield. The layout further shields the feedback node, pin 3, from switching radiation, preventing unwanted interaction. Finally, the layout should orient L_1

VARIABLE-CAPACITANCE DIODES

By Neil Chadderton, Zetex Inc

The varactor diode capitalizes on the properties of the depletion layer of a p-n diode. Under reverse bias, the carriers in each region—holes in the p type and electrons in the n type—move away from the junction, leaving an area that is depleted of carriers. Thus, reverse bias creates a region that is essentially an insulator and comparable to the classic parallel-plate-capacitor model. The effective width of this depletion region increases with reverse bias, and, consequently, the capacitance decreases. Thus, the depletion layer effectively creates a voltage-dependent-junction capacitance that can vary between the forward conduction region and the reverse breakdown voltage.

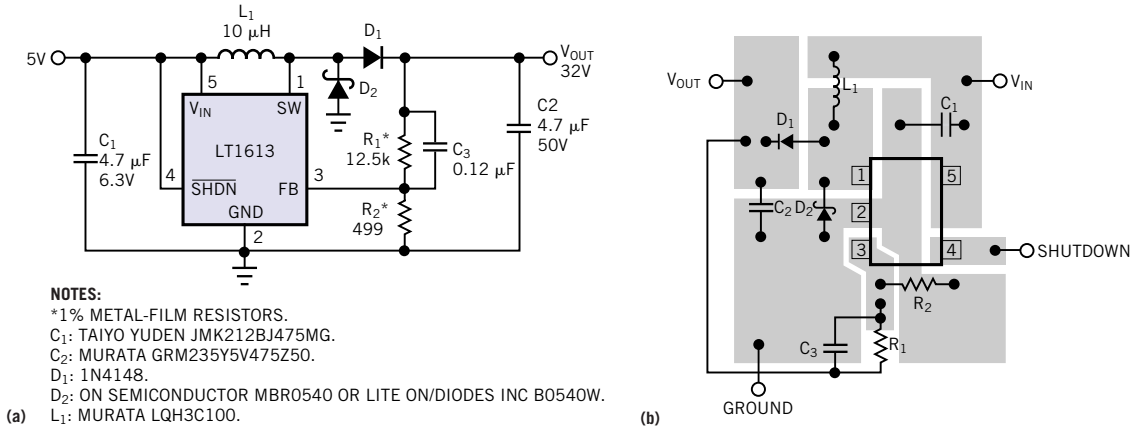
Manufacturers can produce varactor diodes with different junction profiles that exhibit different CV (capacitance-voltage) characteristics. Varactor types include those that exhibit a small range of capacitance to types that show a large change in capacitance for a relatively small change in bias voltage. This feature is particularly useful in battery-powered systems where the available bias voltage is limited.

When you choose a varactor diode, you should consider numerous device characteristics. The most important characteristic is the CV curve that summarizes the range of useful capacitance and also shows the shape of the CV relationship, which may be relevant when a specific response is necessary. Factors to consider include the circuit's operational frequency range and, hence, the appropriate capacitance range, the available bias voltage, and the required response. The quality factor, or Q, at a particular condition is a useful parameter in assessing the performance of a device in tuned circuits. With respect to stability, the temperature coefficient of capacitance as capacitance changes may also be relevant. The reverse breakdown voltage, V_{BR}, also has a bearing on device selection because this parameter limits the maximum reverse bias that you can use to achieve the minimum capacitance.

REFERENCE

1. Chadderton, Neil, "Zetex variable capacitance diodes," Application Note 9, Zetex plc, www.zetex.com.

Figure 3



NOTES:
*1% METAL-FILM RESISTORS.
C_1: TAIYO YUDEN JMK212BJ475MG.
C_2: MURATA GRM235Y5V475Z50.
D_1: 1N4148.
D_2: ON SEMICONDUCTOR MBR0540 OR LITE ON/DIODES INC B0540W.
L_1: MURATA LQH3C100.

A boost regulator with the appropriate components (a) and layout (b) has the necessary low-noise characteristics for varactor biasing. Proper layout requires attention to component placement and ground-current-flow management. A compact layout reduces parasitic inductance, radiation, and crosstalk. A good grounding scheme minimizes return-current mixing.

so that its radiation causes minimal circuit disruption.

The low-voltage PLL output in **Figure 1** requires an analog-level shift to bias the varactor. **Figure 4** shows some alternatives. In **Figure 4a**, the LT1613 regulator IC's 32V output powers the amplifier. The feedback ratio sets a gain of 10, resulting in a 0 to 30V output for a 0 to 3V

PREAMPLIFIER AND OSCILLOSCOPE SELECTION

The low-level measurements this article describes require some form of preamplification for the oscilloscope. Current oscilloscopes rarely have sensitivities greater than 2 mV/DIV, although older instruments offer more capability. Table A lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurements. These units feature wideband, low-noise performance. It is particularly significant that many of these instruments are no longer in production in keeping with current instrumentation trends that emphasize digital-signal acquisition as opposed to analog-measurement capability.

The monitoring oscilloscope should have adequate bandwidth and exceptional trace clarity. High-quality analog oscilloscopes are unmatched in trace clarity. The exceptionally small spot size of these instruments is well-suited to low-level-noise measurement. In our work, we have found Tektronix's 454, 454A, 547, and 556 to be excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise-floor-limited background. The digitizing uncertainties and raster-scan limitations of DSOs impose display-resolution penalties. Many DSO displays do not even register the small levels of switching-based noise.

TABLE A–REPRESENTATIVE PREAMPLIFIERS AND OSCILLOSCOPE PLUG-INS

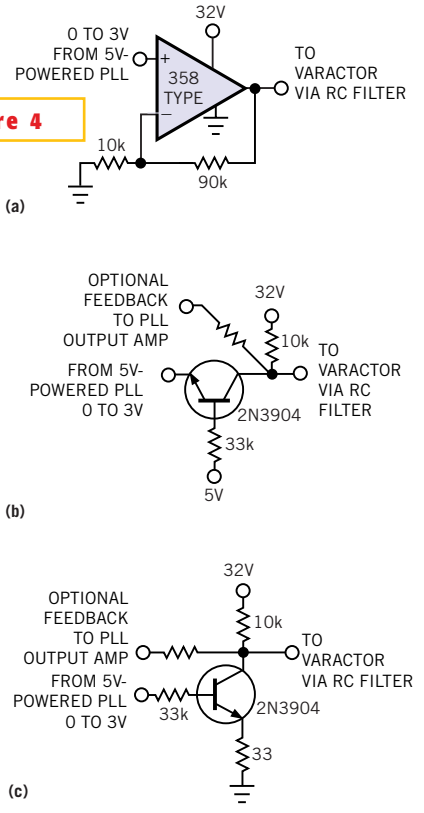
Instrument type	Manufacturer	Model	Bandwidth (MHz)	Maximum sensitivity/gain	Availability	Comments
Amplifier	Hewlett-Packard	461A	150	Gain=100	Secondary market	50Ω input, stand-alone
Differential amplifier	Preamble	1855	100	Gain=10	Current production	Stand-alone, settable band stops
Differential amplifier	Tektronix	1A7/1A7A	1	10 µV/DIV	Secondary market	Requires 500 series mainframe settable band stops
Differential amplifier	Tektronix	7A22	1	10 µV/DIV	Secondary market	Requires 7000 series mainframe settable band stops
Differential amplifier	Tektronix	5A22	1	10 µV/DIV	Secondary market	Requires 5000 series mainframe settable band stops
Differential amplifier	Tektronix	ADA-400A	1	10 µV/DIV	Current production	Stand-alone with optional power supply, settable band stops
Differential amplifier	Preamble	1822	10	Gain=1000	Current production	Stand-alone, settable band stops
Differential amplifier	Stanford Research Systems	SR-560	1	Gain=50,000	Current production	Stand-alone, settable band stops battery or line operation

input. **Figure 4b** is a noninverting common-base stage. The gain in this circuit is less well-controlled than in **Figure 4a**, but overall frequency-synthesizer loop action obviates this concern. **Figure 4c**'s common-emitter circuit is similar to **Figure 4b**'s except that it inverts the signal to the varactor.

Figure 5 combines the considerations mentioned above into a realistic test circuit. The 5V-powered design comprises the LT1613 regulator, an amplifier-based level shift, and a VCO operating in the gigahertz region. Using a filtered LT1004 reference and a gain of 10, the circuit biases the amplifier to a 12V output, which simulates a typical varactor-bias point. The regulator configuration's low-noise output receives additional filtering via the 100Ω, 0.1-µF network at the amplifier power pin and by the amplifier's PSRR (power-supply rejection ratio). The RC combination provides a theoretical, or unloaded, break below 20 kHz, and you can derive the amplifier's PSRR benefit from **Figure 6**. This graph shows PSRR versus frequency for a typical amplifier. There is a steep roll-off beyond 100 Hz, although almost 20 dB of attenuation is available in the megahertz region. This attenuation implies that the amplifier provides some beneficial filtering of the LT1613's residual 1.7-MHz switching components.

A final RC filter section sits directly at the VCO-varactor-bias input. Ideally, this filter's break frequency is far away from the 1.7-MHz switching rate for maximum ripple attenuation. In practice, the filter is within the PLL, which places restrictions on how much delay the filter can introduce. A PLL bandwidth of 5 kHz is usually desirable and dictates a filter point of about 50 kHz to ensure closed-loop stability. As such, the design sets the final RC filter—1.6 kΩ and 0.002 µF—at this frequency. It is worth noting that the varactor's input resistance is high—essentially that of a reverse-biased diode—and no filter buffering is necessary to drive it.

Figure 4



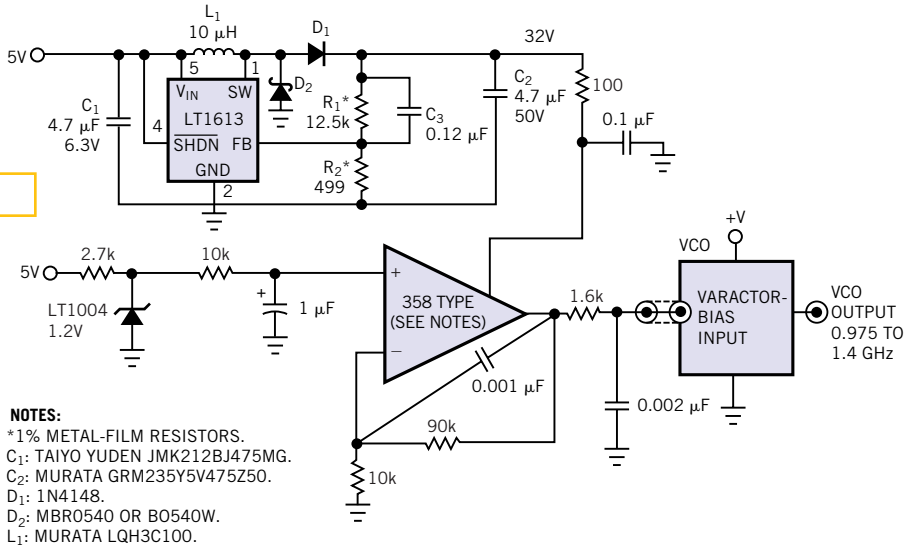
Level-shift options include an op amp (a), a noninverting common-base configuration (b), and an inverting common-emitter configuration (c). The op amp's operating point is inherently stable; the other options rely on PLL closed-loop action or optional feedback.

ANALYZING NOISE PERFORMANCE

Careful measurements permit verification of circuit-noise performance (see **sidebar** "Preamplifier and oscilloscope selection"). **Figure 7a** shows ripple of approximately 2 mV at the LT1613's 32V output. Taken at the amplifier power pin, **Figure 7b** shows the effect of the 100Ω, 0.1-µF filter. Ripple and noise decrease to about 500 µV. **Figure 7c**, recorded at the amplifier output, shows the influence of amplifier PSRR. Ripple and noise further decrease to approximately 300 µV. The actual ripple component is approximately 100 µV. The final RC filter, located directly at the VCO varactor input, gives approximately 20 dB of further attenuation. **Figure 7d** shows ripple and noise inside 20 µV with a ripple component of about 10 µV.

The above results require good measurement technique and the use of a coaxial probing environment (**Reference 1**). Deviations from this regime produce misleading and pessimistic indications. For example, **Figure 8a** shows a 50% amplitude error over **Figure**

Figure 5



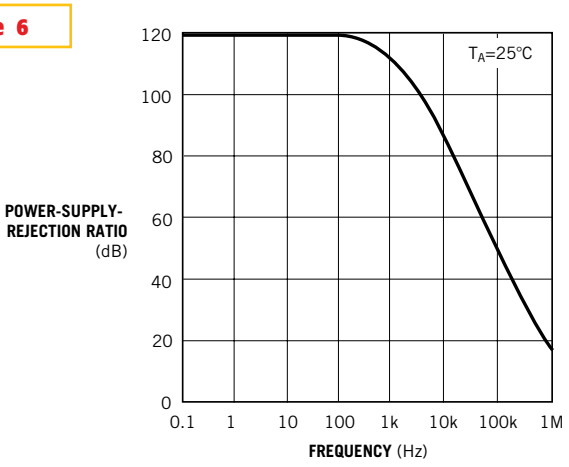
NOTES:
*1% METAL-FILM RESISTORS.
C_1: TAIYO YUDEN JMK212BJ475MG.
C_2: MURATA GRM235Y5V475Z50.
D_1: 1N4148.
D_2: MBR0540 OR BO540W.
L_1: MURATA LQH3C100.
VCO: MINI-CIRCUITS POS-1400.
DO NOT USE OTHER SIDE OF 358 DUAL OP AMP.
WIRE AS GROUNDED INPUT FOLLOWER.
ALTERNATIVELY, LT1006 MAY BE USED.

The noise-test circuit includes a step-up switching regulator with only one inductor, a biased-op-amp level shift, filtering elements, and a gigahertz-region VCO.

7a, even though the scope probe nominally monitors the same point. The difference between these two figures results from **Figure 8a**'s use of a 3-in. probe-ground lead instead of **Figure 7a**'s use of a coaxial ground-tip adapter. Similarly, the 500-mV measurement at **Figure 7b**'s amplifier power pin degrades to **Figure 8b**'s indicated 2-mV representation using the 3-in. probe-ground strap. The same ground strap causes error in **Figure 8c**'s apparent 2-mV amplifier output unlike **Figure 7c**'s correct 300-mV excursion. **Figure 8d** shows a 70-mV indication at the VCO varactor input using the 3-in. ground strap, which is different from **Figure 7d**'s 20-mV data taken with the coaxial ground-tip adapter. (If you don't think 70 mV is a long way from 20 mV, you should consider your reaction to a 3.5-times income-tax reduction.)

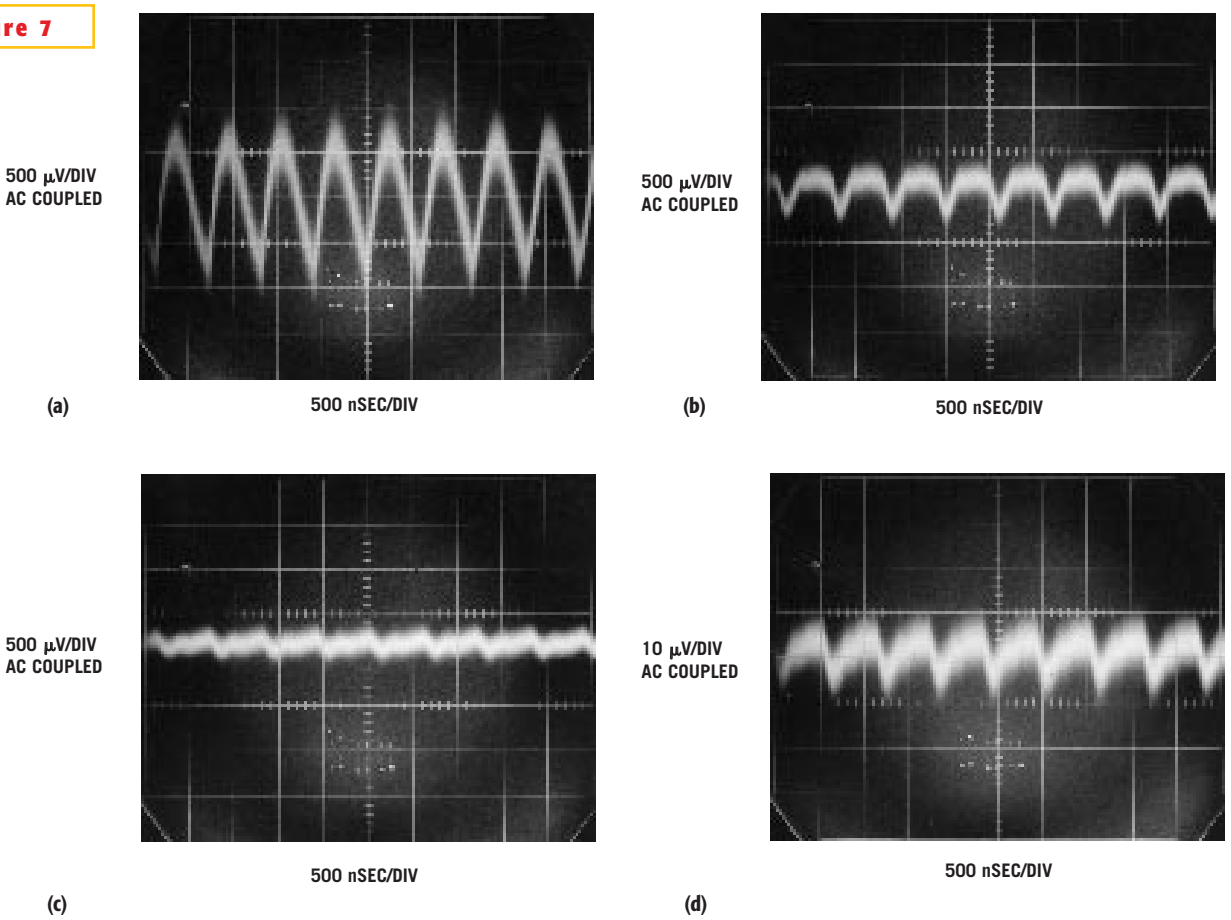
When using the coaxial ground-tip adapter (**Figure 8e**), the VCO varactor input shows a blizzard of noise, compared with **Figure 7d**'s orderly trace, because a 12-in. voltmeter lead connects to the input point. Pickup and stray RF act against the node's finite output impedance, corrupting the measurement. **Figure 8f**, also tak-

Figure 6



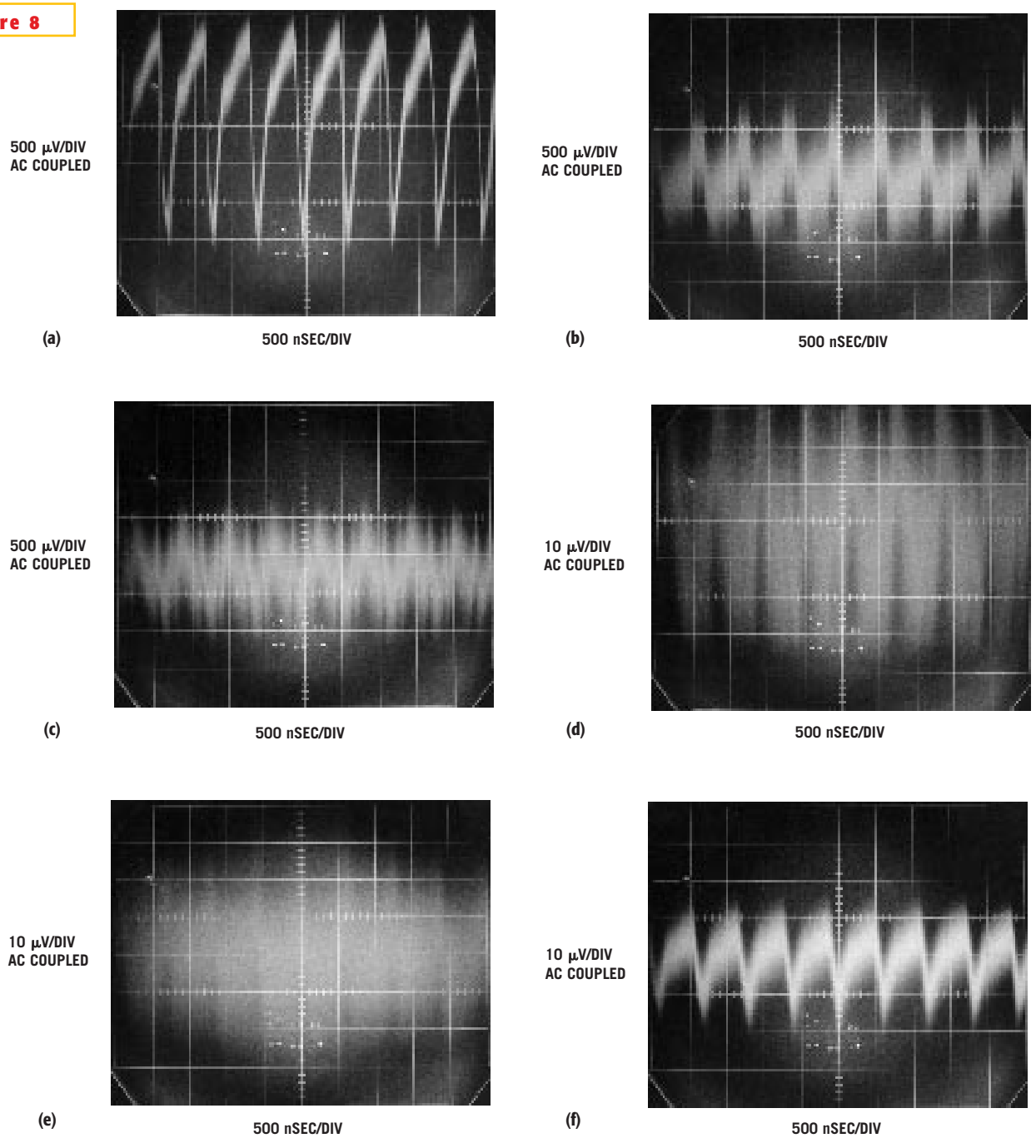
The typical op amp's PSRR degrades with frequency, although nearly 20 dB is available in the LT1613's megahertz switching range.

Figure 7



The regulator's output shows ripple and noise of 2 mV p-p (a). The RC filter at the amplifier's power-input pin reduces ripple and noise to 500 µV p-p (b). The amplifier output shows additional filtering due to the amplifier's PSRR; any aberrations are inside 300 µV (c). The result is the VCO varactor-bias input, which displays less than 20 µV of ripple and noise after the 50-kHz RC filter (d).

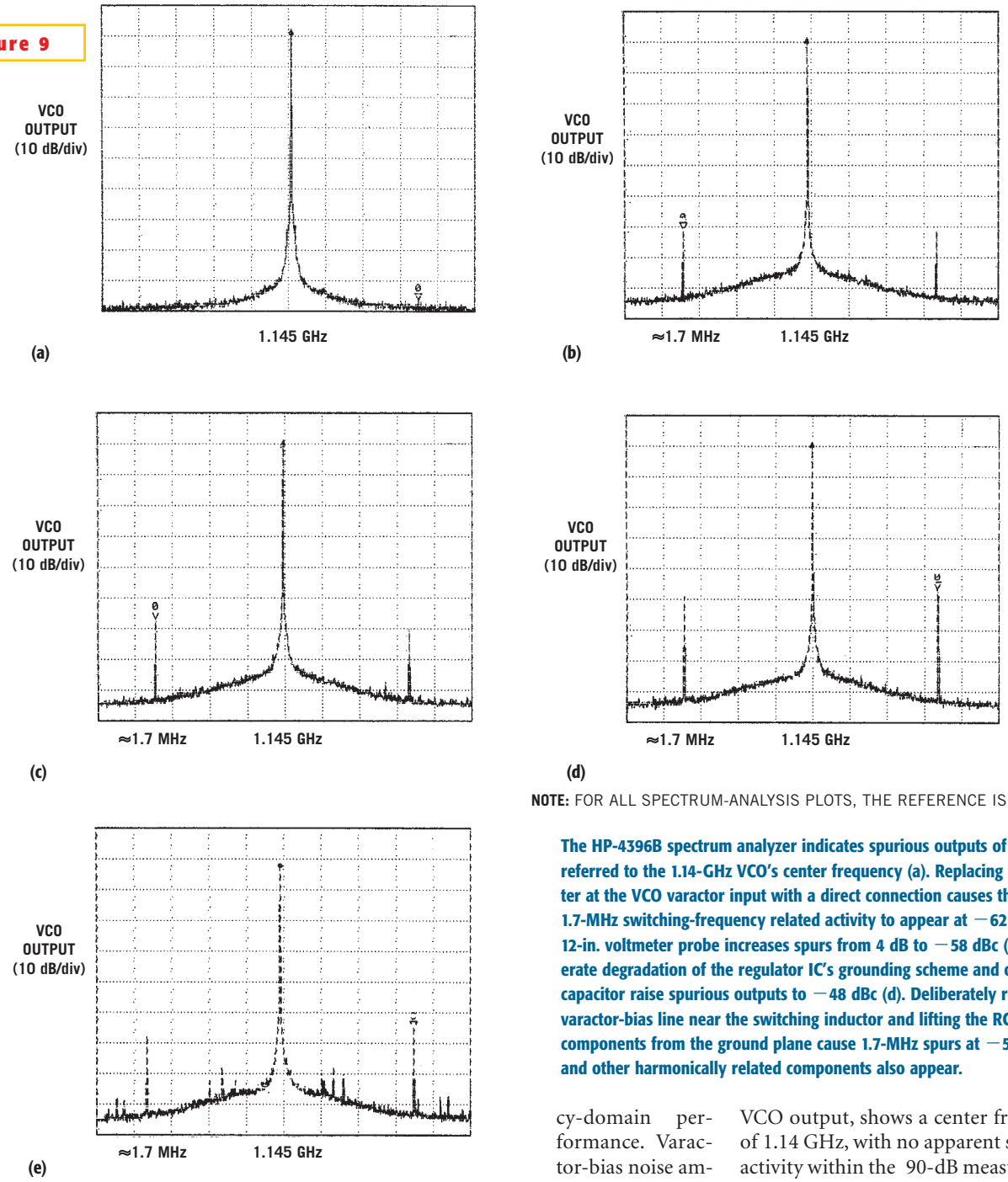
Figure 8



Improper probing technique leads to erroneous results. A 3-in. ground lead causes a 50% display error versus Figure 7a's purely coaxial measurement (a). A 3-in. ground lead degrades Figure 7b's 500-µV reading to 2 mV (b). A probe-ground strap causes an erroneous 2-mV indication compared with the actual value of Figure 7c's 300-µV reading (c). A probe-ground strap causes 3.5-times readout error versus Figure 7d's correctly measured 20 µV (d). A 12-in. voltmeter probe introduces a 2.5-times measurement error to Figure 7d's results (e). An oscilloscope trigger-channel probe also causes a 50% measurement error (f).

en at the VCO input, is clearer than **Figure 8e** but still shows greater than 50% error. The culprit is a second probe, which on the LT1613 VSW pin and triggers the oscilloscope. Even with coaxial techniques in use at both probe points, the trigger probe dumps transient currents into the ground plane. This current introduces small common-mode volt-

Figure 9



NOTE: FOR ALL SPECTRUM-ANALYSIS PLOTS, THE REFERENCE IS 15 dBm.

The HP-4396B spectrum analyzer indicates spurious outputs of −90 dBc referred to the 1.14-GHz VCO's center frequency (a). Replacing the RC filter at the VCO varactor input with a direct connection causes the LT1613's 1.7-MHz switching-frequency related activity to appear at −62 dBc (b). A 12-in. voltmeter probe increases spurs from 4 dB to −58 dBc (c). Deliberate degradation of the regulator IC's grounding scheme and output capacitor raise spurious outputs to −48 dBc (d). Deliberately routing the varactor-bias line near the switching inductor and lifting the RC filter components from the ground plane cause 1.7-MHz spurs at −54 dBc (e), and other harmonically related components also appear.

ages, resulting in a noise increase. One approach is to trigger the oscilloscope with a noninvasive probe (**Reference 1**).

CHECKING RESULTS

Although the varactor-bias noise-amplitude measurements are critical, it is difficult to correlate them with frequency-domain performance. Varactor-bias noise amplitude translates into spurious VCO outputs, which is the measurement of ultimate concern. Although it is possible to view the gigahertz-region VCO on an oscilloscope, a time-domain measurement lacks adequate sensitivity to detect spurious activity. You should use a spectrum analyzer. **Figure 9a**, a spectral plot of the VCO output, shows a center frequency of 1.14 GHz, with no apparent spurious activity within the 90-dB measurement noise floor. The marker at 1.7 MHz (3.5 divisions from center), corresponds to the LT1613's switching frequency. No distinguishable activity is apparent at approximately −90 dBc. Succeeding figures "sanity-check" this performance by systematically degrading the circuit and noting results. In **Figure 9b**, a direct connection replaces the VCO varactor

input's RC filter. The 1.7-MHz spurious outputs are clearer at approximately −62 dBc. Connecting a 12-in. voltmeter lead to the measurement point results in a 4-dB degradation to approximately −58 dBc (**Figure 9c**). **Figure 9d** shows effects due to poor LT1613 layout. (A power-ground pin is routed circuitously, rather than directly, back to input common.) The **figure** also shows poor component choice, such as a lossy capacitor for C_2. In this case, spurious activity jumps to −48 dBc. Even with the proper layout and components, you can see problems in **Figure 9e** when you move the varactor-bias line close to switching inductor L_1. The bias line and RC-filter components are also farther away from the ground plane in **Figure 9e** than in the previous plots. The resultant electromagnetic pickup and increase in bias-line effective inductance cause 1.7-MHz spurs at −54 dBc. Additional harmonically related activity, although less severe, is also apparent. When you restore the bias line and RC filter to their proper orientation, the resultant plot is essentially identical to **Figure 9a**.

In sum, layout and measurement practices are at least as important as circuit design. As always, "the hidden schematic dominates performance," which is a favorite quotation of Charly Gullett of Intel Corp.□

Authors' biographies

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), has been writing technical articles for EDN *for 25 years (see pg 45). He specializes in analog-circuit and -instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.*

David Beebe is associate design engineer at Linear Technology Corp (Milpitas, CA), where he has worked for five years. In his current position, he helped develop a line of bipolar, low-power, and micropower switching power supplies. He attended the College of San Mateo (San Mateo, CA), Mission College (Santa Clara, CA), and Community College of the Air Force (Montgomery, AL). Sparetime interests include acting as a mechanic and pit-crew member for Cliff Blackwell's No. 27B Sprint Car in Northern California.

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5. McAbel, WE, "Probe Measurements," Tektronix Inc, 1971.

Thank you, Bill Hewlett

IT WAS A SIMPLE DEAL. If my next report card had a B average, my parents would give me a trip or two weeks at summer camp. My grandfather suggested New York City where I could see Mickey Mantle (his hero) play at Yankee Stadium. My mother liked Yellowstone National Park, and my dad came up with Washington, DC, or sailing around Mackinac Island. I wasn't interested in summer camp, and I didn't want to go to any of these places.

It's not that I was being intentionally difficult or oppositional. I wasn't. I knew exactly where I wanted to go: 1501 Page Mill Road in Palo Alto, California, the home of Hewlett-Packard—the only place I really wanted to see because it was there that the company actually designed and built all their great stuff and then wrote it up in the *HP Journal*. And maybe, just maybe, if I was incredibly lucky, I'd get to meet my hero, Bill Hewlett. Wow.

I never made the trip. I did poorly in Math (C−) and flat-out flunked science class, so I didn't get to meet him. Now, his recent passing makes me wonder how meeting him then would have affected me. It couldn't have been anything but positive.

Bill Hewlett was the essence of greatness in every sense of the word. He lived a professional and personal life of sterling, uncorrupted excellence. Given his character, it seems reasonable that Hewlett-Packard became not just a great company but a national treasure. The breadth and depth of HP product innovation during Bill's tenure is without parallel. The "HP Contribution" was not a vacuous corporate slogan. He would not build a product unless it offered genuine advancement. One could only marvel at the sheer engineering horsepower and the utter finesse of a Hewlett-Packard product.

The management structure Bill and his buddy Dave Packard put in place was equally rigorous and startling. Individual respect and trust, generous leave and medical benefits, profit sharing, employee stock ownership, and other similar benefits were radical notions more than 40 years ago. Characteristically, Hewlett felt his most significant accomplishment was that the management values instilled in HP permitted the company to prosper without him.

Such exceptional professional accomplishment could come only from an exemplary set of personal values. More than anything, Bill Hewlett was a gentleman. His integrity and sense of ethics was flawless. He once settled a patent issue without lawyers—only an apology, a handshake, and a check. He understood wealth and never allowed it to define him. He lived quietly, with no interest in constructing badges or displays. He built hospitals. In a world full of pretentious disappointments, he quietly stood out as everything a public figure can and should be. He was a great man.

Bill Hewlett was the very best that engineering and humanity has to offer. The contribution is incomparable; the loss, incalculable. Thank you, Bill Hewlett, for all that you did and all that you were.

Hands-on management the HP way. Hewlett (center) discusses an instrument's innards with two engineers at YHP, HP's Japanese operation (1963) (courtesy Agilent Technologies).

Hewlett (center), Packard (left), and Bill Gates (right) at Stanford University in 1996. Hewlett built numerous buildings for his and others' alma maters but would not allow his name to appear on any (courtesy Stanford University).

HP's first product, an audio oscillator, derived directly from Hewlett's master's thesis. It provided a direction, methods, and standards that are reflected in HP and Agilent products to this day.

FOR THE PRICE OF A SAN FRANCISCO DINNER, YOU CAN PUT STANDARDS-LAB PERFORMANCE ON A CIRCUIT BOARD. PART 1 OF THIS THREE-PART ARTICLE CHRONICLES A 1-PPM DAC AND ITS VARIOUS DESIGN OPTIONS, PART 2 IN THE NEXT ISSUE PRESENTS VERIFICATION TECHNIQUES, AND PART 3 DISCUSSES THE HANDLING OF PARASITIC EFFECTS.

20-bit DAC demonstrates the art of digitizing 1 ppm Part 1: exploring design options

If you design and use precision instruments, a 1-ppm measurement is a nearly impossible dream. This level of performance used to be attainable only from large, slow, and expensive instruments that require extreme care in handling and use. However, now a DAC design that uses a simple, powerful feedback loop can capture the magic 1-ppm level using approximately $100 worth of components (**Figure 1**).

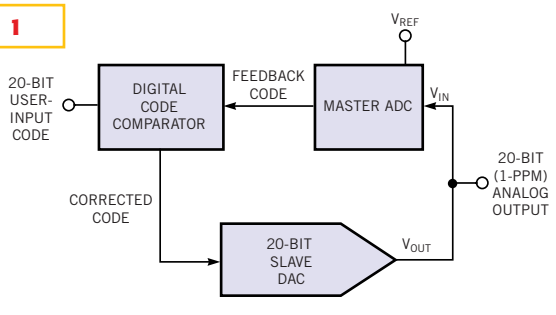
High-precision, instrumentation-grade digital-to-analog conversion has undergone significant progress (see www.ednmag.com/ednmag/reg/2001/04122001/08ms743.htm for "A history of digital-to-analog conversion"). Ten years ago, 12-bit DACs were premium devices. Today, 16-bit DACs are available and increasingly common in system design. These DACs are true precision devices with less than 1-LSB linearity error and 1-ppm/°C drift. Nonetheless, some DAC applications require even higher performance. Automatic test equipment, instruments, calibration apparatus, laser trimmers, medical electronics, and other applications often require DAC accuracy beyond 16 bits. You can find 18-bit DACs in circuit-assembly form, although they are expensive and require frequent calibration. Designs that use manually switched resistor ratios can achieve DAC resolutions of 20 and even 23 (0.1 ppm) bits or more. The most accurate resistor-based DAC of this type is Lord Kelvin's Kelvin-Varley divider, which can achieve ratio accuracies of 0.1 ppm. These devices, although amazingly accurate, are large, slow, and extremely costly. Standards laboratories are typically the only places where these types of DACs are still in use. (Part 2 discusses this type of DAC in more detail.)

Thus, a practical, 20-bit (1-ppm) DAC that is easy to construct and does not require frequent calibration is a useful development. The scheme in **Figure 1** is based on the performance of a true 1-ppm ADC with scale and zero drifts less than 0.02 ppm/°C. The DAC uses this device, the 24-bit LTC2400, as a feedback element in a digitally corrected loop to realize 20-bit performance. The ADC has an integrated oscillator, 4-ppm nonlinearity, and 0.3-ppm rms noise. It uses delta-sigma technology to provide extremely high stability.

ADCs AND DACs REVERSE ROLES

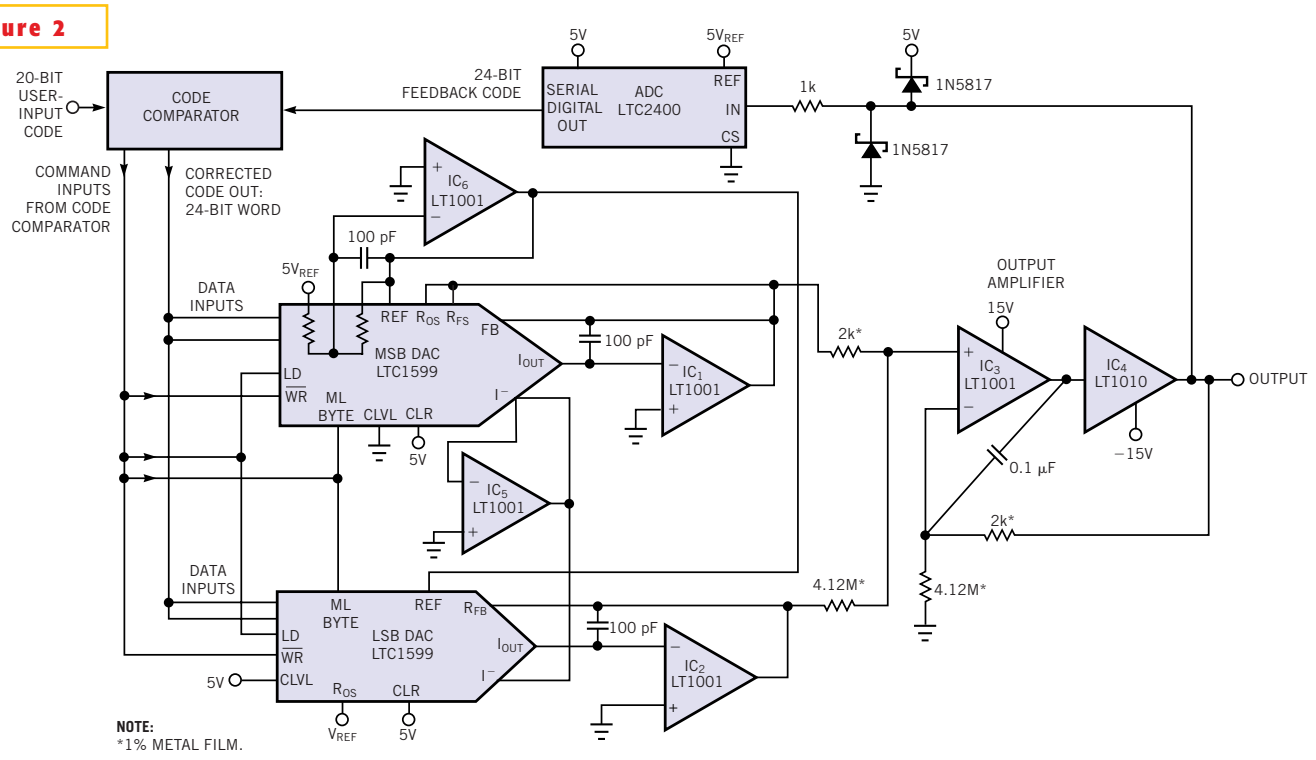
In practice, the 20-bit DAC's overall output is the "slave" of this monitoring "master" ADC, which

Figure 1



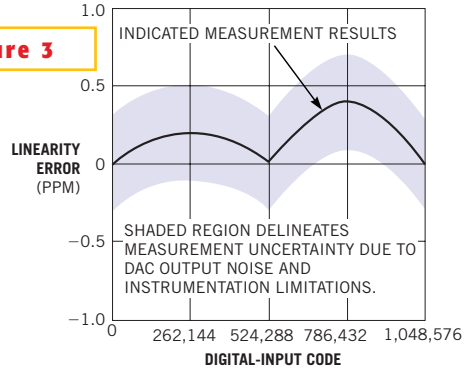
For this 20-bit DAC, digital comparison allows an ADC to correct DAC errors, and the ADC's low-uncertainty characteristics permit 1-ppm output accuracy.

Figure 2



The composite DAC comprises two DAC values summed by an output amplifier. The ADC and a digital code comparator furnish stabilizing feedback.

Figure 3



A linearity plot shows no error outside 1 ppm for all codes.

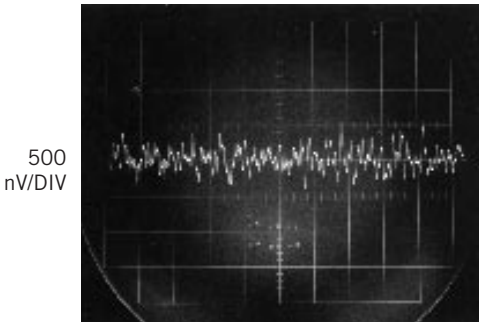


Figure 4

The output-noise measurement indicates less than 1 mV, or approximately 0.2 LSB, of noise. The measurement's noise floor, due to equipment limitations, is 0.2 µV.

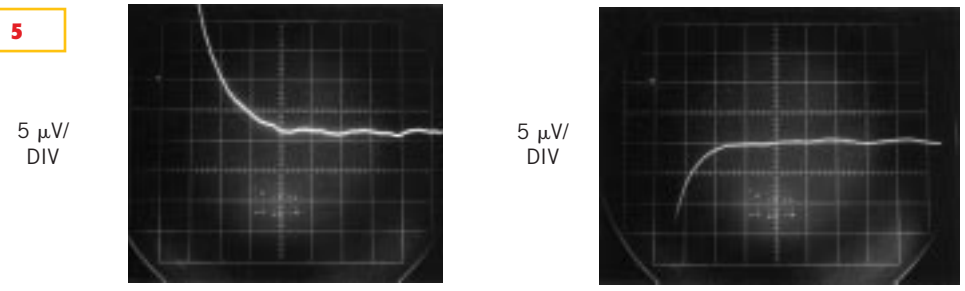
feeds digital information to a code comparator. The code comparator determines the difference between the user-input word and the master ADC's output, and it presents a corrected code to the slave DAC. In this fashion, the loop continuously corrects the slave DAC's drifts and nonlinearity to an accuracy that the ADC and V_{REF} determine.

This arrangement represents a turnabout for DACs and ADCs. For years, designers have used DACs in feedback loops to make ADCs. In this case, however, the ADC performs the role of circuit component rather than the traditional stand-alone role in which it feeds back a loop to form a DAC.

This loop has a number of desirable attributes. The ADC and its reference set accuracy limitations. The sole DAC requirement is that it must be monotonic. No other components in the loop need to be stable. Additionally, loop behavior averages low-order bit indexing and jitter, obviating the loop's inherent small-signal instability. You can use classical remote sensing or digitally based sensing by placing the ADC at the load. The ADC's SO-8 package and lack of external components make this digitally incarnated Kelvin-sensing scheme practical.

The circuit realization of the scheme in **Figure 2** has a resolution of 1 ppm, with software correction, and full-scale error drift of 0.1 ppm/°C (**Table 1**). In **Figure 3**, the circuit's linearity-versus-output-code data shows that overall linearity is within 1 ppm. Output noise, measured in

Figure 5



Settling time after a full-scale step to within 1 ppm (±5 µV) is 1400 msec (a). Small-step settling time measures 100 msec to within 1 ppm for a 500-µV transition (b).

a 0.1-to-10-Hz bandpass, is approximately 0.2 LSB (**Figure 4**). Equipment limitations, which set a noise floor of approximately 0.2 µV, somewhat corrupt this measurement. The ADC's conversion rate combines with the loop's sampled data characteristic and slow amplifiers to dictate a relatively slow DAC response. The full-scale slew response requires approximately 150 µsec. Full-scale DAC settling time to within 1 ppm (±5 µV) requires approximately 1400 msec (**Figure 5a**). A smaller step of 500 µV needs only 100 msec to settle within 1 ppm (**Figure 5b**).

Establishing and maintaining confidence in a 1-ppm linearity measurement is uncomfortably close to the state of the art. And measuring settling time is not straightforward, even at the relatively slow speeds involved in this scheme. Part 2 discusses linearity, settling time, and noise-measurement techniques in detail.

BIT OVERLAP ASSURES LOOP CAPTURE

The slave DAC actually comprises two DACs (**Figure 2**). The circuit feeds the upper 16 bits of the code comparator's output to a 16-bit DAC, the MSB DAC, while a separate DAC, the LSB DAC, converts the lower bits. Although the circuit presents a total of 32 bits to the two DACs, 8 bits of overlap assure loop capture under all conditions. The composite DACs' resultant 24-bit resolution provides 4 bits of indexing range below the 20th bit, ensuring a stable LSB of 1 ppm of scale. The 8-bit overlap assures the loop can always capture the correct output value.

IC_1 and IC_2 transform the LSB and MSB DAC output currents into voltages, and IC_3 adds the two voltages. The circuit arranges IC_3's scaling so that the correction loop can always capture and correct any combination of zero- and full-scale errors. IC_3's output, which is the circuit output, drives the ADC through IC_4, which provides buffering to drive loads and cables.

The code comparator takes the difference between the input word and the ADC's digital output and produces a corrected code. The circuit applies this corrected code to the MSB and LSB DACs, closing a feedback loop. The ADC and voltage-reference errors determine the loop's integrity. The resistor and diodes at the 5V-powered ADC protect it from inadvertent IC_4 outputs, such as power-up spikes, transients, and a lost supply. IC_6 is a reference inverter, and IC_5 provides a clean ground potential to both DACs.

The code comparator enforces the loop by setting the slave DAC inputs to the code that equalizes the user input and the ADC's output. The code comparator's digital hardware consists of three input data latches and a PIC-16C55A processor (**Figure 6**). Inputs include user data, such as the DAC inputs, curvature correction for linearity via DIP switches, a convert command (DAC $\overline{WR}$), and a selectable filter-time constant. The DAC RDY output indicates when the DAC output has settled to the user's input value. Additional outputs and an input control and monitor the analog section in **Figure 2** to effect loop closure. Comparator code by Florin Opresch drives the processor. You can download it from www.ednmag.com/ednmag/reg/2001/04122001/08ms743.htm.

TABLE 1—20-BIT DAC PERFORMANCE SPECIFICATIONS

Parameter	Specification
Resolution	1 ppm
Full-scale error	4 ppm of V_{REF} (trimmable to 1 ppm by adjusting V_{REF})
Full-scale-error drift	0.04 ppm/°C exclusive of reference (0.1 ppm/°C with LTZ1000A reference)
Offset error	0.5 ppm
Offset-error drift	0.01 ppm/°C
Nonlinearity	±2 ppm, trimmable to less than 1 ppm
Output noise	0.2 ppm (~0.9 µV, 0.1-to-10-Hz bandwidth)
Slew rate	0.033V/µsec
Settling-time, full-scale step	1400 msec (see note)
Settling-time, 500-µV step	100 msec (see note)
Output-voltage range	0 to 5V, with other ranges possible

Note:
Settling-time measurement is from onset of DAC movement. An additional and unpredictable time, due to processor and ADC delays, can add approximately 10 to 200 msec.

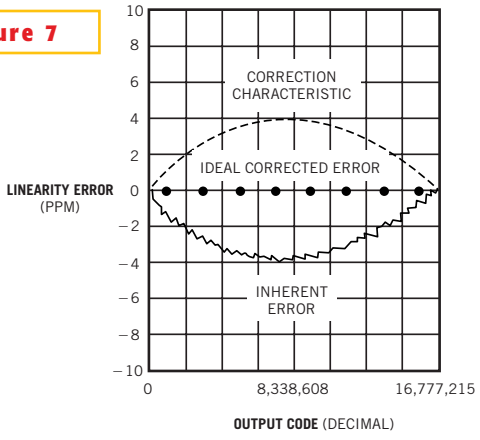
ADC SETS THE LINEARITY

The ADC's linearity determines overall DAC linearity. The LTC2400 ADC has approximately ±2 ppm nonlinearity. In applications for which this error is permissible, you can ignore this error. **Figure 7**'s lower curve shows the ADC's inherent nonlinearity, along with the first-order correction you need (upper curve) to get nonlinearity inside 1-ppm (center curve). If you need true 1-ppm performance, as in **Fig-**

ure 3, you can use software-based correction, which is part of the previously mentioned comparator code. The software generates the desired "inverted bowl" correction characteristic. You can set the correction to complement the residual nonlinearity characteristics of any individual LTC2400 using DIP switches at the code comparator.

The LTC2410 offers another approach to improved linearity. This LTC2400 variant has improved linearity but specifies a maximum input range of 2.5V. **Figure 8a** divides the DAC output with a precision-resistor ratio set, which allows you to use the LTC2410 while maintaining the 5V full-scale output. The disadvantage of this approach is the ratio set's additional 0.1-ppm/°C and 5-ppm/year error contribution. **Figure 8b** is similar to **Figure 8a**, although the ratio set's new value in **Figure 8b** permits a 10V full-scale output.

Figure 7

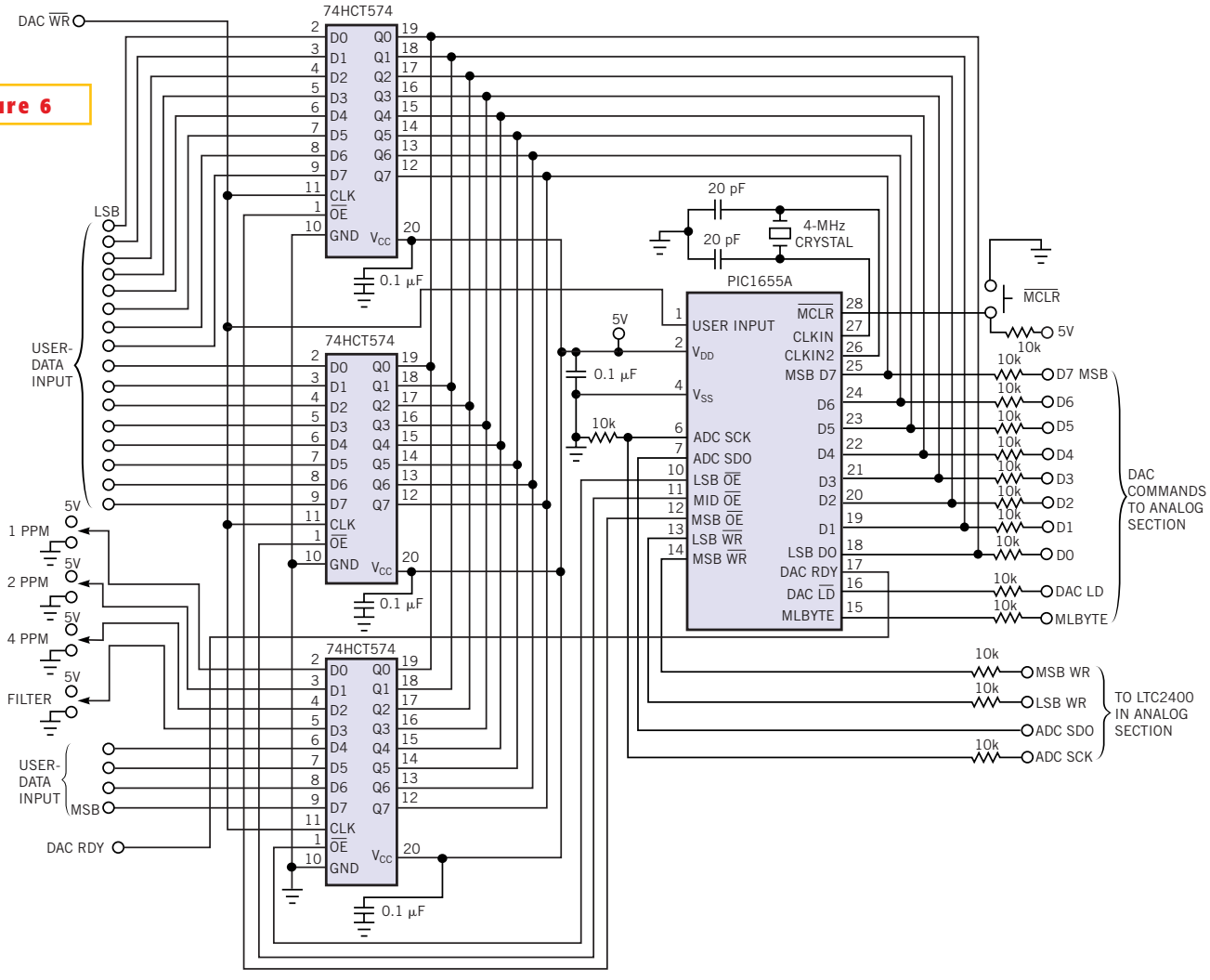


The LTC2400 ADC has inherent residual linearity error. If you apply a correction characteristic, you can achieve a corrected linearity error of less than 1 ppm.

MODIFYING THE OUTPUT RANGE

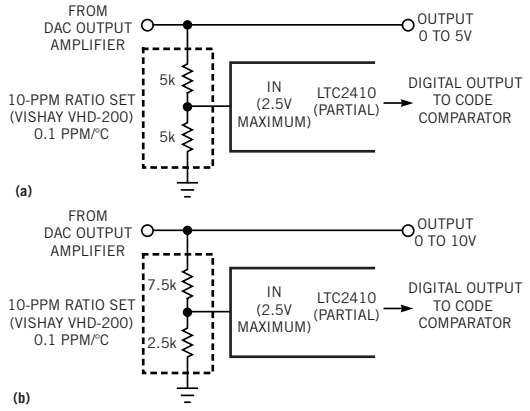
Some applications may require outputs other than the text circuit's 0-to-5V range. The simplest variation is a bipolar output (**Figure 9**). This circuit, a summing inverter, subtracts the DAC output from a reference to obtain a bipolar output. You can vary resistor and reference values to obtain different output excursions. The LT1010 output buffer provides drive capability, and the

Figure 6



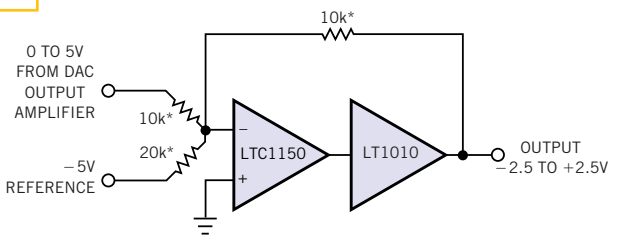
The code comparator uses three data latches and a PIC-16C55A processor to enforce the loop.

Figure 8



A precision-resistor ratio set divides the DAC's output, permitting higher inherent linearity with the LTC2410 ADC (a). A 3-to-1 ratio set permits a 10V output while accommodating the LTC2410 ADC's 2.5V input (b).

Figure 9



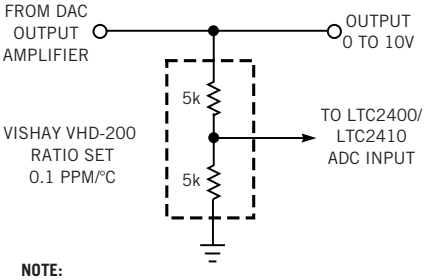
Precision resistors and a chopper-stabilized output amplifier allow a bipolar DAC output, with additional resistor-based error.

chopper-stabilized amplifier maintains 0.05-μV/°C stability. The resistors introduce a 0.3-ppm/°C error contribution.

Another approach for achieving voltage gain divides the DAC output before feedback to the ADC (**Figure 10**). In this case, the 1-to-1 divider ratio sets a 10V output, assuming an ADC reference of 5V. As in **Figure 9**, the resistors add a slight temperature error of approximately 0.1 ppm/°C for the specified ratio set.

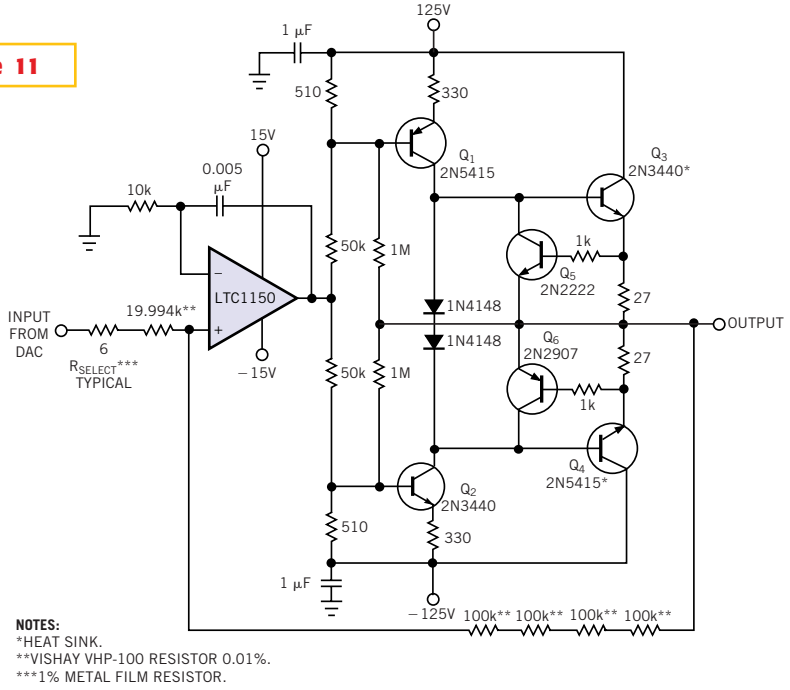
Figure 11 uses active devices for voltage outputs as high as ±100V. A chopper-stabilized amplifier drives the discrete high-voltage stage in a closed-loop fashion. Q_1 and Q_2 furnish voltage gain and feed the Q_3 and Q_4 emitter-follower outputs. Q_5 and Q_6 set the current limit at 25 mA by diverting the output drive when voltages across the 27Ω shunt resistors become too high. The local 1-MΩ/50-kΩ feedback pairs set stage gain at 20, allowing the drive from the LTC1150 to cause a full ±120V output swing. The local feedback reduces stage gain-bandwidth, easing dynamic control. Frequency compensation for this stage is relatively simple because only Q_1 and Q_2 contribute voltage gain. Additionally, the high-voltage transistors have large junctions, which result in low f_Ts, and special high-frequency roll-off precautions are unnecessary. Because the stage inverts the input, feedback returns to the amplifier's positive input. Frequency compensation consists of rolling off the amplifier with the local 0.005-μF/10-kΩ pair. Using four individual resistors minimizes heating and voltage-coefficient errors in the

Figure 10



A feedback divider at the ADC provides for a voltage gain of 2 but also results in a slight increase in the overall temperature coefficient.

Figure 11



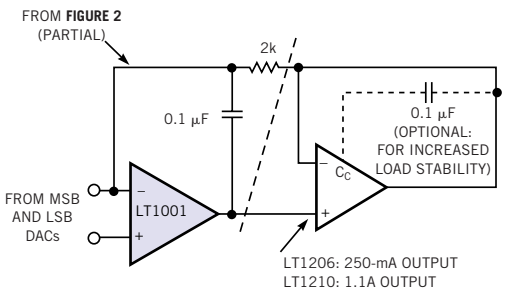
NOTES:
*HEAT SINK.
**VISHAY VHP-100 RESISTOR 0.01%.
***1% METAL FILM RESISTOR.

A high-voltage output stage delivers ±100V at 25 mA, and multiple feedback resistors minimize dissipation and voltage-coefficient effects.

feedback term. Trimming involves selecting the indicated resistor for an exactly 100.0000V output with the DAC at full scale.

A fourth approach increases output-current capability with a current-gain stage inside the DAC output amplifier's feedback loop (**Figure 12**). This stage replaces buffer IC_4 in **Figure 2**. Two options that differ in output capacity are possible. Note that as output current rises, wiring resistance becomes a potentially large error term. For example, at an output of only 10 mA, a wiring resistance of 0.001Ω introduces a 10-µV drop, which is a 2-ppm error. Because of this wiring-resistance-induced error, the circuit should supply heavy loads using short, highly conductive paths and use remote sensing.

Figure 12



Two output stages supply 250-mA and 1.1A loads, respectively. Remote sensing is usually necessary to compensate for IR drops.

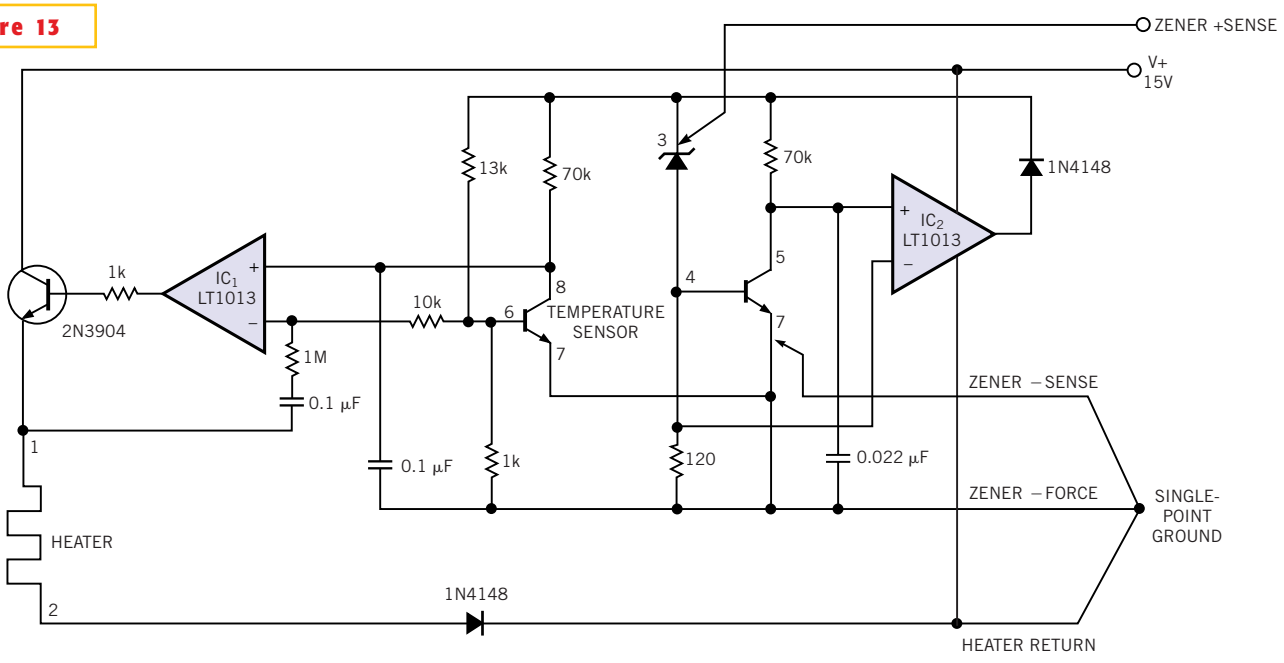
CHOOSE A VOLTAGE REFERENCE

The $5V_{REF}$ input to the ADC in **Figure 2** requires some attention. You can use self-contained references, which are convenient and easy to apply. Some references, such as the LM199A and the LTZ1000A, require external circuitry but offer high performance. In general, select a reference that offers the lowest time and temperature drifts. Regardless of the reference you choose, you must trim the reference to establish absolute DAC accuracy.

A circuit built around the LTZ1000A offers high stability (**Figure 13**). IC_1 senses the LTZ1000A die temperature and accordingly controls the IC heater via the 2N3904. IC_2 controls reference current. Kelvin connections sense the Zener reference level, minimizing voltage-drop effects. A single-point ground eliminates return-current mixing and the attendant errors that this mixing produces.

Other choices for reference buffering employ chopper-stabilized amplifiers augmented with buffer-output stages (**Figure 14**). Buffer error is extremely low. **Figure 14a** shows a simple unity-gain stage that transmits the input to the output with low error and minimal reference loading. **Figure 14b** takes moderate gain, allowing a 7V-reference input to produce 10V at the output. **Figure 14c** offers two ways to get 5V from the nominal 7V input. A precision divider lightly loads the reference in one case. In the optional case, the circuit avoids loading the reference by placing the divider at the

Figure 13



NOTES:
R_1 THROUGH R_5: VISHAY VHP-100 0.1%.
HEATER, UNLABELED ⊣⊢ AND ZENER=LTZ1000A.
PIN NUMBERS APPEAR FOR INDIVIDUAL LTZ1000A ELEMENTS.

A 7V reference includes a heater-control amplifier (IC_1), a Zener current regulator (IC_2), and a Zener diode. Note the Zener's Kelvin connections and single-point ground.

output and driving the ADC's reference input from the divider output.□

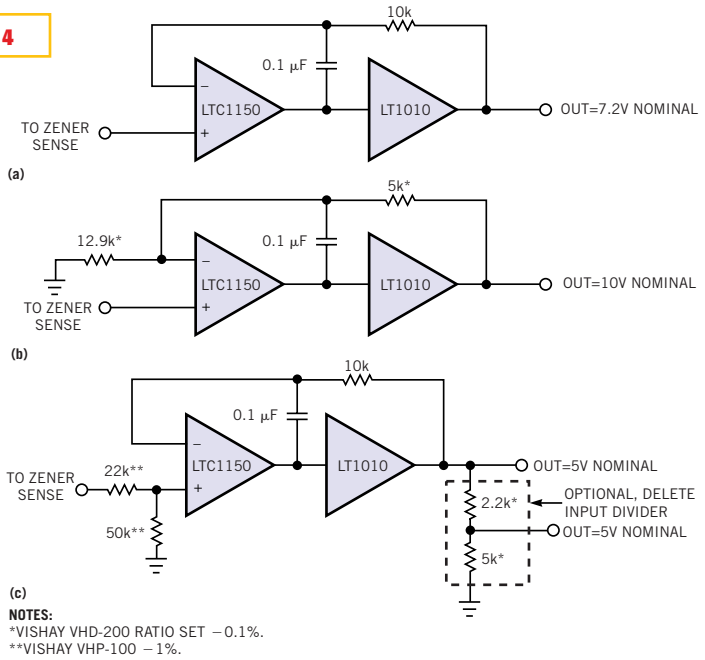
Author's biography

Jim Williams is a staff scientist at Linear Technology Corp (Milpitas, CA, www.linear-tech.com), where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA), where he first encountered serious 1-ppm measurement using the Kelvin-Varley divider. A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

Acknowledgments

Thanks to Patrick Copley, Jim Brubaker, Florin Opresch, Josh Guerrero, and VJ Sun for their contributions.

Figure 14



Chopper-stabilized reference-buffer options include unity gain (a), 10V output (b), and 5V output (c). Trimming is necessary for absolute accuracy.

PART 2 OF THIS SERIES ON THE DESIGN OF A 20-BIT DAC DISCUSSES THE ALL-IMPORTANT TECHNIQUES FOR TESTING THE PERFORMANCE–LINEARITY, SETTLING TIME, AND NOISE–AT SUCH MINUSCULE DATA LEVELS. SEE PART 3 IN THE NEXT ISSUE.

Measurement techniques help hit the 1-ppm mark

A TRUE 20-BIT DAC that fits on a circuit board and costs approximately $100 to build is a design milestone (see *EDN*, April 12, 2000, pg 95 or www.ednmag.com/ednmag/reg/2001/04122001/08ms743.htm). Claiming to achieve this level of performance is one thing, but proving it with precise measurements is another. The measurement techniques are at times more exacting than the actual circuit's design. Part 2 of this series presents approaches and circuits for measuring linearity, settling time, and noise.

MEASURE LINEARITY TO 1 PPM

Of these three measurements, determining the DAC's linearity requires the greatest effort. Verifying 1-ppm linearity of the DAC and the integral ADC requires special considerations, and, interestingly, some help from the 19th century. Testing necessitates some form of voltage source that produces equal-amplitude output steps for incremental digital inputs. Additionally, for measurement confidence, it is desirable that the source be substantially more linear than the 1-ppm requirement. This demand is stringent and painfully close to the state of the art.

The most linear "digital-to-analog" converter is also one of the oldest. Lord Kelvin's KVD (Kelvin-Varley divider) is, in its most developed form, linear to 0.1 ppm. This manually switched device features 10 million individual dial settings arranged in seven decades. You can think of the device as a three-terminal potentiometer with fixed "end-to-end" resistance and a seven-decade switched wiper position (**Figure 1a**).

The actual construction of a 0.1-ppm KVD is

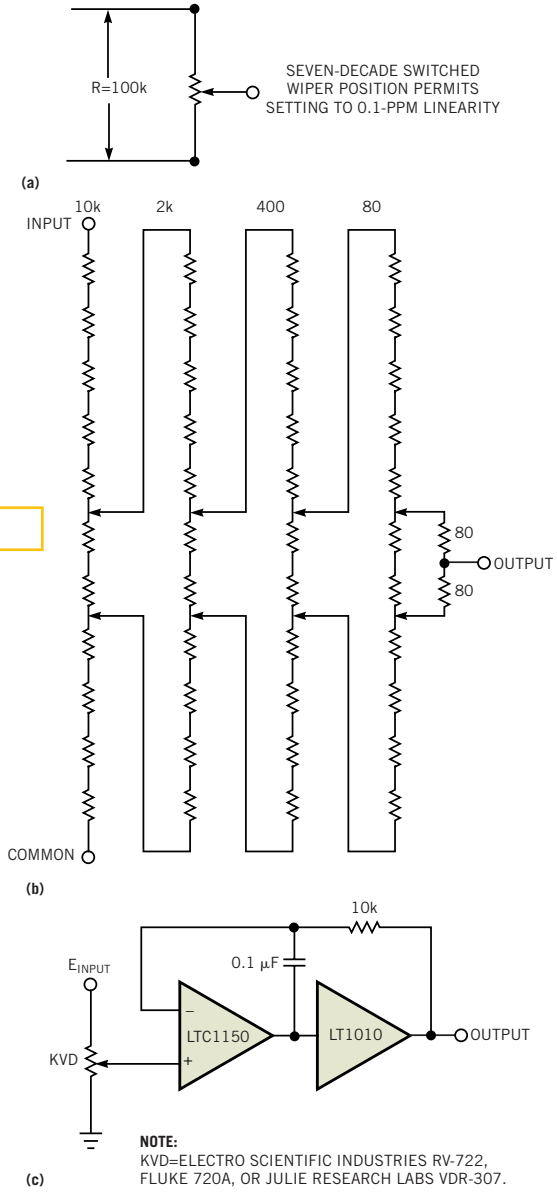


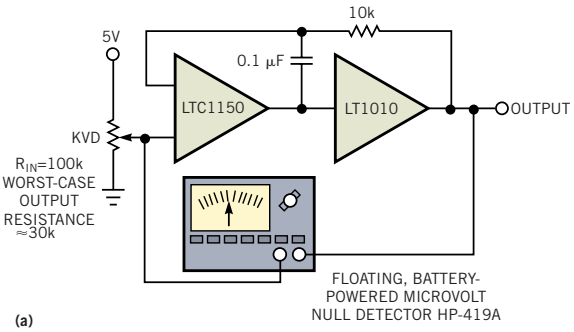
Figure 1

A conceptual KVD is a three-terminal potentiometer with a seven-decade switched wiper position (a). You can expand this four-decade KVD by continuing the divide-by-5 chains (b). Adding an output buffer to the KVD gives output-drive capability (c).

NOTE:
KVD=ELECTRO SCIENTIFIC INDUSTRIES RV-722, FLUKE 720A, OR JULIE RESEARCH LABS VDR-307.

more artistry and witchcraft than science. The market is relatively small, the vendors few, and the resultant price high. If $13,000 for a bunch of switches and resistors seems offensive, try building and certifying your own KVD. The KVD in **Figure 1b** has a 100-kΩ input impedance. Thus, wiper's output resistance is high and varies with setting. As such, a very low bias-current follower is necessary to unload the KVD without introducing significant error (**Figure 1c**). The LT1010 output buffer allows for driving cables and loads and, more subtly, maintains the amplifier's high open-loop gain.

The schematic in **Figure 1c** is deceptively simple. In practice, construction details are crucial. Parasitic thermocouples, or namely the Seebeck effect; layout; grounding; shielding; guarding; cable choice; and other issues affect achievable performance. Part 3 discusses these issues in detail. In fact, as good as the chopper-stabilized LTC1150 is with respect to drift, offset, bias current, and CMRR (common-mode rejection ratio), selection is necessary if you seek sub-ppm nonlinearity performance. An error-budget analysis details some of the selection criteria (**Figure 2**). You can test the buffer with **Figure 2a**'s circuit. As you run the KVD through its entire range, the floating null detector must remain well within 1 ppm, or 5 μV, and preferably at less than 0.5 ppm. This test ensures that you account for all error sources, particularly I_B and CMRR, whose effects vary with operating point. Measured performance indicates that the sum of all errors called out in **Figure 2b** are well within desired limits.



(a)

ERROR SOURCE	WORST-CASE SPEC	REALISTIC SELECTION TARGET	ERROR IN PPM
E_{OS}	5 μV	0.5 μV	0.1
$E_{OS\Delta T}$	0.05 μV/°C	0.05 μV/°C	0.01/°C
I_B	50 pA	10 pA	0.1
CMRR	110 dB	140 dB	0.1
FINITE GAIN	140 dB	140 dB	0.1

(b)

Figure 2

You can determine buffer error by measuring the I/O deviation with a floating microvolt null detector. This technique permits evaluation of fixed and operating-point-induced errors (a). An error-budget analysis for the KVD buffer details the selection criteria (b).

CIRCUIT CONSTRUCTION IS CRITICAL

The detailed schematic of the sub-ppm-linearity voltage source includes offset trim, a stable voltage source, and a second KVD to drive the main KVD (**Figure 3**). Additionally, an ensemble of three HP3458A voltmeters monitors the output. The offset trim bleeds a small current into the main KVD ground return, producing a few microvolts of offset-trim range. This range allows you to functionally trim out all sources of zero error, such as amplifier offsets and parasitic thermocouple mismatches, permitting a true zero-volt output when the main KVD setting is all zeros. Three voltmeters, which have a specification of less than 0.1-ppm nonlinearity on the 10V range, "vote" on the source's output. In other words, each voltmeter monitors the source's output. Then, you correct each reading for absolute error and average the three corrected readings to obtain the apparent linearity.

The single-point-grounding scheme prevents the mixing of return currents and the attendant errors. The shielded cables for connecting the KVDs and voltmeters should have low-thermal-activity specifications. Keithley type SC-93 and Guildline #SCW are suitable. Crush-type copper lugs, as opposed to soldered types, provide lower parasitic-thermocouple activity at KVD and DVM connection points. However, you must keep the lugs clean to prevent oxidation, thus avoiding excessive thermal voltages (see Part 3). A copper deoxidant (Caig

TABLE 1–HIGH-SENSITIVITY, LOW-NOISE AMPLIFIERS

Instrument type	Manufacturer	Model number	Maximum bandwidth	Sensitivity or Gain	Availability	Comments
Differential amplifier	Tektronix	1A7/1A7A	500 kHz/1 MHz	10 μV/DIV	Secondary market	Requires 500 series mainframe, settable bandstops
Differential amplifier	Tektronix	7A22	1 MHz	10 μV/DIV	Secondary market	Requires 7000 series mainframe, settable bandstops
Differential amplifier	Tektronix	5A22	1 MHz	10 μV/DIV	Secondary market	Requires 5000 series mainframe, settable bandstops
Differential amplifier	Tektronix	ADA-400A	1 MHz	10 μV/DIV	Current production	Stand-alone with optional power supply, settable bandstops
Differential amplifier	Tektronix	AM-502	1 MHz	Gain=100,000	Secondary market	Stand-alone with optional power supply, settable bandstops
Differential amplifier	Preamble	1822	10 MHz	Gain=1000	Current production	Stand-alone, settable bandstops
Differential amplifier	Stanford Research Systems	SR-560	1 MHz	Gain=50,000	Current production	Stand-alone, settable bandstops, battery or line operation

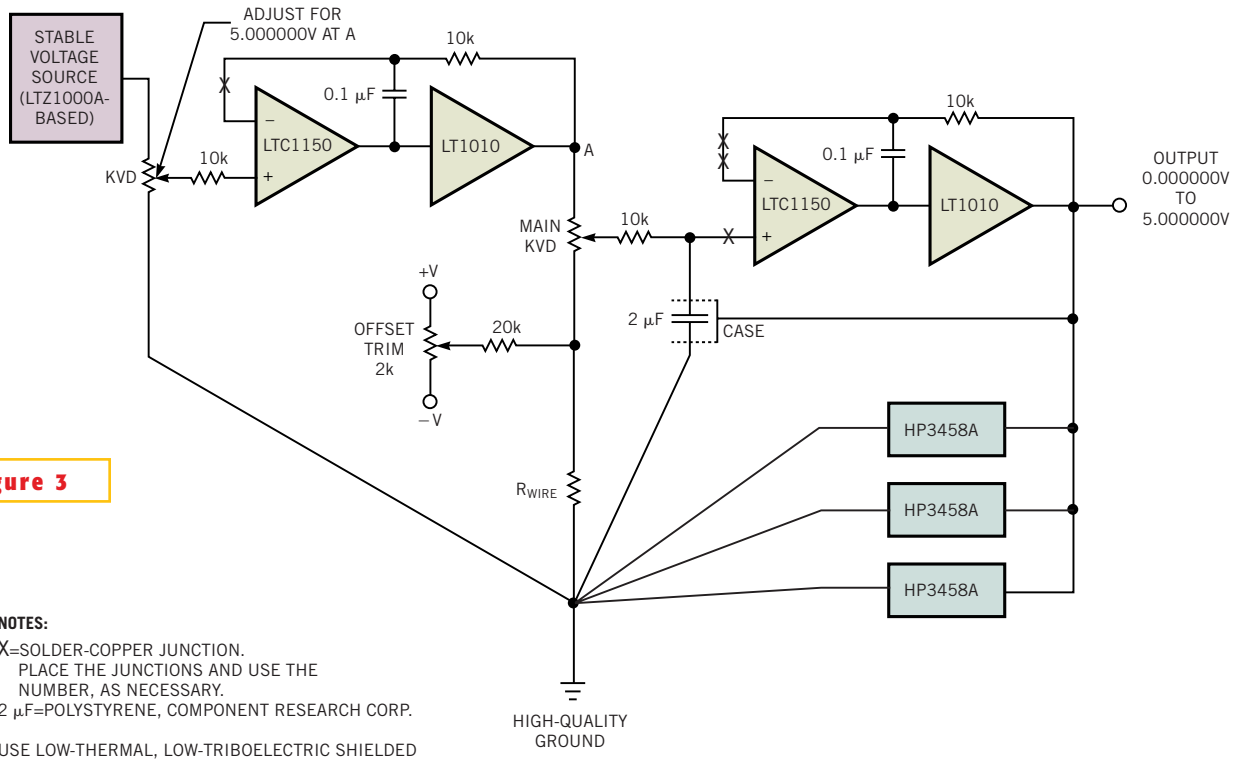


Figure 3

NOTES:

X=SOLDER-COPPER JUNCTION.
PLACE THE JUNCTIONS AND USE THE NUMBER, AS NECESSARY.
2 µF=POLYSTYRENE, COMPONENT RESEARCH CORP.

USE LOW-THERMAL, LOW-TRIBOELECTRIC SHIELDED CABLE FOR KVD AND DIGITAL-VOLTMETER CONNECTIONS.

The complete sub-ppm-linearity voltage source includes offset trim, a stable voltage source, and a second KVD to drive the main KVD.

Labs "Deoxit" D100L) is effective for maintaining such cleanliness. Low thermal lugs and jacks, preterminated to cables, are also available (Hewlett-Packard 11053, 11174A) and convenient.

Thermal baffles that enclose the KVD and DVM connections tend to thermally equilibrate their associated banana-jack terminals, minimizing residual parasitic-thermocouple activity. Additionally, you should restrict the number of connections in the signal path. You also need to balance electrical connections in the signal path against each other such that the net signal-path degradation due to thermocouples is nominally equal to zero. When you introduce a deliberate thermocouple, be sure to match materials. Complying with this guideline may necessitate a deliberate introduction of solder-copper junctions, marked "X" on **Figure 3**, to obtain optimum differential cancellation (see Part 3). Simply breaking the appropriate wire or pc trace and soldering it facilitates this cancellation. Ensure that the introduced thermocouples temperature-track the junctions they are supposed to cancel. You can usually ensure temperature

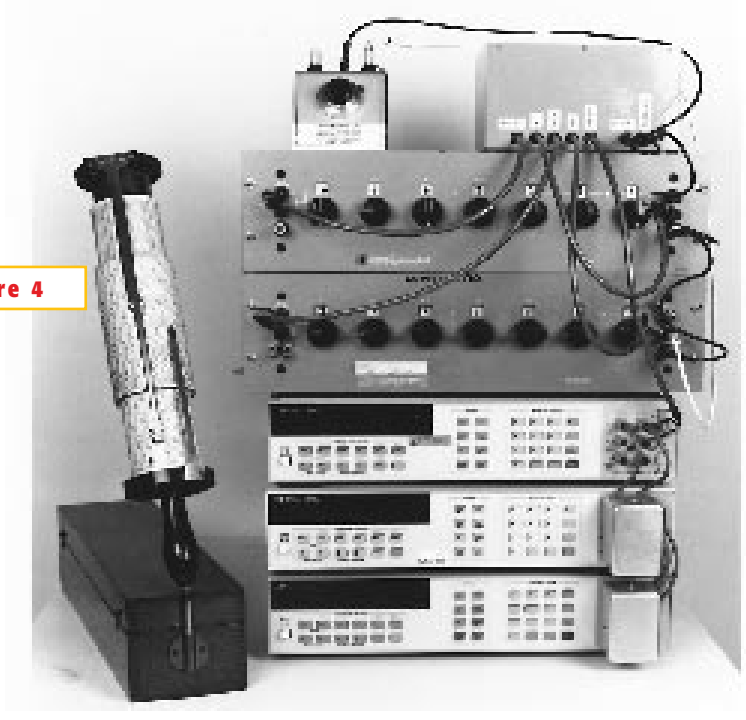


Figure 4

In the sub-ppm-linearity voltage source, the LTZ1000A-based reference and buffers are at the upper right. Offset trim is at the upper left, and reference and main KVDs are at the upper center and center middle, respectively. Three HP3458 DVMs at the bottom monitor output. The computer in the left foreground aids linearity calculations.

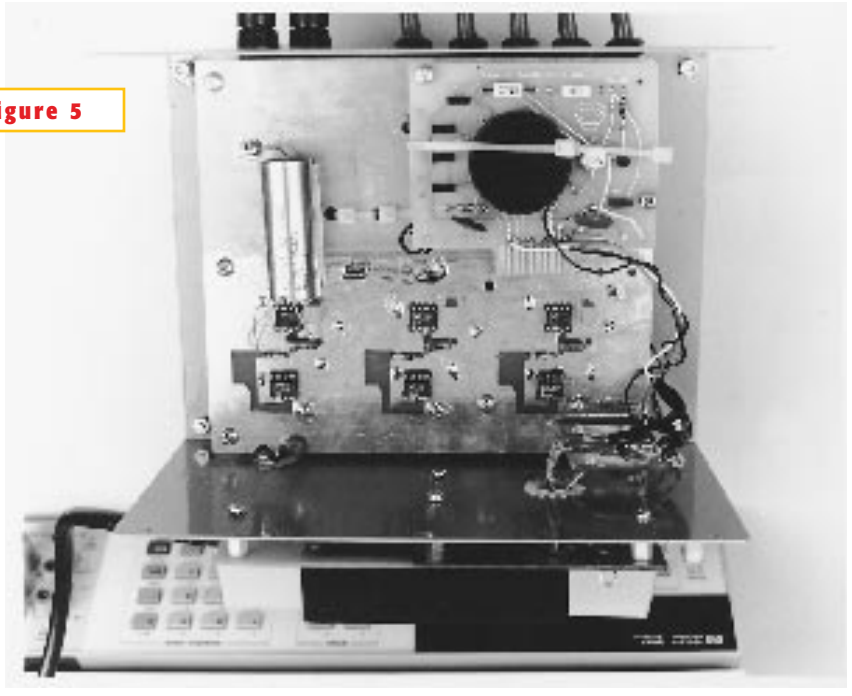
tracking by locating all junctions close to each other.

The noise-filtering capacitor at the main KVD is a low-leakage type; the output buffer drives the capacitor's metal to guard against surface leakage.

When studying this measurement approach, it is essential to differentiate between linearity and absolute accuracy. This differentiation eliminates concerns with absolute standards, permitting certain freedoms in the measurement scheme. In particular, although **Figure 3** uses single-point grounding, the circuit does not use remote sensing. This choice is deliberate, made to minimize the number of potential error-causing parasitic thermocouples in the signal path. Similarly, the design does not use a ratiometric reference connection between the KVD LTZ1000A voltage source and the voltmeters for the same reason. In theory, a ratiometric connection affords lower drift. In practice, the resultant introduced parasitic thermocouples obviate the desired advantage. Additionally, the aggregate stability of the LTZ1000A reference and the voltmeter references (also, incidentally, LTZ1000A based) is comfortably inside 0.1 ppm for periods of 10 minutes, which is more than enough time for a 10-point linearity measurement.

Figures 4 and **5** are photographs of the voltage source and the reference-buffer-box internal construction. This KVD-based, high-linearity voltage source has been in use for years. The measurement regime involves three steps:

Figure 5

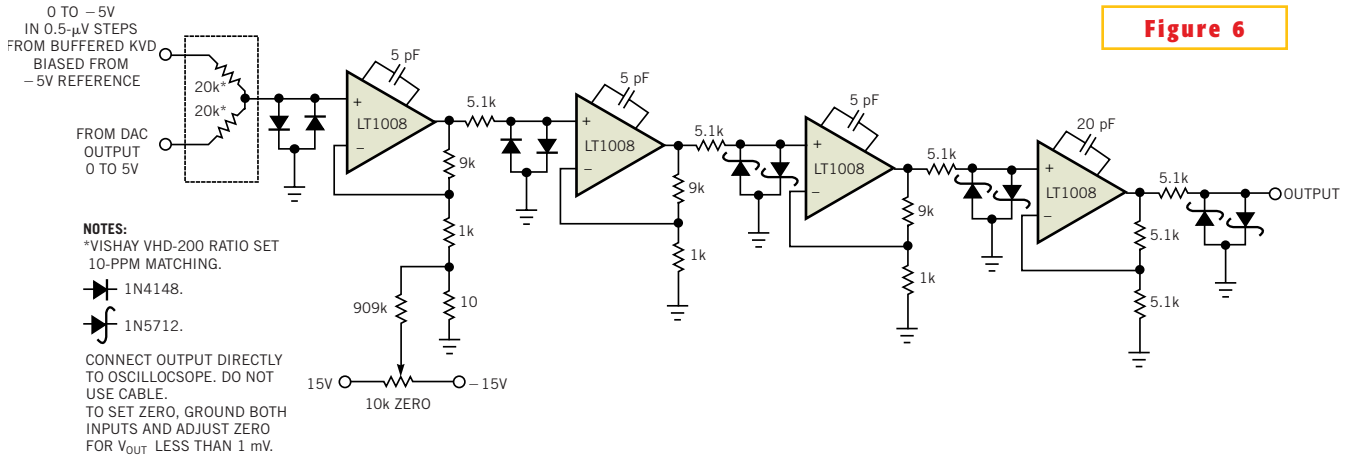


In the reference-buffer box, the LTZ1000A reference circuitry is at the lower left, buffer amplifiers are in the center, the capacitor-case bootstrap connection is center-right, and single-point-ground "mecca" is at the upper left. The power supply at the top mounts outside of the box, minimizing magnetic-field disturbances.

- verifying KVD linearity by intercomparison with other KVDs and by an independent calibration laboratory,
- taking worst-case voltmeter ensemble deviations over 0 to 5V every 0.5V, and
- performing 100 runs (10 per day, once per hour).

During this period, the total linearity uncertainty defined by the source and its monitoring voltmeters is just 0.3 ppm. This value is more than three times better than the desired 1-ppm performance, promoting confidence in your measurements. A delightful activity, particularly for those wholly unenthralled with Web surfing, is to spend hours "surfing the Kelvin." This activity consists of dialing various KVD settings and noting ADC

Figure 6

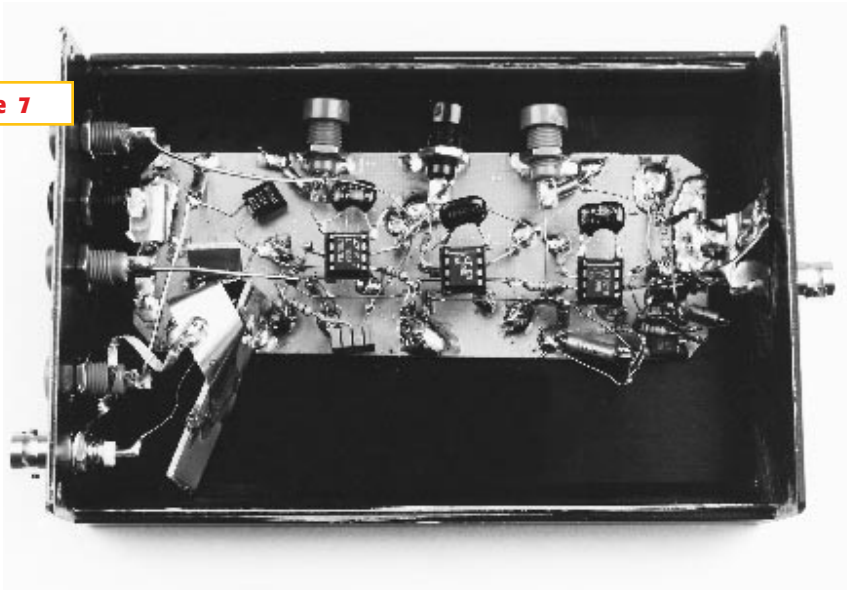


A clamped, distributed gain-of-2000 amplifier permits DAC settling-time measurements without saturation effects.

agreement within 1 ppm. This astonishingly nerdy behavior thrills certain types.

MEASURING DAC SETTLING TIME

Figure 7



The settling-time amplifier's bandwidth is only 10 kHz, but its high gain of 2000 necessitates careful layout to avoid parasitic-feedback-induced oscillation. The input at lower left is fully shielded to prevent radiative feedthrough to amplifier, and the enclosure shields the circuit from stray RF and pickup.

Measuring the 20-bit DAC's output settling time is a challenging task. Although the time scale involved is relatively slow, the LSB step size of 5-μV presents problems. The issue reduces to obtaining a great deal of gain without inducing overdrive in the monitoring oscilloscope. Such overdrive will corrupt the measurement, rendering displayed results meaningless.

The input structure of **Figure 6** resistively balances the DAC output against the precision variable reference supply, such as in **Figure 3**, which is adjustable in 0.5-μV steps. The circuit's remainder constitutes a clamped, distributed gain-of-2000 amplifier. Diode clamping at each gain-stage input prevents saturation from occurring even with large DAC-reference supply imbalances. The distributed gain allows a 10-kHz bandwidth while maintaining clamping effectiveness. The monitoring oscilloscope, operating at 5 or 10 mV/DIV (5 to 10 μV at the DAC output) can readily discern 5-μV settling without incurring deleterious overdrive.

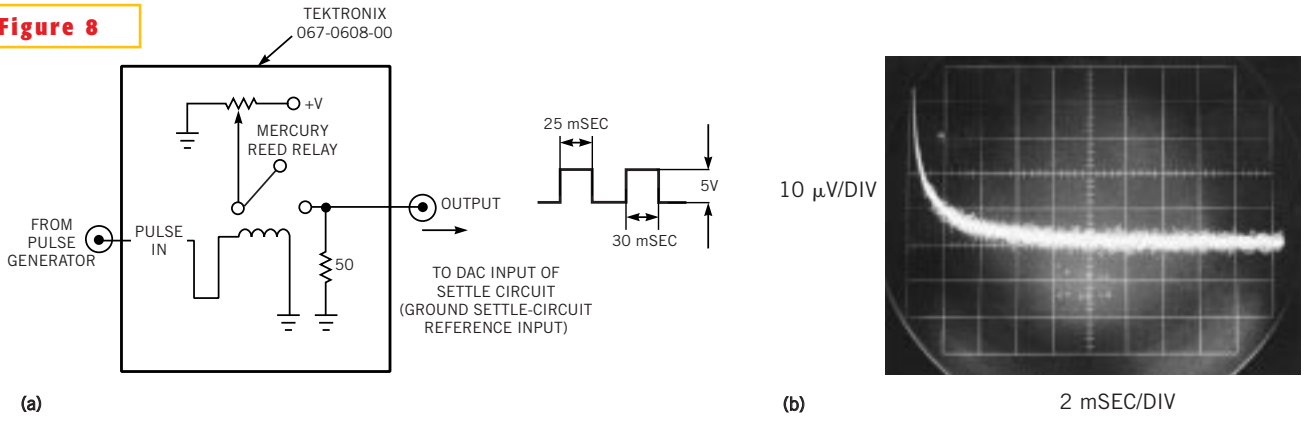
Layout and construction of this circuit requires care. A linear layout minimizes parasitic feedback paths, preventing oscillation (**Figure 7**). The construction fully shields the DAC input-step signal, preventing feedthrough to various sensitive points within the amplifier. Finally, the entire circuit sits in a shielded enclosure to minimize effects of stray RF and pickup.

You can test the settling-time test circuit by applying a test step that settles much faster than the DAC. One method is to use a mercury-wetted reed-relay-based pulse generator to supply the step (**Figure 8a**). The mercury-wetted reed relay opens in 5 nsec, and the when the relay opens, the circuit's output settles essentially instantaneously relative to DAC speed and settling-time-amplifier bandwidth. The relay in **Figure 8a** is commercially available, but you can obtain similar results with standard mercury-based reed relays. You test **Figure 6**'s response by grounding one input and driving the other input with **Figure 8a**'s pulse generator. The test circuit settles to within 1 ppm (±5 μV) in 2 msec (**Figure 8b**). This time is much faster than the DAC's settling time, lending confidence to the settling-time results of Part 1.

MEASURING MICROVOLT NOISE LEVELS

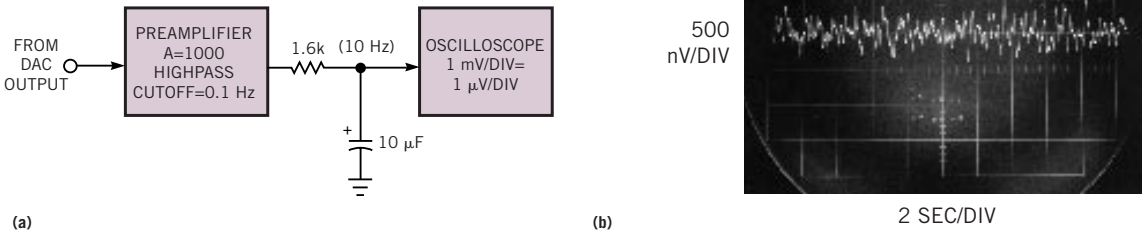
Verifying DAC output noise requires a quiet, high-gain amplifier at the oscilloscope. **Figure 9a** shows one way to take

Figure 8



A mercury wetted reed-relay-based pulser supplies a clean step to test the settling-time circuit (a), which responds to the test step with 2-msec settling to ±1ppm (±5 μV) (b).

Figure 9



A microvolt noise measurement necessitates a high-gain preamplifier for the oscilloscope (a). DAC output noise in a 0.1-to-10-Hz measurement bandpass, set by the preamplifier and discrete filter, is less than 1 mV, or approximately 0.2 LSB (b). Equipment limitations set the measurement noise floor at 0.2 µV.

the measurement. The input preamplifier, operating at a gain of 1000, has a highpass cutoff at 0.1 Hz and drives the oscilloscope via a 10-Hz discrete lowpass filter. The oscilloscope, set to 1 mV/DIV, indicates 1 µV/DIV referred to the preamplifier input. **Figure 9b** indicates that the DAC output noise is well below an LSB, about 0.9 µV. Equipment limitations set the measurement noise floor at 0.2 µV. These signal levels dictate a completely shielded, coaxial path from breadboard to oscilloscope (**Figure 10**).

Table 1 lists some applicable high-sensitivity amplifiers suitable for the noise measurement. Current-generation oscilloscopes rarely have sensitivities greater than 2 mV/DIV, although older instruments offer more capability. The **table** lists representative preamplifiers and oscilloscope plug-ins suitable for noise measurement. These units feature wideband, low-noise performance. It is particularly significant that many of these instruments are no longer in production. This fact is in keeping with current instrumentation trends, which emphasize digital-signal acquisition as opposed to analog-measurement capability.

The monitoring oscilloscope should have exceptional trace clarity. In the latter, high-quality analog oscilloscopes are unmatched. The exceptionally small spot size of these instruments suits low-level noise measurement. Tektronix types 453, 453A, 454, 454A, 547, and 556 are excellent choices. Their pristine trace presentation is ideal for discerning small signals of interest against a noise-floor-limited background. The digitizing uncertainties and raster-scan limitations of DSOs impose display-resolution penalties. Many DSO displays will not even register the fine structure of the noise waveform.□

Author's biography

Jim Williams is a staff scientist at Linear Technology Corp (Milpitas, CA, www.linear-tech.com), where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA) where he first encountered serious 1-ppm measurement using the KVD. A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

Acknowledgments

I am indebted to Lord Kelvin and to Warren Little of the CS Draper Laboratory (née Massachusetts Institute of Technology Instrumentation Laboratory) standards lab. Warren taught me, with great patience, the wonders of KVDs some 30 years ago, and I am still trading on his efforts.

Figure 10

The noise-measurement test setup includes a shielded DAC breadboard (foreground), a preamplifier (left), and a lowpass filter attached to the oscilloscope (center). The measurement path is fully coaxial.

UNDESIRABLE AND UNINTENDED THERMOCOUPLES ARE THE PRIMARY SOURCES OF ERROR IN LOW-DRIFT CIRCUITS. ATTENTION TO LAYOUT AND OTHER CONSTRUCTION DETAILS IS THE ONLY WAY TO TACKLE THE PROBLEM.

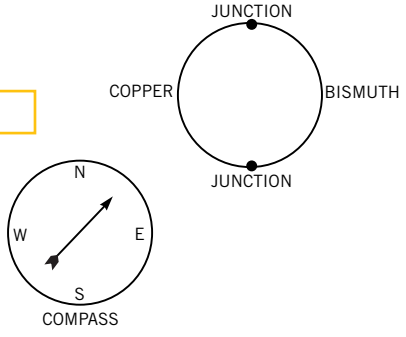
Minimizing thermocouples maintains 20-bit DAC precision

Subtle parasitics can have pronounced and seemingly inexplicable effects on the performance of low-level circuits, and a 1-ppm DAC is certainly in this category. Part 1 of this three-part series discussed the circuit design of a 20-bit DAC with 0.1 ppm/°C of drift, and part 2 discussed the measurement techniques (**references 1** and **2**). This third and final part discusses how you deal with cables, connections, solder, component choice, terror, and circuit arcana.

Perhaps the most prevalent detractors to microvolt-level circuitry are unintended thermocouples. (**Reference 2** also includes considerable discussion on dealing with thermocouples.) In 1822, Thomas Seebeck, an Estonian physician, accidentally joined semicircular pieces of bismuth and copper while studying thermal effects on galvanic arrangements (**Figure 1**). A nearby compass indicated a magnetic disturbance. Seebeck experimented repeatedly with different metal combinations at various temperatures, noting relative magnetic-field strengths. Curiously, he did not believe that electric current was flowing and preferred to describe the effect as "thermomagnetism." He published his results in a paper (**Reference 1**). Subsequent investigation showed the "Seebeck effect" to be fundamentally electrical in nature, repeatable, and quite useful. Thermocouples, by far the most common transducers, are Seebeck's descendants. Unfortunately, unintended and unwanted thermocouples are also Seebeck's progeny.

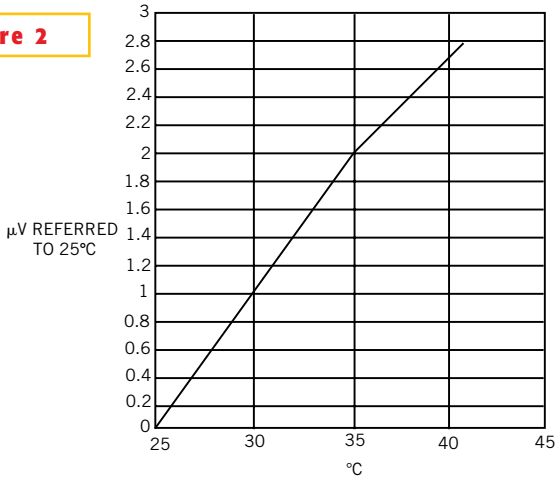
In low-drift circuits, unwanted thermocouples are probably the primary source of error. Connectors, switches, relay contacts, sockets, wire, and even solder are all candidates for thermal-EMF (electromagnetic-field) generation. It is relatively clear that connectors and sockets can form thermal junctions. However, it is not at all obvious that junctions of copper wire from different manufacturers can easily gen-

Figure 1



Joining pieces of bismuth and copper led Thomas Seebeck to his accidental discovery of what he called "thermomagnetism" and what we now call the Seebeck effect.

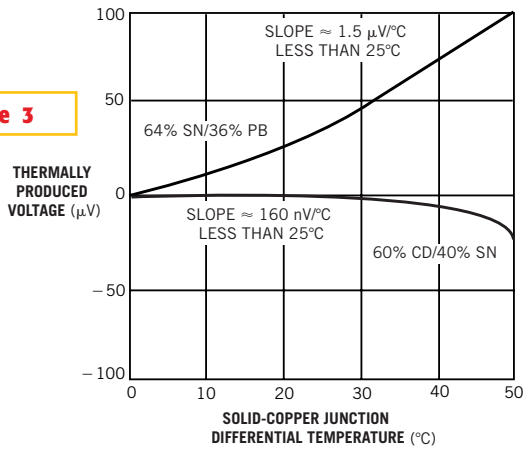
Figure 2



Two supposedly identical copper wires generate thermal EMFs due to oxidation and impurities.

erate drifts of 200 nV/°C, which is four times a precision amplifier's drift specification (**Figure 2**). Even solder can become an error term at low levels, creating a junction with copper, Kovar wires, or pc-board traces (**Figure 3**).

Figure 3



NOTE: SOURCE IS NEW ELECTRONICS 2/6/77.

Solder-copper junctions can create thermal EMFs. Cadmium/tin has notably lower activity but is toxic, unavailable, and not recommended.

Table 1 lists thermocouple potentials for some common materials in electronic assemblies. The information indicates the inadvisability of mixing materials in the signal path. The table also dramatically points out that you must keep copper/copper (top table entry) connections clean or a degradation of 5000-to-1 occurs as they oxidize (bottom table entry). The unusually energetic response of the copper/-copper-oxide combination necessitates cleaning digital voltmeter and Kelvin-Varley divider connections with a copper deoxidant (Caig Labs, "Deoxit" D100L).

If you find the information in **Table 1** to be seemingly academic, the implications in **Figure 4** should wake you up. This **figure** lists thermoelectric potentials for commonly employed laboratory connectors. Thermocouple activity of some connectors is more than 20 times greater than other types, so be careful when using them.

LAYOUT CAN REDUCE THERMAL ERRORS

Minimizing thermal-EMF-induced errors is possible if you pay judicious attention to pc-board layout. In general, it is good practice to limit the number of junctions in the signal path. Avoid as much as possible using connectors, sockets, switches, and other potential error sources. When avoiding the use of these error sources is impossible, attempt to balance the number and type of junctions in the signal path so that differential cancellation occurs. Ensuring this cancellation may involve deliberately creating and introducing junctions to offset unavoidable junctions, which can be a tricky procedure. Repeated and deliberate temperature excursions may be necessary to determine the optimal number and placement of added junctions. Experimentation, tempered by a healthy reserve of patience and abundance of time, is necessary. This practice, which is a common standards-laboratory procedure, can be effective in reducing drifts that originate from thermal EMFs. A simple example uses a nominally unnecessary resistor to promote such thermal balancing (**Figure 5**).

For remote signal sources, connectors may be unavoidable. In these cases, choose a connector specified for relatively low thermal-EMF activity and ensure a similarly balanced approach in routing signals through the connector along the pc board and to circuitry. If some imbalance is unavoidable, deliberately introduce an intentional counterbalancing junction. In all cases, maintain the differencing junctions in proximity, which will keep them at the same temperature. Avoid drafts and temperature gradients, which can introduce thermal imbalances and cause problems. **Figure 6** shows the LTC1150 amplifier in a test circuit to measure its temperature stability. The lead lengths of the resistors connected to the amplifier's inputs are identical. The thermal capacity each input sees is also balanced because of the

CONNECTION TYPE	DESCRIPTION	THERMOELECTRIC POTENTIAL (μV/°C)
BNC-BNC MATE		0.4
BNC-BANANA ADAPTER		0.35
BNC-BNC "BARREL" ADAPTER		0.4
MALE/FEMALE BANANA MATE SAMPLE #1		0.35
MALE/FEMALE BANANA MATE SAMPLE #2		1.1
MALE/FEMALE BANANA MATE SAMPLE #3 (TYPE SPECIFIED FOR LOW THERMAL ACTIVITY)		0.07
COPPER LUG-COPPER BANANA BINDING POST		0.08
COPPER LUG-STANDARD BANANA BINDING POST		0.5
PLATED LUG-COPPER BANANA BINDING POST		1.7

Figure 4 **Measured thermoelectric potentials of some common laboratory connectors can vary widely. The pronounced difference between samples of banana connectors is due to manufacturers' materials choice; the copper-lug/copper-banana post has 20 times lower activity than the plated-lug/copper-banana post.**

symmetrical connection of the resistors and their identical size. Thus, thermal-EMF-induced shifts are equal in phase and amplitude, and cancellation occurs. Slight air currents can still affect this arrangement. **Figure 7** shows a strip chart of output noise with a small styrofoam cup covering the circuit and with no cover in "still" air. This data illustrates why it is often prudent to enclose low-level circuitry inside some form of thermal baffle.

Thermal EMFs are the most likely, but not the only, potential low-level error source. Electrostatic and electromagnetic shielding may also be necessary. Power-supply-transformer fields are notorious sources of errors that are often mistakenly attributed to an amplifier's dc drift and noise. A transformer's magnetic field impinging on a pc trace can easily generate microvolts across that conductor in accordance with well-known magnetic theory. The circuit cannot distinguish between this spurious signal and the desired input. Attempts to eliminate the problem by rolling off the circuit's response may work, but the filtered version of the undesired pickup often masquerades as an unstable dc term. The most direct approach is to use shielded transformers, but careful layout may be equally effective and less costly.

The transformer's magnetic field may disturb a circuit that requires the transformer to be close by to achieve a good grounding scheme. An RF choke connected across a scope probe can determine the presence and relative intensity of transformer fields, aiding layout experimentation.

Another source of parasitic error is stray leakage current. You must prevent such leakage currents from influencing circuit operation. The simplest way is to connect leakage-sensitive points via Teflon standoffs. Then, stray leakage currents do not affect sensitive points because they never contact the pc board. Although this approach is effective, its implementation may not be acceptable in production.

Guarding is another technique for minimizing board-leakage effects. The guard is a pc trace that completely encircles the leakage-sensitive points. You drive this trace at a potential equal to that of the point, preventing leakage to the "guarded" point. On pc boards, the guard should enclose the node or nodes you want to protect. This guarding technique eliminates the effects of capacitor surface leakage in **Figure 3** of part 2.□

TABLE 1—THERMOELECTRIC POTENTIALS FOR VARIOUS MATERIALS

Materials	Potential (μV/°C)
Copper/copper	Less than 0.2
Copper/silver	0.3
Copper/gold	0.3
Copper-cadmium/tin	0.3
Copper-lead/tin	1 to 3
Copper/kovar	40
Copper/silicon	400
Copper/copper-oxide	1000

Note: This information comes from Keithley Instruments, "Low level measurements," 1984.

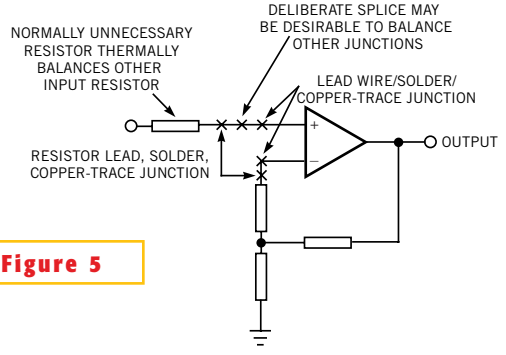


Figure 5

Typical thermal-layout considerations emphasize minimizing and compensating for parasitic thermocouples. The thermal mass at the amplifier inputs should be equal to allow parasitic-thermocouple outputs to arrive matched in phase and amplitude.

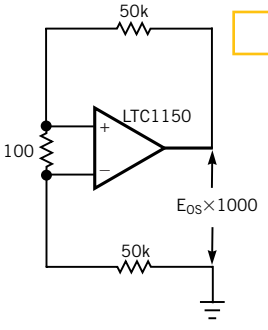


Figure 6

In an amplifier-drift test circuit, thermal EMFs and the thermal capacity at each input must be similar for cancellation to occur.

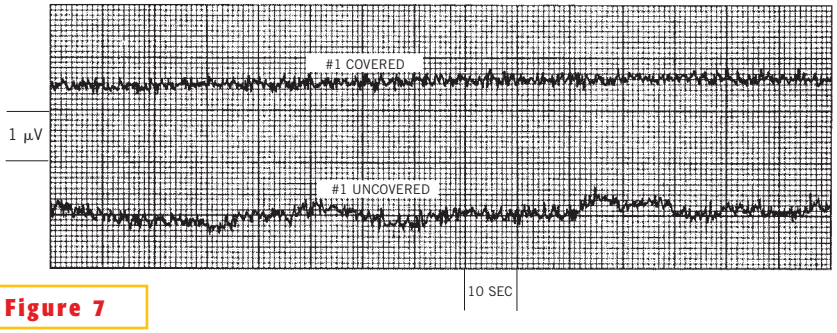


Figure 7

Slight air movement can affect the performance of a thermal baffle for a low-frequency amplifier. In the top trace, a small cup covers the amplifier, and the amplifier in the bottom trace is uncovered. The instability worsens if air movement increases.

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Author's biography

Jim Williams is a staff scientist at Linear Technology Corp (Milpitas, CA, www.linear-tech.com), where he specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA), where he first encountered serious 1-ppm measurement using the Kelvin-Varley divider. A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

 By Jim Williams, Linear Technology Corp

THERMOELECTRIC-COOLER-BASED TEMPERATURE CONTROLLERS HAVE SOME UNUSUAL REQUIREMENTS. THEY ACCOUNT FOR CIRCUIT- AND THERMAL-DESIGN CHARACTERISTICS TO PROVIDE CLIMATIC PAMPERING FOR TEMPERAMENTAL LASERS.

Controlling the temperature of fiber-optic lasers

Continued demands for increased bandwidth have resulted in the deployment of fiber-optic-based networks. Solid-state lasers drive these fiber-optic lines, which can provide high information density. Highly packed data schemes such as DWDM (dense-wavelength-division multiplexing) involve driving a fiber with multiple lasers to obtain large, multichannel data streams. The narrow channel spacing relies on precise control of laser wavelength to within 0.1 nm. Lasers can provide this precision, but temperature variation influences operation. The intensity of a laser peaks sharply versus wavelength, implying that control within 0.1 nm of laser wavelength is necessary to maintain performance (**Figure 1a**). A typical laser wavelength-versus-temperature plot exhibits a 0.1-nm/°C slope, which means that, although temperature facilitates tuning laser wavelength, the temperature must not vary after the laser wavelength has stabilized (**Figure 1b**). Typically, temperature control of 0.1°C is necessary to maintain laser operation well within 0.1 nm.

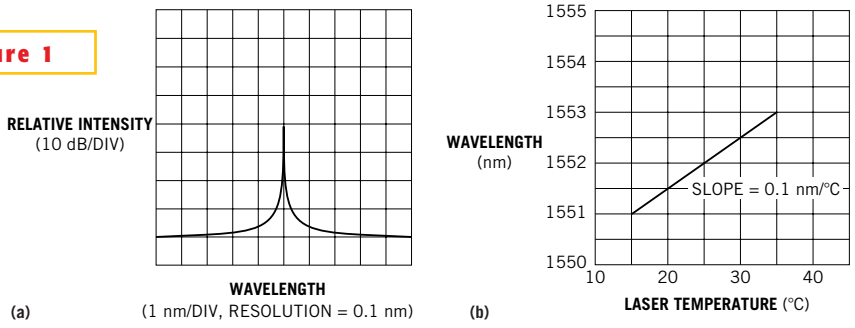
A temperature controller for this application must meet some unusual requirements. Most notably, because of ambient-temperature variations and laser-operation uncertainties, the controller must either source or remove heat to maintain control. Peltier-based TECs (thermoelectric coolers), permit this type of control, but the controller must be truly bidirectional. The controller's heat-flow control must not have a dead zone or untoward dynamics in the "hot-to-cold" transition region. Additionally, the temperature controller must be a precision device that can maintain control well inside 0.1°C over time and temperature variations. Laser-based-system packaging is compact, so that size with efficient operation is important to avoid excessive heat dissipation. Finally, the controller must operate from a single low-voltage source, and the controller's power delivery—presumably a switched-mode type—must not corrupt the supply with noise.

TEMPERATURE CONTROLLER MEETS UNUSUAL DEMANDS

The TEC temperature controller in **Figure 2** meets these demands. The circuit includes the input, which includes a DAC and thermistor; a controller stage; and the output stage, which includes the TEC. The LTC1658 DAC, IC_1, and the thermistor form a bridge, and IC_2 amplifies the output. The LTC1923 controller, IC_3, is a PWM that provides appropriately modulated and phased drive to the power-output stage.

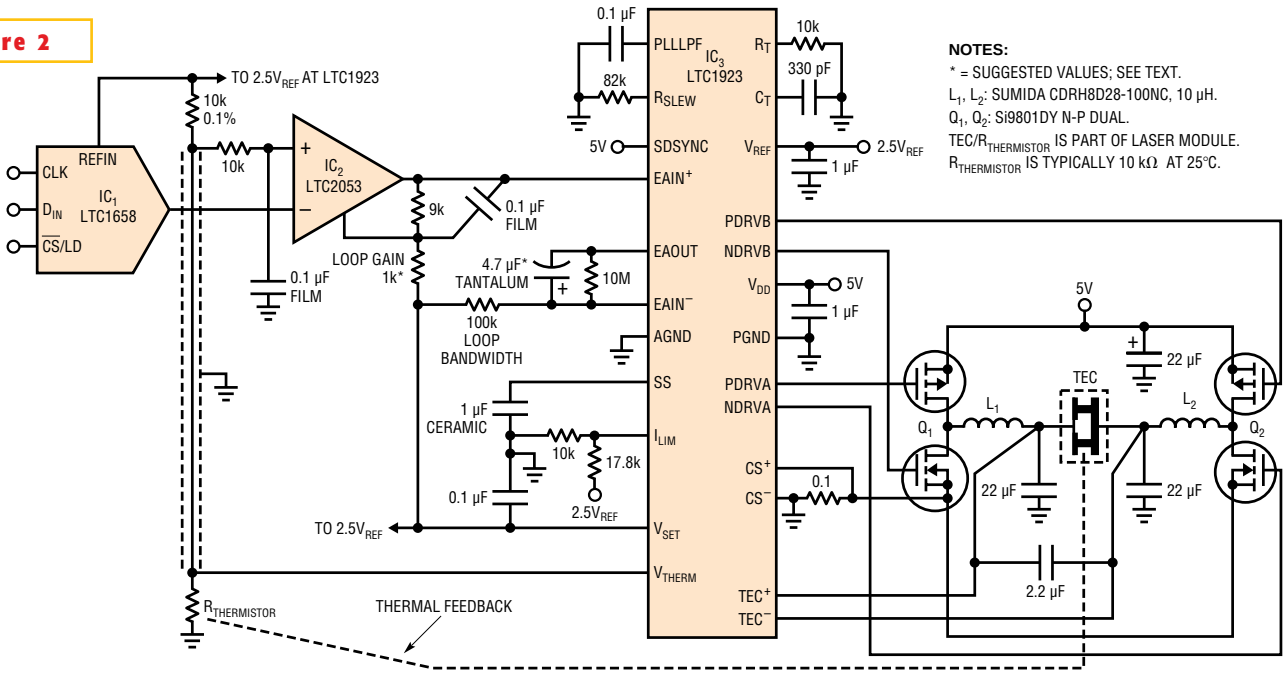
The laser is an electrically delicate and expensive load. As such, the controller provides a variety of monitoring, limiting, and overload-protection ca-

Figure 1



The peak intensity of a laser approaches 40 dB within a 1-nm window (a), and laser wavelength varies by approximately 0.1 nm/°C (b). A typical application requires wavelength stability within 0.1 nm, mandating temperature control.

Figure 2



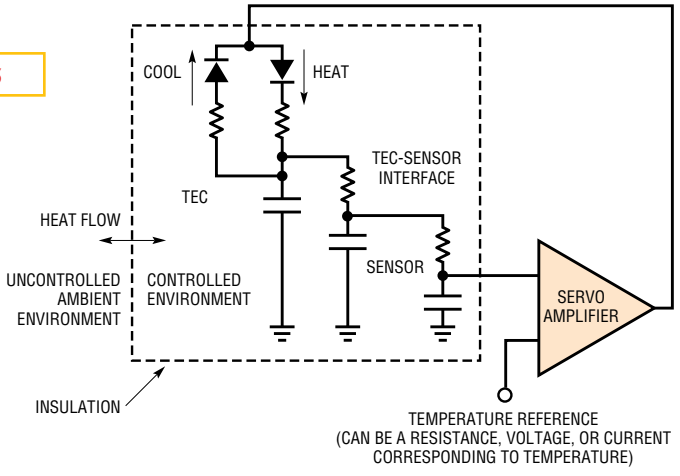
A TEC temperature controller includes a DAC, IC_1; a thermistor-bridge amplifier, IC_2; a switched-mode controller, IC_3; and a power output H-bridge. The DAC establishes the temperature setpoint, and you use a gain adjustment and compensation capacitor to optimize loop-gain bandwidth.

pabilities: soft-start and overcurrent protection, TEC-voltage sense, current sense, and "out-of-bounds" temperature sensing. Aberrant operation results in circuit shutdown, preventing laser-module damage. Two other features promote system-level compatibility. A PLL-based oscillator permits reliable clock synchronization of multiple controller ICs in multilaser systems.

Finally, the switched-mode power delivery to the TEC is efficient, but special design considerations are necessary to ensure that switching-related noise does not reflect back into the host's power supply. The controller includes edge slew limiting, which minimizes switching-related harmonics by slowing down the power stages' transition times. This feature greatly reduces high-frequency harmonic content, which prevents excessive switching-related noise from corrupting the power supply or the laser (**Reference 1**). The switched-mode-power-output stage, an H-bridge type, permits efficient bidirectional drive to the TEC, allowing either heating or cooling of the laser. The thermistor, TEC, and laser, which the manufacturer packages as one module, have tight thermal coupling.

The DAC allows you to adjust the temperature setpoint to any individual laser's optimum operating point, which manufacturers normally specify for each laser. Controller gain and bandwidth adjustments optimize the thermal-loop response for best temperature stability.

Figure 3



A simplified TEC control-loop model uses resistors and capacitors to represent thermal resistance and capacity, respectively. To avoid instability, the servo amplifier's gain bandwidth must take the lumped delay of the thermal terms into account.

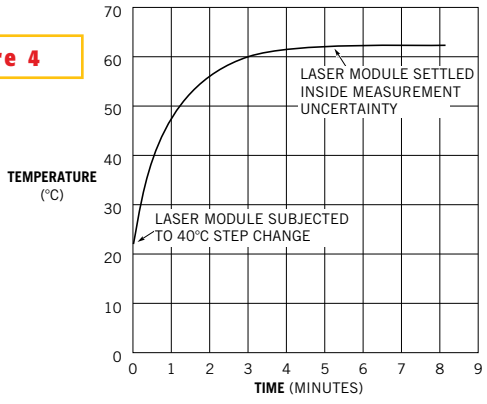
THERMAL-LOOP CONSIDERATIONS

The key to high-performance temperature control is matching the controller's gain bandwidth to the thermal feedback path. Theoretically, this matching is a simple matter using conventional servo-feedback techniques. Practically, the long time constants and uncertain delays inherent in thermal systems present a challenge. Both servo systems and oscillators are feedback systems, but one is supposed to oscillate, and the other is not. This unfortunate relationship is very apparent in thermal-control systems.

A model of the thermal-control loop

is simply a network of resistors and capacitors (**Figure 3**). The resistors are equivalent to the thermal resistance, and the capacitors are equivalent to thermal capacity. In **Figure 3**, the TEC, TEC-sensor interface, and the sensor all have RC factors that contribute to a lumped delay in the system's ability to respond. To prevent oscillation, gain-bandwidth limiting is necessary to account for this delay. Because high gain bandwidth is desirable for good control, delays need to be as low as possible. Laser-module purveyors presumably address this issue during manufacturing.

Figure 4



The package thermal resistance and capacity set the ambient-to-sensor lag characteristic for a typical laser module.

The model also includes insulation between the controlled environment and the uncontrolled ambient. The function of insulation is to keep the loss-rate low so that the temperature-control device can keep up with the losses. For any given system, the higher the ratio between the TEC-sensor time constants and the insulation time constants, the better the performance of the control loop (see **sidebar** "Practical considerations in TEC-based control loops").

PRACTICAL CONSIDERATIONS IN TEC-BASED CONTROL LOOPS

A number of practical issues are involved in implementing TEC (thermoelectric-cooler)-based control loops. These issues fall within three loosely defined categories: temperature setpoint, loop compensation, and loop gain.

It is important to differentiate between temperature accuracy and stability requirements. The exact temperature setpoint is unimportant, as long as it is stable. Each individual laser's output maximizes at some temperature (**Figure 1**). You typically increment the temperature setpoint until the laser reaches its peak intensity. At this point, the system requires only temperature-setpoint stability. For this reason, thermistor tolerances are 5% on laser-module data sheets. Thermistor stability over time primarily determines the temperature-setpoint stability over years. Thermistor-time stability is a function of operating temperatures, temperature cycling, moisture contamination, and packaging. The laser modules' relatively mild operating conditions are benign, promoting good long-term stability. You can typically expect thermistor stability comfortably inside 0.1°C over years, assuming that the laser module uses good grade thermistors.

Components that determine the temperature setpoint should have adequate stability over time and temperature. For example, the 10-kΩ, 0.1% resistor in **Figure 2** should have a temperature coefficient of 50 ppm/°C and, preferably, 25 ppm/°C to temperature-setpoint errors approaching 0.1°C over ambient temperature extremes.

An issue related to temperature setpoint is that the servo loop controls the sensor temperature. The laser operates at a somewhat different temperature from the sensor, although laser-temperature stability depends on a stable loop-controlled environment. The assumption is that the laser's dissipation constant remains fixed, which is largely true. This phenomenon also occurs in the sensor's operation. Strictly speaking, the sensor operates at a slightly higher temperature than its nominally isothermal environment. The assumption is that the sensor's dissipation constant remains fixed, which is essentially the case. Because of this fact, the sensor's temperature is stable.

The "dominant-pole" compensation scheme of **Figure 2** takes advantage of the long time constant from ambient into the laser module (**Figure 4**). The loop gain rolls off at a frequency low enough to accommodate the TEC-thermistor lag but high enough to smooth transients arriving from the outside ambient. The relatively high time-constant ratio between the TEC/thermistor and the module insulation, which ranges from less than 1 second to minutes, makes this approach viable. Attempts at improving the loop response with more sophisticated compensation schemes encounter difficulty due to the laser module's thermal-term uncertainties. Thermal terms can vary significantly between laser-module brands, rendering tailored compensation schemes impractical or even deleterious. Note that this restriction still applies, although less severely, even for modules of "identical" manufacture. It is very difficult to maintain tight thermal-term tolerances in production.

The simple dominant-pole-compensation scheme provides good loop response over a range of laser module types. This scheme is the way to go.

Both electrical and thermal gain terms set the loop gain. The most unusual aspect of the loop-gain issue is that the TEC gain differs for heating and cooling modes. Significantly more gain is available in heating mode, accounting for the higher stability in this mode (**Figure 7**). This higher gain means that you should determine loop-gain bandwidth limits in heating mode to avoid unpleasant surprises. (The suggested loop gain and compensation values of **Figure 2** reflect this suggestion.) It is certainly possible to get cute by changing loop-gain bandwidth with the mode, but performance improvement is probably not worth the ruckus. The LTC1923's "heat-cool" status pin beckons alluringly.

A TEC is a heat pump, and the temperature across the TEC determines its efficiency. Gain varies with efficiency, degrading temperature stability as efficiency decreases. Thus, you should provide good coupling from the laser module to a heat sink. Yes, this means you should use that messy white goop. A less obnoxious alternative is to use thermally conductive gaskets, which are nearly as good. The small amount of power involved does not require large heat-sink capability, but adequate thermal flow is necessary. Usually, coupling the module to the circuit's copper ground plane is sufficient, assuming the plane does not already have a thermal bias.

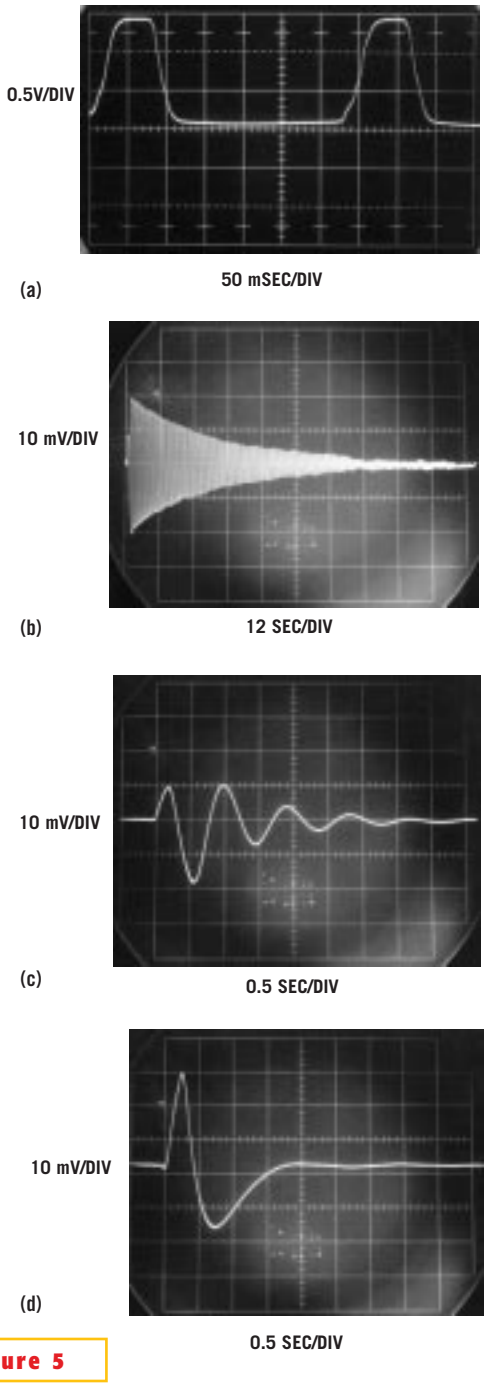


Figure 5

Deliberate excess of loop gain-bandwidth introduces large-signal oscillation, and the duty cycle reveals asymmetric gains for heating and cooling modes (a). When gain-bandwidth is still excessively high, the loop response to a small step in the temperature setpoint results in a damped, ringing response of greater than 2 minutes in duration (b). After reducing the loop gain-bandwidth, the response isn't yet optimal, but settling occurs in 4.5 seconds (c). Gain-bandwidth optimization results in nearly critically damped response with settling in 2 seconds (d).

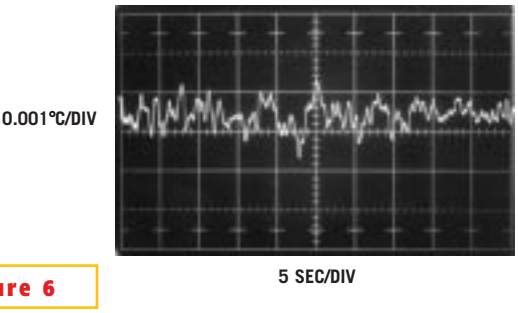


Figure 6

Short-term monitoring in a room environment indicates 0.001°C cooling-mode baseline stability.

OPTIMIZE THE TEMPERATURE-CONTROL LOOP

Temperature-control-loop optimization begins with thermal characterization of the laser module. As mentioned, the ratio between the TEC-sensor and insulation time constants is important. Determination of this information places realistic bounds on achievable controller gain bandwidth. When you subject a typical laser module to a 40°C step change in ambient temperature, the ambient-to-sensor lag, measured in minutes, exhibits a classic first-order response (**Figure 4**). The **figure** plots the laser module's internal temperature, monitored by its thermistor, versus time with no power to the TEC.

You can characterize the TEC sensor's lumped delay by operating the laser module in **Figure 2**'s circuit with the gain set at maximum and with no compensation capacitor. The result is large-signal oscillation due to thermal lag dominating the loop (**Figure 5a**). This **figure** presents a great deal of valuable information. When a circuit "doesn't work" because "it oscillates," whether at millihertz or gigahertz, four burning questions should immediately dominate the pending investigation: What are the oscillation frequency, the amplitude, the duty cycle, and the waveshape? The solution to the problem invariably resides in the answers to these queries. Just stare thoughtfully at the waveform, and the truth will bloom.

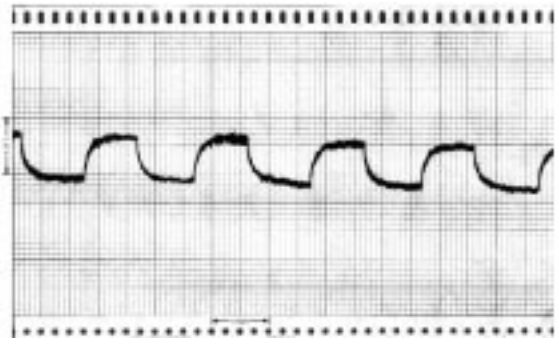
In this case, the frequency, which TEC-sensor lag primarily determines, limits how much loop bandwidth you can achieve. The high ratio of this frequency to the laser module's thermal time constant—the lag characteristic in **Figure 4**—means that simple, dominant-pole loop compensation is effective. The saturation-limited waveshape suggests that excessive gain is driving the loop into full cooling and heating states. Finally, the asymmetric duty cycle reflects the TEC's differing thermal efficiency in the cooling and heating modes.

Reducing the controller's gain bandwidth from the extremes of **Figure 5a** produced **Figure 5b**'s display. This waveform results from a small step change in the temperature setpoint of approximately 0.1°C. Gain bandwidth is still excessively high, producing a damped, ringing response that lasts longer than 2 minutes. The loop is just marginally stable. **Figure 5c**'s test conditions are identical to **Figure 5b**'s, but the gain bandwidth is significantly smaller. The response is still not optimal, but settling occurs in approximately 4.5 seconds, or approximately 25 times faster than the previous case. **Figure 5d**'s response, taken at further reduced gain-bandwidth settings, is nearly critically damped and settles cleanly in about 2 seconds. A laser module optimized in this fashion easily attenuates external temperature shifts by a factor of thousands without overshoots or excessive lags.

Further, although substantial thermal differences exist between various laser modules, some generalized guidelines on gain-bandwidth values are possible (see the **sidebar**). A dc gain of 1000 is sufficient for this application's required temperature control, with bandwidth below 1 Hz providing adequate loop stability. **Figure 2**'s suggested gain and bandwidth values reflect these conclusions, although stability testing is mandatory in all cases.

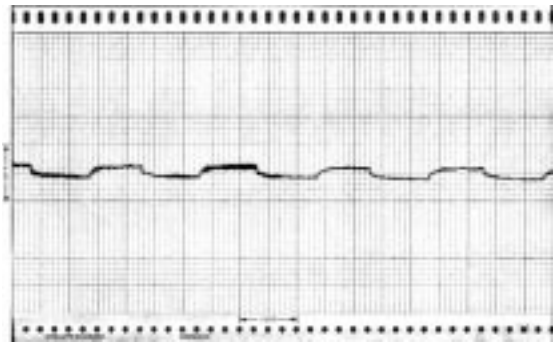
VERIFY TEMPERATURE STABILITY

After you optimize the loop, you can measure the temperature stability by



(a)

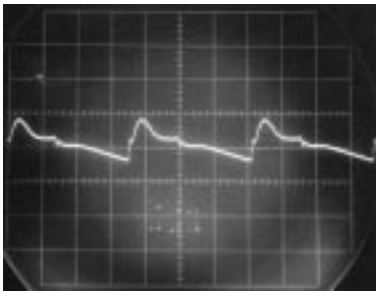
Note:
The 0.0025°C baseline tilt over plot length results from varying ambient temperature.



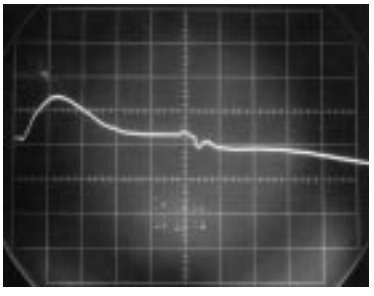
(b)

Note:
The baseline tilt, which is barely detectable, also shows a four times improvement versus part (a).

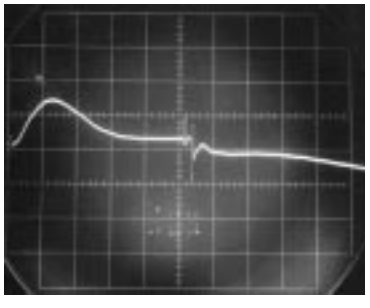
Figure 7 **A measurement of long-term cooling-mode stability in an environment that steps 20°C above ambient every hour shows a 0.008°C peak-to-peak variation, indicating a thermal gain of 2500 (a). A heating-mode measurement under identical test conditions shows a peak-to-peak variation of 0.002°C, or a fourfold stability improvement due to the TEC's higher heating-mode efficiency, which results in higher thermal gain (b).**



(a)



(b)



(c)

Figure 8 **With edge slew-rate limiting in use, the "reflected" noise at the 5V input supply due to switching-regulator operation consists of 12 mV p-p of ripple with much lower high-frequency edge-related harmonics (a). A time and amplitude expansion more clearly shows the residual high-frequency content with slew limiting (b). If you disable the slew limiting, the high-frequency harmonic content rises approximately tenfold (c).**

monitoring the thermistor-bridge offset with a stable, calibrated differential amplifier. Note that this measurement monitors thermistor stability. The laser's temperature stability is somewhat different due to slight thermal decoupling and variations in laser power dissipation.

Figure 6 records ±1 millidegree baseline stability over 50 sec in the cooling mode. A more stringent test measures longer term stability with significant variations in ambient temperature. **Figure 7a**'s strip-chart recording measures cooling-mode stability against an environment that steps 20°C above ambient every hour over nine hours. (Yes, such archaic devices as strip charts are still useful.) The data shows a variation of 0.008°C, indicating a thermal gain of 2500. (The term "thermal gain" is temperature-control-aficionado jargon for the ratio of ambient-to-controlled temperature variation.) The 0.0025°C baseline tilt over the nine-hour plot length derives from varying ambient temperature. **Figure 7b** uses identical test conditions as **Figure 7a**, except that the controller operates in the heating mode. The TEC's higher heating-mode efficiency furnishes greater thermal gain, resulting in a fourfold stability improvement to about 0.002°C variation. Baseline tilt, just detectable, shows a similar fourfold improvement versus **Figure 7a**.

This level of performance ensures the desired stable-laser characteristics. Thermistor aging characteristics primarily determine temperature stability over years.

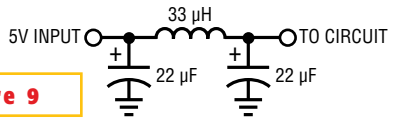


Figure 9 **An LC filter reduces reflected ripple to 1 mV and the high-frequency harmonic-noise residue to 500 µV.**

The switched-mode power delivery to the TEC provides efficient operation but raises concerns about noise injected back into the host system via the power supply. In particular, the switching edge's high-frequency harmonic content can corrupt the power supply, causing system-level problems. Such "reflected" noise can be troublesome. The LTC1923 avoids these issues by controlling the slew of its switching edges, minimizing high-frequency harmonic content (**Reference 1**). This slowing of switching transients typically reduces efficiency by only 1 to 2%, which is a small penalty for the greatly improved noise performance. **Figure 8a** shows noise and ripple at the 5V supply with slew control in use. A ripple of 12 mV in amplitude is usually not a concern, as opposed to the high-frequency transition-related components, which are much lower in amplitude. **Figure 8b**, a time and amplitude expansion of **Figure 8a**'s display, more clearly studies the high-frequency residue. High-frequency amplitude, measured at center screen, is about 1 mV. A good way to measure the effectiveness of slew limiting is by disabling it. High-frequency content jumps to nearly 10 mV, or almost 10 times worse performance (**Figure 8c**). Leave that slew limiting in there.

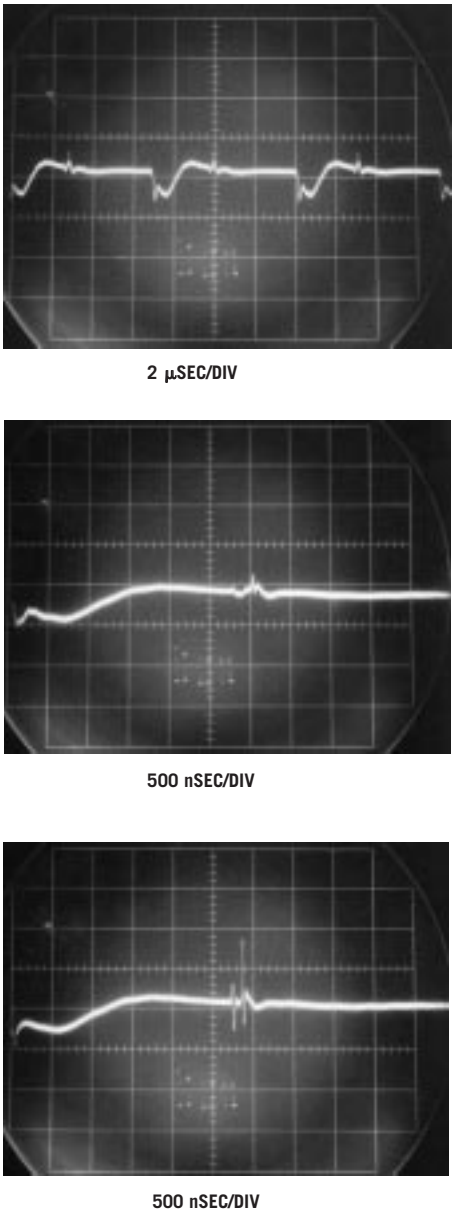


Figure 10

With an LC filter in use, 5V-supply reflected ripple measures 1 mV, and switching-edge-related harmonic content is small due to the slew-limiting action (a). Horizontal expansion shows that the high-frequency-harmonic amplitude with slew limiting is 500 µV, or approximately one-third the amplitude of Figure 9b (b). Without slew limiting, harmonic-content, amplitude rises to 2.2 mV, which is a 4.4-times degradation (c).

This level of noise reduction is suitable for most applications. Some special cases may require even lower reflected noise, and you can use a simple LC filter in these cases (**Figure 9**). Combined with the LTC1923's slew limiting, this filter provides vanishingly small reflected ripple and high-frequency harmonics. With this filter in place, the ripple is only approximately 1 mV, and the high-frequency content is at submillivolt levels (**Figure 10a**). **Figure 10b** expands the time scale to examine the high-frequency remnants. The amplitude is 500 µV, or approximately one-third of **Figure 8b**'s reading. As before, you can measure the effectiveness of slew limiting by disabling it. The result is a 4.4-times increase in high-frequency content to approximately 2.2 mV (**Figure 10c**). So, as before, if you want to achieve the lowest reflected noise, leave that slew limiting in there.□

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Author's biography

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By Jim Williams, Linear Technology Corp

IT TAKES AN AURA OF THOUGHTFUL CAUTION TO DESIGN A LASER CURRENT SOURCE. A RANGE OF CIRCUITS THAT USE LINEAR AND SWITCHED-MODE TECHNIQUES SHOWS HOW.

Current sources for fiber-optic lasers: a compendium of pleasant current events

DC CURRENT IS THE POWER SOURCE for a large group of fiber-optic lasers. A current source with modulation farther along the signal path supplies laser drive. The current source, although conceptually simple, constitutes a tricky design problem. You have to consider a number of practical requirements for a fiber-optic current source, and failure to do so can destroy lasers or optical components.

A laser current source is deceptively simple in concept. Inputs include a current-output programming port, an output-current clamp, and an enable command. Laser current is the sole output. In practice, however, a laser current source must meet a number of practical and subtle requirements. The key to a successful design is a thorough understanding of individual system requirements. Various approaches suit different sets of freedoms and constraints, although all must address some basic concerns.

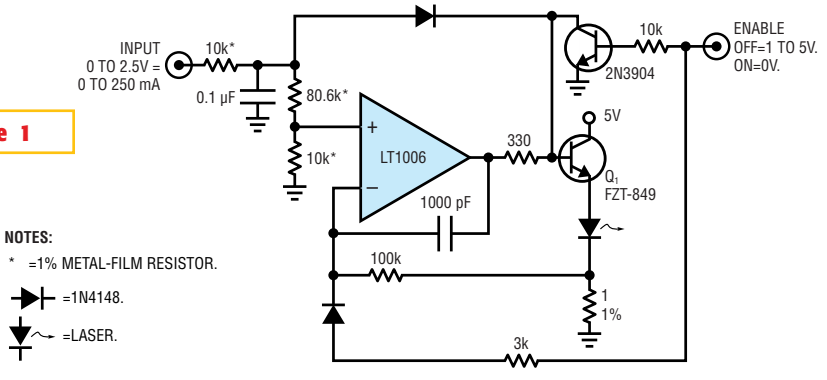
Performance and protection are the basic concerns for laser current sources. Performance issues include the current source's magnitude and stability under all conditions, output-connection restrictions, voltage compliance, efficiency, programming interface, and power requirements. Protection features are necessary to prevent laser and optical component damage. The laser, which is an expensive and delicate device, must have protection under all conditions, including supply ramp-up and -down, improper control-input commands, open or intermittent load connections, and "hot plugging."

LASER-PERFORMANCE ISSUES

The performance issues for a laser current source are as follows:

- Required power supply: The first step is to define the available power supply. A single-rail 5V supply is currently the most common and desirable. You must account for supply tolerances, which are typically ±5%. System-distribution-voltage drops may result in surprisingly low rail voltages at the point of load. Split rails are occasionally available, although they are relatively rare. Additionally, split-rail operation can complicate laser protection, particularly during supply sequencing.
- Output-current capability: Low-power lasers operate on less than 250 mA. Higher power types can require as much as 2.5A.
- Output-voltage compliance: The current source's output-voltage compliance must be able to accommodate the laser's forward-junction drop and any additional drops in the drive path. Typically, voltage compliance of 2.5V is adequate.
- Efficiency: Heat buildup in fiber-optic systems is often a concern due to space limitations. Accordingly, current-source efficiency can be an issue. Linear regulation is often adequate at low current.

Figure 1

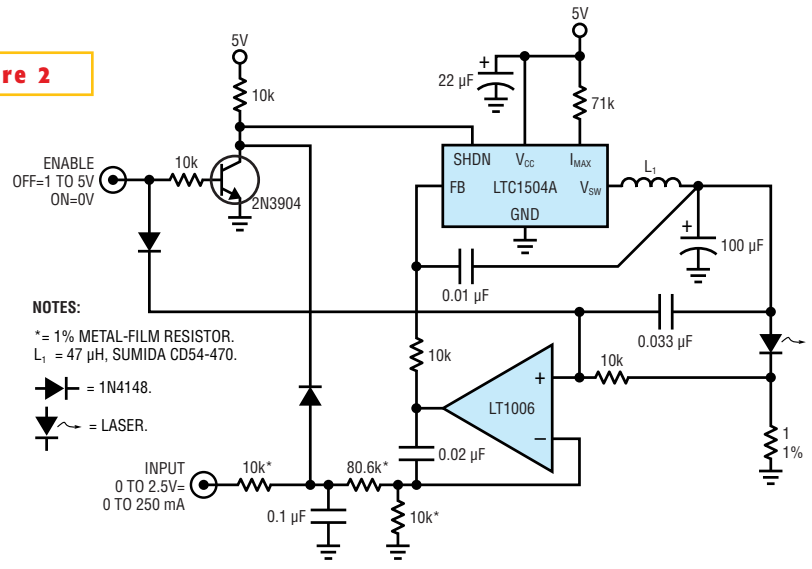


A basic current source requires off-ground operation of the laser terminals. The amplifier controls the current by comparing the 0.1Ω shunt voltage to the input.

Switching-regulator-based approaches may be necessary at high current levels.

- Laser connection: In some cases, the laser may float off ground. Other applications require grounded-anode or -cathode operation. Grounding the anode seemingly mandates a negative supply, but you can retain single-rail operation by using switching-regulator techniques.
- Output-current programming: A programming-port voltage sets the output current. You can derive the voltage from a potentiometer, DAC, or filtered PWM. Typically, a range of 0 to 2.5V corresponds to a current range of 0 to 250 mA or 0 to 2.5A. Setpoint accuracy is usually within 0.5%, although you can readily achieve better tolerances.
- Stability: The current source needs good regulation against line, load, and temperature changes. Line- and load-induced variations should be within 0.05% with typical temperature drifts of 0.01%. Judicious component choice can considerably improve these figures.
- Noise: You must minimize current-source noise, which can modulate laser output. Typically, noise bandwidth to 100 MHz is of interest. A linearly regulated current source has inherently low noise and usually presents no problems. Switching-regulator-based current sources require special techniques to maintain low noise.
- Transient response: The current source does not need a fast transient response, but you cannot under any circumstances let the output overshoot the programmed current. Such overshoots can damage the laser or associated optical components.

Figure 2



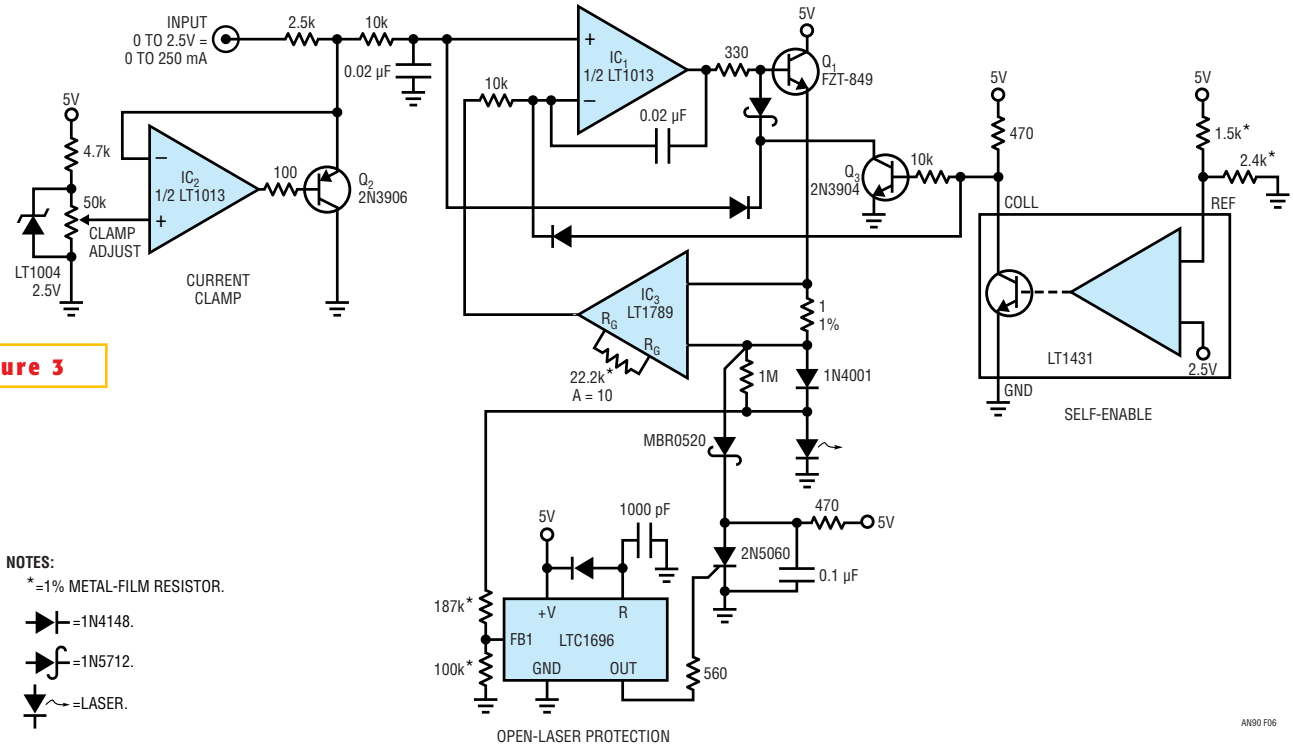
A switching regulator replaces Figure 1's Q_1 to provide higher efficiency.

LASER-PROTECTION ISSUES

The specifics of laser protection are as follows:

- Overshoot: Because outputs that

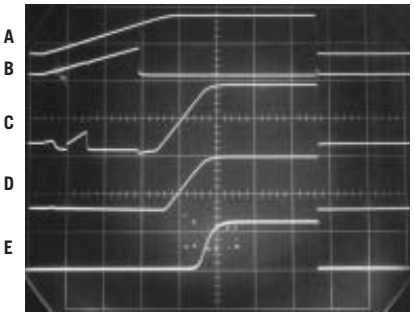
Figure 3



Differential sensing of the shunt voltage allows for grounding the laser's cathode with a single supply. A self-enable feature monitors the power supply and operates when V_{SUPPLY} is 4V. Open-laser and current clamps protect the laser.

overshoot the nominal programmed current can be destructive, you must account for any possible combination of improper control-input or power-supply turn-on and -off characteristics. Also, any spurious laser current under any condition is impermissible. Portions of the current-source circuitry may have undesired and unpredictable responses during supply ramp-up and -down, complicating the design.

- Enable: An enable line allows for shutting off the current-source output. You can also use the enable line to hold off the current-output during supply ramp-up to prevent undesired outputs. This use of the enable line can be tricky because the power supply for the enable-signal circuitry may be the same supply that runs the laser. The enable signal must reliably operate independently of the power supply's turn-on profile. Optionally, the enable function can be self-contained within the current source, eliminating the necessity of generating this signal.
- Output-current clamp: The output-current clamp sets the maximum output current, overriding the output-current programming command. A potentiometer, DAC, or filtered PWM signal can set this voltage-controlled input.
- Open-laser protection: An unprotected current source's output rises to maximum voltage if you disconnect the load. This circumstance can lead to hot-plugging the laser, a potentially destructive event. Intermittent laser connections can produce similar undesirable results. The current-source output should latch off if the load disconnects. Recycling the power clears the latch but only if the load has been established.



TRACE	DESCRIPTION	SCALE
A	POWER-SUPPLY VOLTAGE	5V/DIV
B	LT1431 OUTPUT	5V/DIV
C	IC_1 OUTPUT	2V/DIV
D	Q_1 EMITTER	2V/DIV
E	LASER CURRENT	50 mA/DIV

Figure 4 Power-supply start-up waveforms for Figure 3 show the 3-msec ramp on the 5V rail. The self-enable circuit prevents spurious IC_1 outputs during this period from corrupting the laser current.

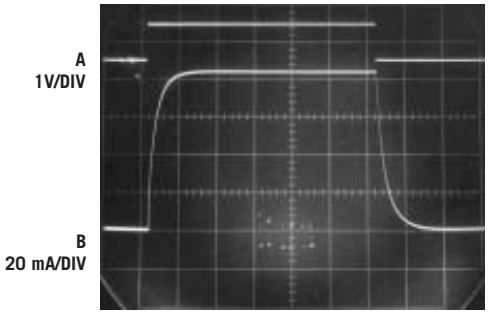
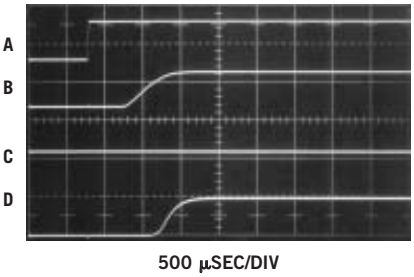


Figure 5 Figure 3's output (Trace B) responds to Trace A's input step. Trace B's laser current has controlled damping and no overshoot.

CURRENT-SOURCE CIRCUITS

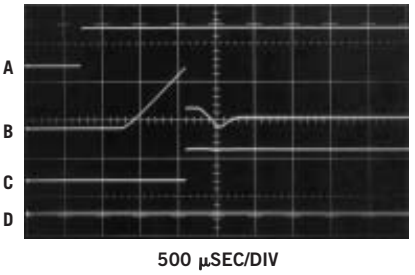
The preceding discussion dictates considerable care when designing laser-current sources. The delicate and expensive load, combined with the noted uncertainties, should promote an aura of thoughtful caution (see **sidebar** "Simulating the laser load" on the Web version of this article at www.edn.com). The following circuit examples maintain this outlook and present practical, usable circuits.

A basic laser current source supplies as much as 250 mA via Q_1 (**Figure 1**). This circuit requires that both laser terminals float. The amplifier controls laser current by maintaining the 1Ω shunt voltage at a potential that the programming input dictates. Local compensation at the amplifier stabilizes the loop, and the 0.1-μF capacitor filters input commands, ensuring that the loop never limits slew. This precaution prevents overshoot due to programming-input dynamics. The enable input turns off the current source by simultaneously grounding Q_1's base and starving the amplifier's + input while biasing the − input high. This combination also ensures that the amplifier smoothly ramps to the desired output current when the enable switches low. An external watchdog circuit that switches after the power supply is within operating limits must drive the enable input. Because the external circuitry may operate from the same supply as the current source, the enable threshold in this circuit is 1V. The 1V threshold ensures that the enable input dominates the current source's output at low supply voltages during power turn-on. This feature prevents spurious outputs due to unpredictable amplifier behavior below the minimum supply voltage.



TRACE	DESCRIPTION	SCALE
A	POWER-SUPPLY VOLTAGE	5V/DIV
B	LASER VOLTAGE	2V/DIV
C	LTC1696 OUTPUT	5V/DIV
D	LASER CURRENT	100 mA/DIV

Figure 6 Figure 3's open-laser protection does not act during normal turn-on. The LTC1696 does not exceed its overvoltage threshold, which keeps the SCR unbiased, and the laser conducts current.



TRACE	DESCRIPTION	SCALE
A	POWER-SUPPLY VOLTAGE	5V/DIV
B	LASER OUTPUT	2V/DIV
C	LTC1696 OUTPUT	5V/DIV
D	LASER CURRENT	1 mA/DIV

Figure 7 When the laser voltage exceeds the overvoltage threshold, the LTC1696 output biases the SCR, which clamps open the laser line, and no current flows.

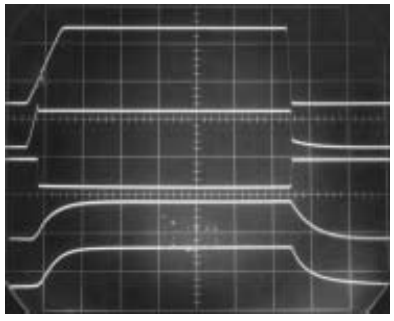
The preceding circuit uses Q_1's linear regulation to close the feedback loop. This approach offers simplicity at the expense of efficiency. Q_1's power dissipation can approach 1W under some conditions. Many applications permit this amount of power, but some situations require minimizing heat. Replacing Q_1 with a step-down switching regulator minimizes the heat (**Figure 2**). The switched-mode power delivery eliminates almost all of the transistor's heat.

This circuit is similar to **Figure 1**'s linear approach, except for the addition of the LTC1504 switching regulator. It is useful to liken the switching regulator's input, V_{CC}; feedback, FB; and output, V_{SW}; to the collector, base, and emitter, respectively, of Q_1 in **Figure 1**. This analogy reveals that two circuits have similar operating characteristics with the switched-mode version enhancing efficiency. The regulator's output LC filter introduces phase shift, necessitating attention to loop compensation. The amplifier's local roll-off is similar to that in **Figure 2**, although good loop damping requires two phase-leading ac feedback elements, the 0.01- and 0.033-µF capacitors. In all other respects, including enable and programming-input considerations, **Figure 2**'s circuit is identical to that in **Figure 1**.

GROUNDED-CATHODE OPERATION

It is sometimes necessary to tie the laser's cathode to ground. A new circuit operates from a single supply and features grounded-cathode operation (**Figure 3**). This circuit is reminiscent of **Figure 1** with a notable exception. In this case, differential amplifier IC_3 senses the voltage across a shunt in the laser anode, permitting cathode grounding. IC_2's gain-scaled output feeds back to IC_1 for loop closure. Loop-compensation and enable-input considerations are similar to the circuits in **figures 1** and **2**, and, as before, you can replace Q_1 with a switching regulator.

Three additional features allow the circuit in **Figure 3** to operate in a fully protected and self-contained fashion. The circuit monitors its power supply and "self-enables" when the supply is within limits, eliminating the enable port and external watchdog in the previous examples. A settable current clamp and open-laser protection prevent laser damage. The self-enable uses an LT1431 shunt regulator. This regulator has the highly desirable property of maintaining a predictable open-collector output when operating below its minimum supply voltage. At initial turn-on, supply voltage is 1V, the LT1431's output does not switch, and current flows to Q_3's base. Q_3 turns

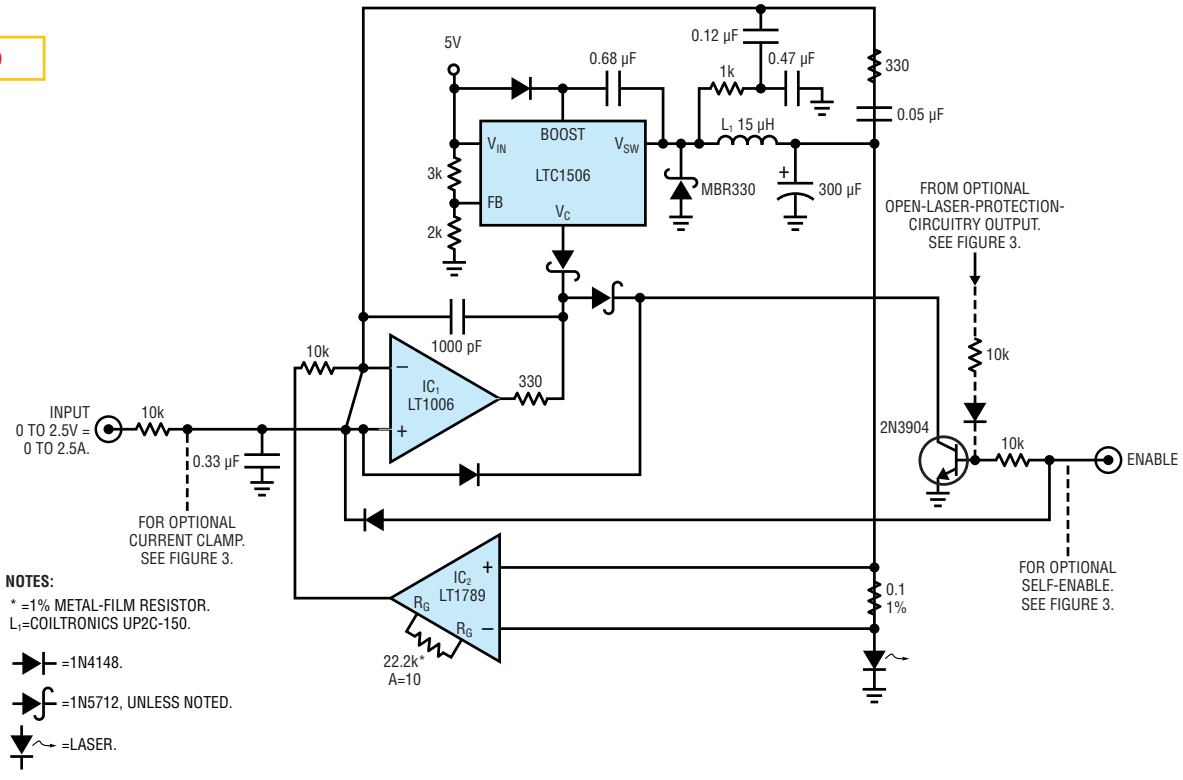


500 µSEC/DIV

TRACE	DESCRIPTION	SCALE
A	PROGRAMMING INPUT	2V/DIV
B	Q_2 EMITTER	1V/DIV
C	IC_2 OUTPUT	5V/DIV
D	IC_1 + INPUT	1V/DIV
E	LASER CURRENT	100 mA/DIV

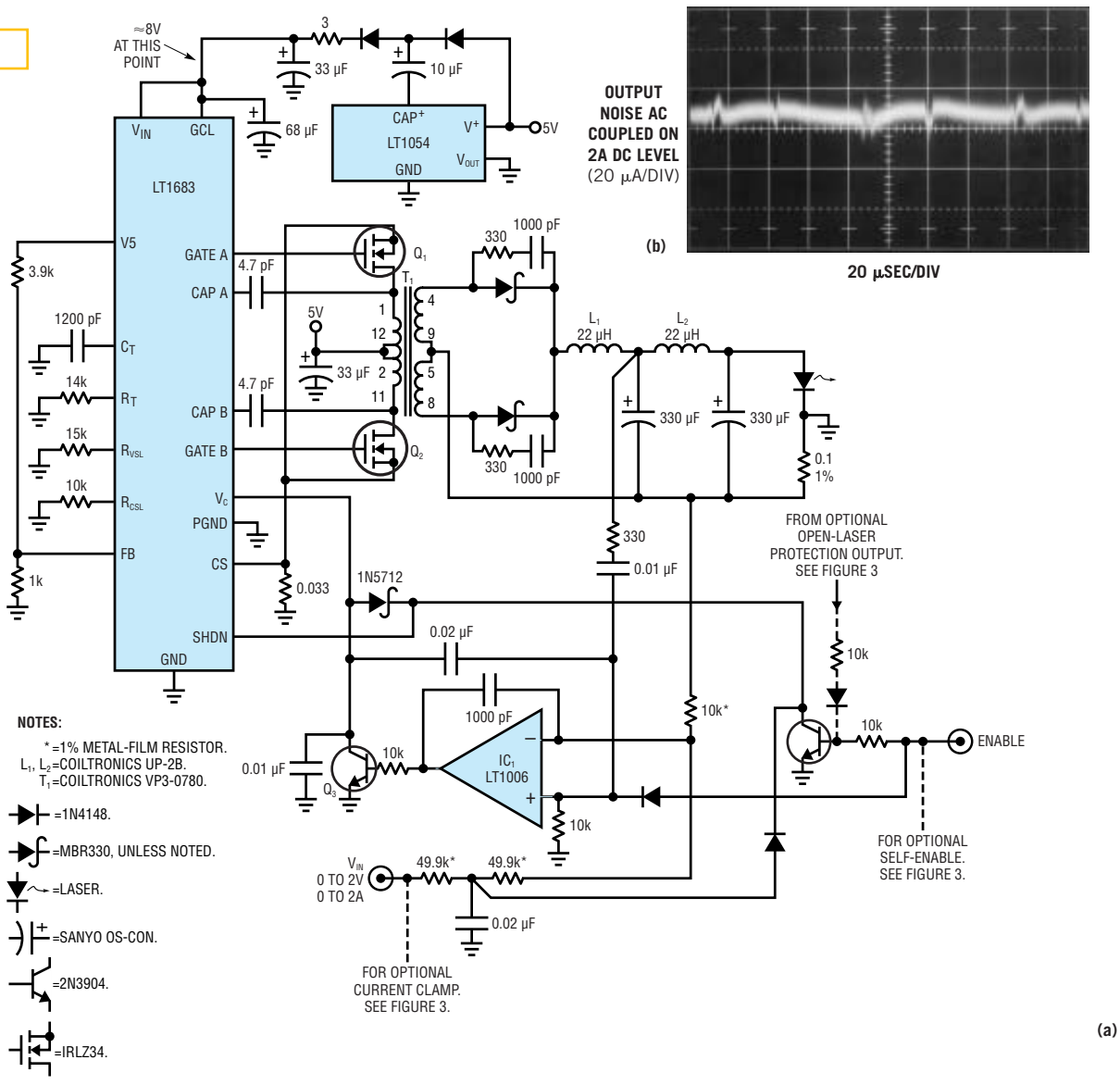
Figure 8 **When the programming input in Figure 3 exceeds the clamp threshold, IC_2 swings abruptly, which causes Q_2's emitter to clamp. IC_1's + input remains at this clamp level, which maintains a safe amount of laser current.**

Figure 9



A switched-mode version of Figure 3 provides 2.5A. Feedback-loop compensation accommodates the switching-regulator delay. Clamp, protection, and self-enable circuits are optional.

Figure 10



A 2A laser current source has a grounded-cathode output (a). Output noise measures 20 µA p-p, or approximately 0.001% (b). Coherent, identifiable components include fundamental-ripple residue and switching artifacts.

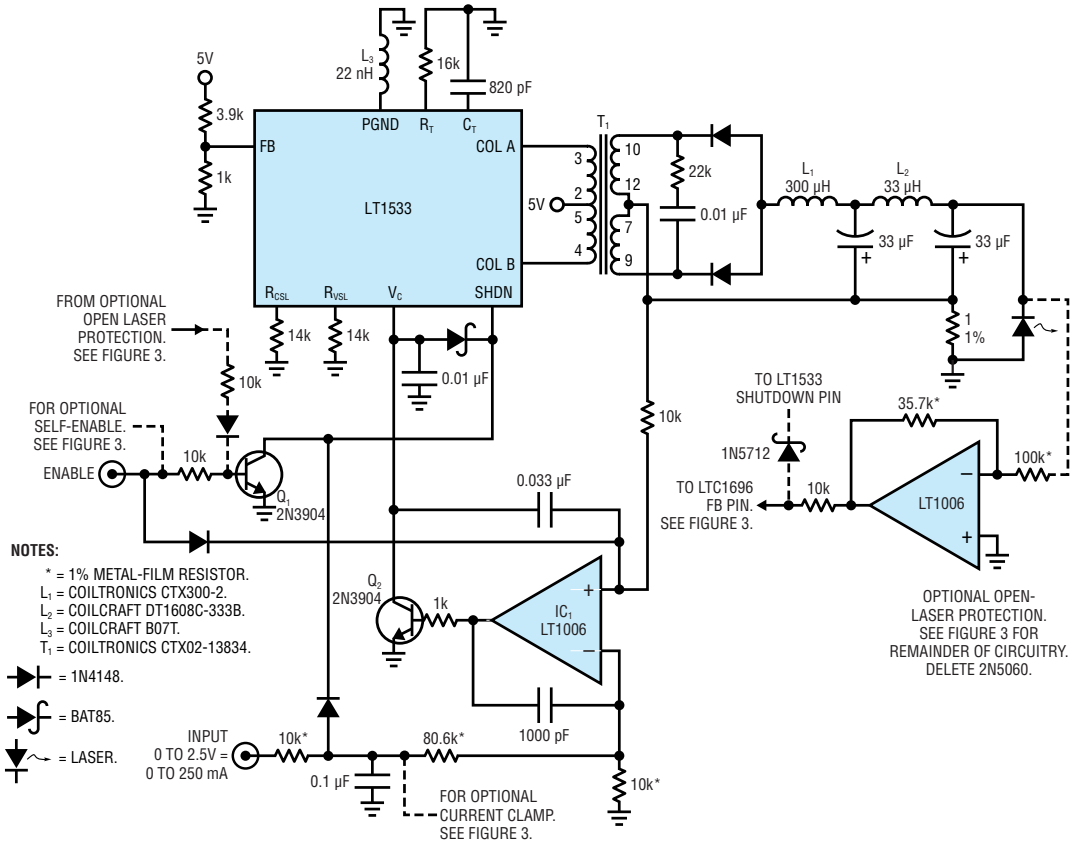
on, preventing Q_1's base from receiving bias. Additionally, this action pulls down the circuit's current-programming input, which drives IC_1's − input. This arrangement ensures that the laser cannot receive current until Q_3 turns off. Also, when Q_3 turns off, IC_1's output cleanly ramps up to the desired programmed current. The resistor values at the LT1431's reference input dictates that the device goes low when V_{SUPPLY} passes through 4V. This 4V potential ensures proper circuit operation.

Supply start-up waveforms detail these self-enable features (**Figure 4**). Trace A, the nominal 5V rail, ramps for 3 msec before arriving at 5V. During this interval, the LT1431 (Trace B) follows the ramp, biasing Q_3 on. The circuit does not control IC_1's output (Trace C) during this period. Q_1's emitter (Trace D), however, is cut off due to Q_3's conduction and cannot pass the disturbance. As a result, the laser conducts no current (Trace E) during this time. When the supply (Trace A) ramps beyond 4V (just before the photo's fourth vertical division), the LT1431 switches low (Trace B), Q_3 switches off, and the circuit self-enables. IC_1's output (Trace C) ramps up, and Q_1's emitter (Trace D) and the laser current (Trace E) are slaves to the output's movement. This action prevents any undesired current in the laser during supply turn-on, regardless of unpredictable circuit behavior at low supply voltages.

PROGRAMMING-INPUT CHANGES

You must control laser current in situations other than supply turn-on. Response to programming-input changes must be similarly well-behaved. The laser-current response (Trace B) to a programming input step shows clean damping with no hint of overshoot (Trace A, **Figure 5**). The circuit in **Figure 3** also includes open-laser protection. If the current source operates into an open load

Figure 11



A 0.0025% noise, grounded-anode laser current source outputs 250 mA.

with no laser, the source produces maximum voltage at the laser output terminals. This circumstance can lead to hot-plugging the laser, a potentially destructive event. Intermittent laser connections can produce similar undesirable results. The LTC1696 overvoltage-protection controller guards against open-laser operation. This device's output latches high when its feedback input, FB, exceeds 0.88V. This circuit biases the FB pin so that a laser output voltage greater than 2.5V forces the LTC1696 high, triggering the SCR to shunt current away from the laser. The 470Ω resistor supplies SCR holding current, and the diodes ensure that no current flows in the output.

Figure 6 details events with a properly connected laser at supply turn-on. Trace A is the supply; Trace B, the laser voltage; Trace C, the LTC1696 output, and Trace D, the laser current. The waveforms show laser voltage, Trace B, rising to about 2V at supply turn-on, Trace A. Under these normal conditions, the LTC1696 output, Trace C, stays low, and laser current, Trace D, rises to the programmed value.

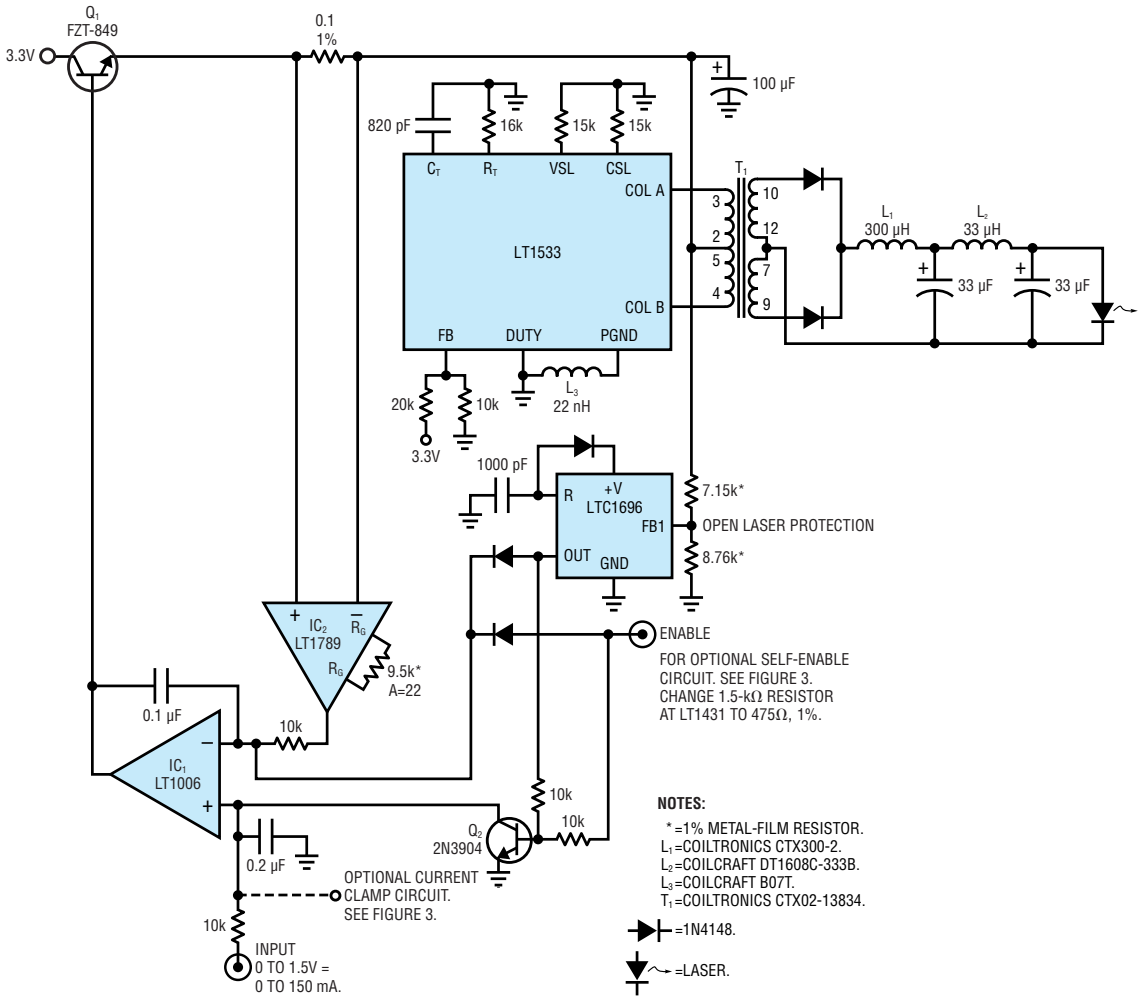
Figure 7 shows what happens when the circuit turns into an open-laser connection. Trace assignments are identical to those in **Figure 6**. At supply turn-on, Trace A, the laser voltage, Trace B, transitions beyond the 2.5V open-laser threshold. The LTC1696 output, Trace C, goes high; the SCR latches; and no current flows in the shunted laser line, Trace D. Once this event occurs, you must recycle the power to reset the LTC1696-SCR latch. If the laser has an improper connection, the circuit repeats its protective action. Open-laser protection is not restricted to turn-on. It also occurs if laser connection is lost at any time during normal circuit operation.

A final protection feature in **Figure 3** is a current clamp that prevents the transmission of uncontrolled programming inputs by clamping them to a settable level. IC_2, Q_2, and associated components form the clamp. Normally, IC_2's + input is above the circuit's programming input (Q_2's emitter voltage), IC_2's output is high, and Q_2 is off. If the programming input exceeds IC_2's + input level, IC_2 swings low, Q_2 comes on, and the amplifier feedback drives Q_2's emitter to the clamp-adjust wiper potential. This action clamps IC_1's input to the clamp-adjust setting, which prevents laser-current overdrive. Clamp action need not be fast to be effective because of IC_1's 10-kΩ, 0.02-µF input filter. **Figure 8**'s traces show clamp response to programming-input overdrive. When the programming input, Trace A, exceeds the clamp's preset level, Q_2's emitter Trace B, does the same, causing IC_2's output, Trace C, to swing down. IC_2 feedback controls Q_2's emitter to the clamp level, arresting the voltage applied to the 10-kΩ, 0.02-µF filter. The filter bandlimits the abrupt clamp operation, resulting in a smooth corner at IC_1's positive input, Trace D. IC_1's clamped input dictates a similarly shaped and clamped laser current, Trace E. The clamp remains active until the programming input falls below the clamp-adjust setting.

GROUNDED-CATHODE SOURCE PROVIDES 2.5A

The circuit in **Figure 9**, which stems from those in **figures 2** and **3**, provides as much as 2.5A to a grounded-cathode

Figure 12



A switched-mode, low-noise current source has a floating output, which permits you to ground the laser's anode or cathode.

laser. IC_1 is the control amplifier, the LT1506 switching regulator efficiently delivers output current, and IC_2 senses laser current via a 0.1Ω shunt resistor. Loop operation is similar to that in **figures 2** and **3** with IC_2 providing dc feedback to IC_1. Frequency compensation differs from that in the previous **figures.** The circuit achieves stable loop operation using a local roll-off at IC_1, augmented by two lead networks associated with L_1. Feeding back a lightly filtered (1-kΩ, 0.47-µF) version of the LT1506's V_{SW} pin's output activity provides midband lead. High-frequency lead compensation, arriving via the 330Ω, 0.05-µF pair, optimizes edge response. The circuit in **Figure 9** uses the externally controlled enable function, although you can also use **Figure 3**'s self-enable feature. Similarly, you can also employ **Figure 3**'s current clamp and open-laser protection in this circuit.

This circuit's switched-mode energy delivery provides high efficiency at high power, but output noise may be an issue. Residual harmonic content related to switching-regulator operation appears in the laser current. The resultant low-level modulation of laser output may be troublesome in some applications. Approximately 800 µA p-p of switching-regulator-related noise (0.05%) appears in the 2A laser-current output. This disturbance comprises fundamental ripple and switching-transition-related harmonics.

LOWER THE NOISE TO 0.001%

A 0.05% noise content suits many optical-system applications. More stringent requirements benefit from extremely low-noise content. A grounded-cathode, 2A circuit uses special switching- regulator techniques to attain only 20 µA p-p noise, which is approximately 0.001% (**Figure 10a**). The circuit substantially reduces the noise by limiting edge-switching speed in the regulator's power stage (**Reference 1**). The LT1683 pulse-width modulator controls the voltage and current rise times in switches Q_1 and Q_2. The LT1683's output stage operates Q_1 and Q_2 in local loops that sense and control their edge times. The circuit feeds back transistor-voltage information using the 4.7-pF capacitors and derives and feeds back current status from the 0.033Ω shunt resistor. This arrangement permits the PWM-control IC to fix transistor-switching times, regardless of power-supply or load changes. The R_{VSL} and R_{CSL} resistors associated with the LT1683 controller set the transition rates. In practice, you set these resistor values by adjusting them to minimize output noise. The remainder of the circuit

forms a grounded-cathode laser-current source.

Q_1 and Q_2 drive T_1, and LC sections filter the rectified output. Because T_1's secondary winding floats, the laser cathode and the 0.1Ω shunt resistor are at circuit ground. The shunt returns to T_1's secondary center tap, completing a laser-current-flow path. This arrangement produces a negative voltage that corresponds to laser current at the shunt's ungrounded end. The circuit resistively sums this potential at IC_1 with the positive-voltage current-programming-input information. IC_1's output controls the LT1683's pulse-width drives to Q_1 and Q_2 via Q_3, closing a loop to set laser current. The circuit sets loop compensation using bandlimiting at IC_1 and Q_3's collector, aided by a single-lead network arriving from the L_1-L_2 junction.

Some circuit details merit attention. An LT1054-based voltage multiplier feeds the LT1683's supply-input pins. This boosted voltage provides enough gate drive to ensure Q_1-Q_2 saturation. Damper networks across T_1's rectifiers minimize diode-switching-related events in the output current. This circuit is compatible with the self-enable and laser-protection features of the previous circuits. Appropriate connection points appear in the **figure**.

The speed-controlled switching times result in a spectacular decrease in noise to just 20 µA p-p, or approximately 0.001% of the 2A-dc laser current (**Figure 10b**). Fundamental ripple residue and switching artifacts are visible against the measurement noise floor. Reliable wideband current-noise measurement at these levels requires special techniques (see **sidebar** "Verifying switching-regulator-related noise" in the Web version of this article at www.edn.com).

GROUND THE ANODE, AND KEEP NOISE LOW

The circuit in **Figure 11** is similar to that in **Figure 10** and uses edge-time control to achieve an exceptionally low-noise output of 0.0025%. This circuit is intended for lower power lasers that require grounded-anode operation. The LT1533, a version of the previous circuit's LT1683, has internal power switches. These switches drive T_1. T_1's rectified and filtered secondary produces a negative output that biases the laser. The laser's anode connects to ground, and the 1Ω shunt resistor completes the current path to T_1's secondary winding. This configuration makes T_1's center tap voltage positive and proportional to laser current. IC_1 compares this voltage to the current programming input. IC_1 biases Q_2, closing a loop around the LT1533. Local bandwidth limiting at IC_1 and Q_2's collector damping and feedback capacitors provide loop compensation.

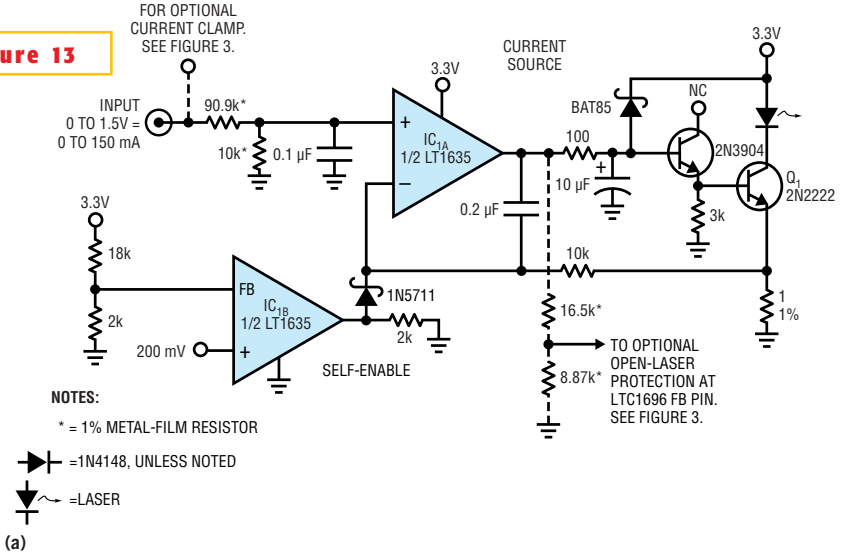
This circuit's 2.5 µA p-p noise qualifies it for the most demanding applications. Residual switching-related noise approaches the measurement noise floor. The enable function operates as previously described. Additionally, this circuit is compatible with **Figure 3**'s self-enable and laser-protection accessory circuits. The **figure** shows the changes that the grounded-anode operation necessitates.

FLOAT THE OUTPUT

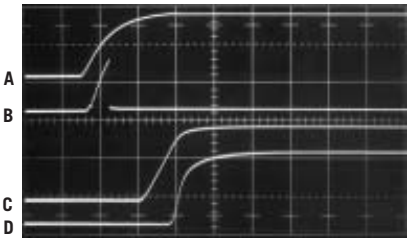
Figure 12 retains **Figure 11**'s low noise but also has a fully floating output. You can ground either laser terminal without affecting circuit operation. The circuit realizes this feature by using feedback to control the transformer's primary current and by relying on interwinding coupling to maintain regulation (**references 2**, **3**, and **4**). This coupling varies slightly with operating point, limiting the output-current regulation to approximately 1%.

The schematic shows the LT1533 low-noise switching regulator driving T_1. The circuit forces the LT1533 to run at a 50% duty cycle by grounding the duty pin. The LT1533 retains its controlled edge-time characteristics. Current flows through Q_1 and the 0.1Ω shunt resistor into T_1's primary winding. The LT1533's open-collector power outputs alternately chop primary current to ground. Q_1's bias sets the primary-current magnitude and, hence, the 0.1Ω shunt voltage. IC_1's output, which represents the difference between the output-current-programming input and IC_2's amplified version of the shunt voltage, sets Q_1's bias. This loop enforces a shunt voltage that's proportional to the value of the current-programming input. In this way, the current-programming input sets T_1's primary current, which determines T_1's secondary current through the laser. Differen-

Figure 13



(a)



20 µSEC/DIV

TRACE	DESCRIPTION	SCALE
A	POWER-SUPPLY VOLTAGE	2V/DIV
B	COMPARATOR OUTPUT	1V/DIV
C	Q_1 BASE	0.5V/DIV
D	OUTPUT CURRENT	50 mA/DIV

(b)

This circuit commits the laser's anode to the supply voltage and features inherent self-enabled operation (a). The output current is off until the supply voltage ramps past 2V, the self-enable comparator operates above 1.2V, and biasing at Q_1's base prevents outputs below 1.2V (b).

tial amplifier IC_2's gain-setting resistor calibrates the current-programming input's scaling.

The primary-side feedback's lack of global feedback mandates a current-regulation compromise. A plot of laser current versus programming input voltage shows 1% conformance over nearly the entire range. Some error below 10 mA exists due to nonideal transformer behavior, but this error is normally insignificant because it is below the typical laser-threshold current. Line regulation, which the sensing scheme also degrades, still is approximately 0.05%/V. Similarly, load regulation, over a 1 to 1.8V compliance voltage, is typically 2%.

This circuit's floating output complicates including the laser-protection and self-enable features of **Figure 3**. Biasing the LTC1696 from T_1's center tap accomplishes open-laser protection. If the laser opens, the loop forces a marked rise at T_1's center tap, latching the LTC1696's output high. This action skews IC_1's inputs, sending its output low and shutting off Q_1. All T_1 drive ceases. Because the LTC1696 output latches, you must recycle the power to reset the circuit. If you haven't connected the laser, the latch acts again, protecting the laser from hot-plugging or intermittent connections. You can add the self-enable and current-clamp options in accordance with the notations on the schematic.

CONNECT ANODE TO POSITIVE SUPPLY

Figure 13a's current source is useful for applications that commit the laser anode to the power supply. IC_{1A} senses Q_1's emitter and closes a loop that forces constant current in the laser. Local compensation at IC_1 and input bandlimiting stabilize the loop. This circuit also includes an inherent self-enable feature. The LT1635 operates at supply voltages as low as 1.2V. At voltages higher than 1.2V, the LT1635's comparator-configured section, IC_{1B}, holds off circuit output until the supply voltage reaches 2V. Below 1.2V supply, Q_1's base biasing prevents unwanted outputs. The slew-retarded input and loop compensation yield a clean dynamic response with no overshoot. As the **figure** shows, you can again include current-clamping and open-laser-protection options. Additionally, higher output current is possible at increased supply voltages, although you must respect Q_1's dissipation limits.

Figure 13b details operation during supply turn-on. At supply ramp-up (Trace A), output current (Trace D) is disabled. When the supply reaches 2V, IC_{1B} (Trace B) goes low, permitting IC_{1A}'s output (Trace C) to rise. This action biases Q_1, and laser current flows (Trace D). The LT1635 operates on supply voltages as low as 1.2V. Below this level, the circuit prevents spurious outputs using junction stacking and bandlimiting at Q_1's base. Q_1's base components also prevent unwanted outputs when the supply rises rapidly. Such rapid rise could cause uncontrolled IC_{1A} outputs before the amplifier and its feedback loop are established.□

AUTHOR'S BIOGRAPHY

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). A former student at Wayne State University (Detroit), Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

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SIMULATING THE LASER LOAD

Fiber-optic lasers form a delicate, unforgiving, and expensive load. Thus, breadboarding with these devices has a high likelihood of catastrophe. A much wiser alternative is to simulate the laser load using either diodes or electronic equivalents.

Lasers look like junctions with typical forward voltages of 1.2 to 2.5V. The simplest way to simulate a laser is to stack appropriate numbers of diodes in series. Tables A and B list typical junction voltages at various currents for two popular diode types. The MR750 is suitable for currents in the ampere range, and the 1N4148 serves well at lower currents. Typically, stacking two to three diodes allows you to simulate the laser in a given current range. Diode-voltage tolerances and variations due to temperature and current changes limit accuracy, although results are generally satisfactory.

Figure A depicts a laser-load simulator powered by a 9V battery. This simulator eliminates diode-load junction-voltage drop uncertainty. Additionally, you can conveniently set any desired "junction-dope" voltage with the indicated potentiometer. Electronic feedback enforces establishment and maintenance of calibrated junction-drop equivalents.

The potentiometer sets a voltage at amplifier IC_1's negative input. IC_1 responds by biasing Q_1. Q_1's drain voltage controls Q_2's base and, hence, Q_2's emitter potential. The circuit feeds Q_2's emitter back to IC_1, closing a loop around the amplifier. This loop forces the voltage across Q_2 to equal the potentiometer's output voltage under all conditions. The capacitors at IC_1 and Q_1 stabilize the loop, and Q_2's base resistor and ferrite bead suppress parasitic oscillation. The 1N5400 prevents Q_1-Q_2 reverse biasing if you reverse the load terminals.

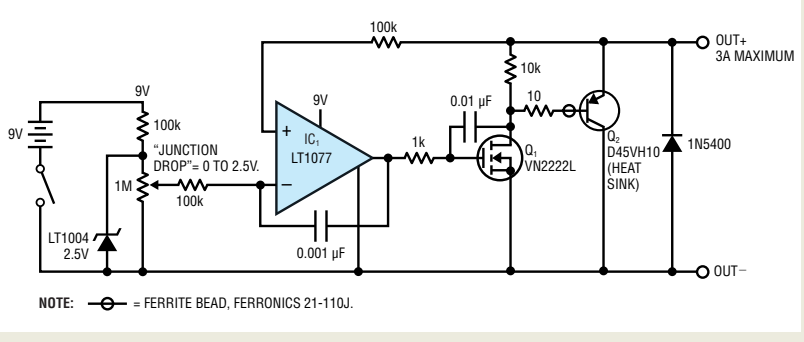


Figure A A floating, battery-powered laser simulator sets the desired junction drop across the output terminals. Amplifier feedback controls Q_2's V_{CE} according to the potentiometer voltage.

TABLE A–CHARACTERISTICS OF MR750 DIODE AT 25°C

Typical junction current (A)	Typical junction voltage (V)
0.5	0.68
1.0	0.76
1.5	0.84
2.0	0.9
2.5	0.95

TABLE B–CHARACTERISTICS OF 1N4148 DIODE AT 25°C

Current probe	Amplifier	Noise floor (100-MHz bandwidth, µA)	Comments
Tektronix P6022 (1 mV/mA)	Preamble 1855 (1 MΩ)	100	Split core is convenient to use, but sensitivity is low, resulting in relatively high overall noise floor.
Tektronix CT-1 mV/mA)	Hewlett-Packard 461A (50Ω)	15	This probe's higher gain accounts for most of the noise-floor reduction. The 50Ω amplifier provides some additional benefit. A close-core probe requires a breaking conductor to make a measurement.

VERIFYING SWITCHING-REGULATOR-RELATED NOISE

Measuring the low switching-regulator-related current noise levels in these laser-current circuits requires care. The microamp amplitudes and wide bandwidth of interest (100 MHz) mandates strict attention to measurement technique. In theory, simply measuring the voltage drop across a shunt resistor permits you to determine the current. In practice, the resultant small voltages and required high-frequency fidelity pose problems. Coaxial probing techniques are applicable, but probe-grounding requirements become severe. The slightest incidence of multiple ground paths—ground loops—corrupt the measurement, rendering observed results meaningless. Differentially configured coaxial probes offer some relief from ground-loop-based difficulties, but there is an inherently better approach.

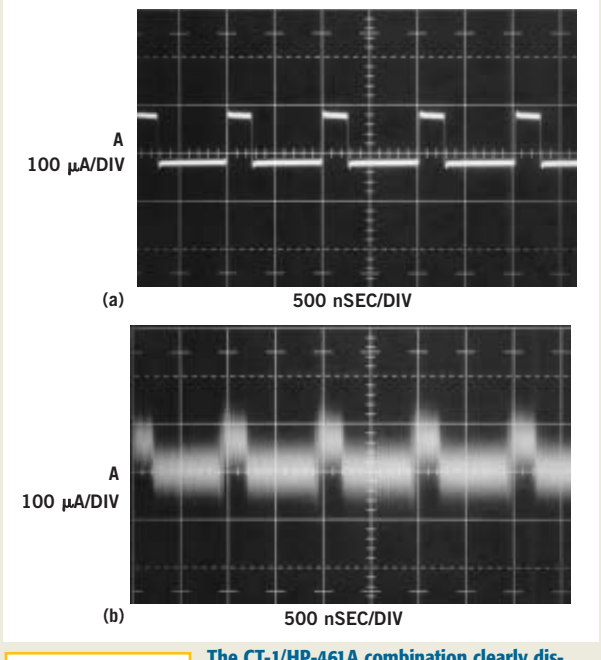


Figure A The CT-1/HP-461A combination clearly displays a 100-µA pulse train (a). The noise floor causes the slight trace thickening. The P6022/Preamble 1855 presentation shows degraded signal-to-noise performance (b).

Current transformers, or probes, offer an attractive way to measure noise and eliminate probe-grounding concerns. A current probe's minimally invasive nature eases connection parasitics, enhancing measurement fidelity. Two types of current probes are available: split core and closed core. The split-core clip-on types are convenient to use but have relatively low gain and a higher noise floor than closed-core types. The closed-core transformer's gain and noise-floor advantages are particularly attractive for wideband, low-current measurement.

Combinations of current probes and amplifiers provide varying degrees of performance and convenience. **Table A** summarizes characteristics for two probes and applicable amplifiers. In general, the construction of the convenient split-core types compromises their noise-floor uncertainties. The closed-core probes are quieter, and some types have inherently higher gain, which is a distinct advantage. A laboratory-based comparison is revealing.

The CT-1 closed-core probe and the HP461A amplifier combination respond to a 100-µA pulsed input with a clearly outlined waveform (**Figure Aa**). The pulse's top- and bottom-trace thickening derives from the noise floor. With the same input, the split-core P6022 and Preamble 1855 combination has much greater noise (**Figure Ab**). The decreased performance is due almost entirely to the split-core probe's construction.

Note that Hall-element stabilized current probes, such as the Tektronix AM503 and P6042, are unsuitable for low-level measurement. The Hall-device-based

flux-nulling loop extends the probe's response to dc but introduces approximately 300 μA of noise.

A test setup allows investigation of the closed-core transformer's capabilities (**Figure Ba**). A defined pulse is the input to the test setup in the **figure**, but in real use you may need to use a specialized external trigger probe for these measurements (**Reference A**). The specified transformer has flat gain over a wide bandwidth, a well-shielded enclosure, and a coaxial 50Ω output connection. The 5-mV/mA output feeds a low-noise ×100, 50Ω input amplifier. An oscilloscope with a high-sensitivity plug-in monitors the amplifier's terminated output. A 1V pulse driving a known resistor value, R, provides a simple way to source calibrated current into the transformer.

If R=10 kΩ, the resultant pulsed current is 100 μA. The waveform is crisp and essentially noise-free, and it agrees with predicted amplitude. More sensitive measurement involves determining the test setup's noise floor. Measurements taken with no current flowing in the transformer indicate a noise limit of approximately 10 μA p-p. Most of this noise is due to the ×100 amplifier. If R= 100 kΩ, the pulsed current level is 10 μA, and the scope-photo trace indicates a 10-μA amplitude (**Figure Bb**).

These measurement exercises and level of agreement determine the test setup's gain and noise performance. This information provides the confidence necessary to make a meaningful low-level current measurement.

TABLE A–CURRENT-PROBE-AMPLIFIER COMBINATIONS

Typical junction current (A)	Typical junction voltage (V)
0.1	0.83
0.2	0.96
0.3	1.08

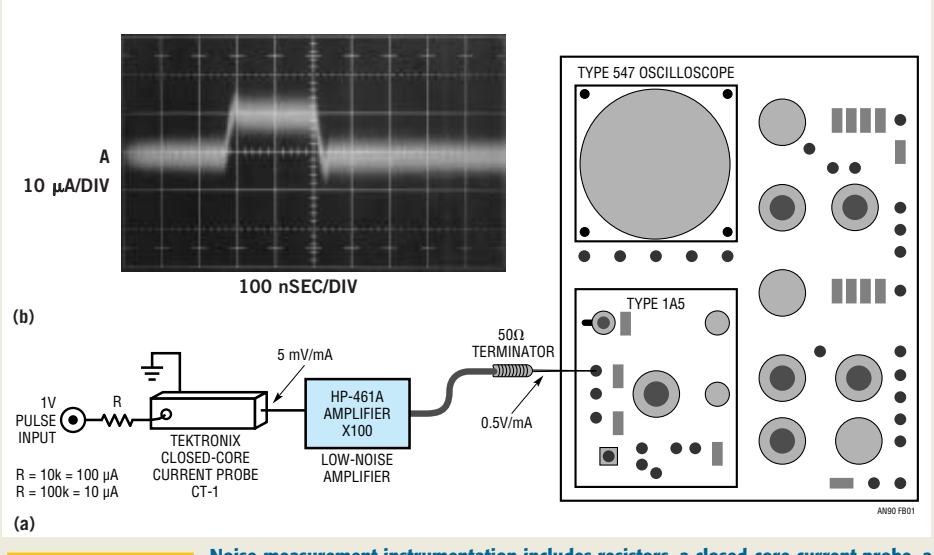


Figure B **Noise-measurement instrumentation includes resistors, a closed-core current probe, a low-noise wideband amplifier, and an oscilloscope (a). A 10-μA input pulse produces a calibrated and readily discernible output (b).**

REFERENCE

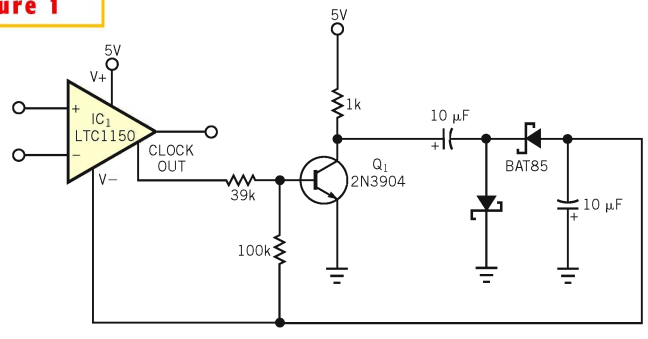
A. Hewlett-Packard Co, *Model 6181C Current Source Operating and Service Manual*, 1975.

Bootstrapping allows single-rail op amp to provide 0V output

Jim Williams, Linear Technology Corp, Milpitas, CA

Many single-supply-powered applications require amplifier-output swings within 1 mV—or even submillivolts—of ground. Amplifier-output-saturation limitations normally preclude such operation. **Figure 1**'s power-supply bootstrapping scheme achieves the desired characteristics with minimal parts count. IC_1, a chopper-stabilized amplifier, features a clock output. This output switches Q_1, providing drive to the diode-capacitor charge pump. The charge pump's output feeds IC_1's V− terminal, pulling it below 0V, thus permitting an output swing to and below ground. In **Figure 2**, the amplifier's V− pin (Trace B) initially rises at supply turn-on but heads negative when amplifier clocking commences at approximately midscreen. The circuit provides a simple way to obtain output swing to 0V, allowing a true "live-at-zero" output.

Figure 1



This configuration uses bootstrapping to allow a single-rail op amp to operate at 0V output.

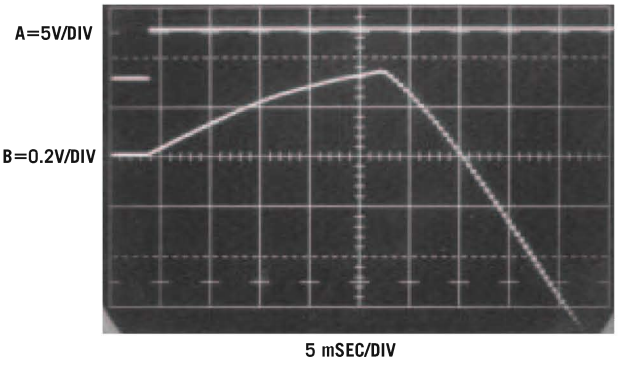


Figure 2 This start-up photo shows that the amplifier's V− pin (Trace B, midscreen) goes negative when the bootstrapping takes hold.

 By Jim Williams, Linear Technology Corp

FEEDING AND READING AN AVALANCHE PHOTODIODE TAKES A HIGH DEGREE OF CIRCUIT SOPHISTICATION.

Bias-voltage and current-sense circuits make avalanche photodiodes work

APDs (avalanche photodiodes) or APDs, are common components in laser-based fiber-optic systems for converting optical data into electrical form. The bias voltage and current measurement requirements constitute a significant design challenge, and common circuit approaches do not meet APD signal-conditioning requirements. More sophisticated techniques are necessary, particularly with any additional performance requirements for high-accuracy, low-noise, and digital outputs.

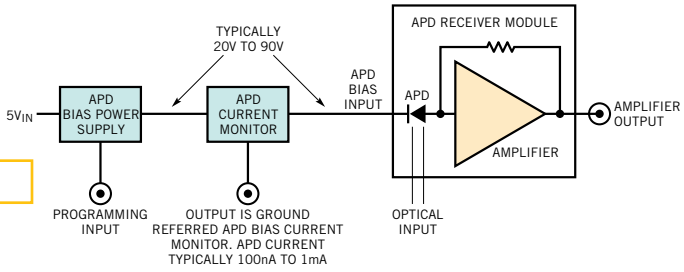


Figure 1

A typical APD module contains an APD, an amplifier, and an optical port. A power supply provides APD bias voltage, and an APD current monitor operates at a high common-mode voltage, complicating signal conditioning.

The usual APD package includes a signal-conditioning amplifier in a small module (**Figure 1**). The APD module contains the APD and a transimpedance (current-to-voltage) amplifier. An optical port permits interfacing fiber-optic cable to the APD's photosensitive portion. The module's compact construction facilitates a direct, low-loss connection between the APD and the amplifier, which is necessary because of the extremely high-speed data rates involved.

The receiver module needs support circuitry. The APD requires a relatively high voltage bias—typically, 20 to 90V—to operate. The bias supply's programming port sets this voltage. This programming voltage may also include corrections for the APD's temperature-dependent response. Additionally, it is desirable to monitor the APD's average current, which indicates optical signal strength. Feedback techniques can combine this information to maintain optical-signal strength at an optimal level. The feedback loop's operating characteristics can also determine whether deleterious degradation of optical components has occurred, permitting the circuit to take corrective measures. APD current is typically 100 nA to 1 mA, a dynamic range of 10,000 to 1. This measurement, which requires accuracy of at least 1%, normally must occur in the APD's "high side," which complicates the circuit design. This restriction applies because the APD's anode is committed to the receiver amplifier's summing point.

The APD module, an expensive and electrically delicate device, requires protection from damage under all conditions. The support circuitry must never produce spurious outputs, which could destroy the APD module. You must devote particular attention to the bias supply's dynamic

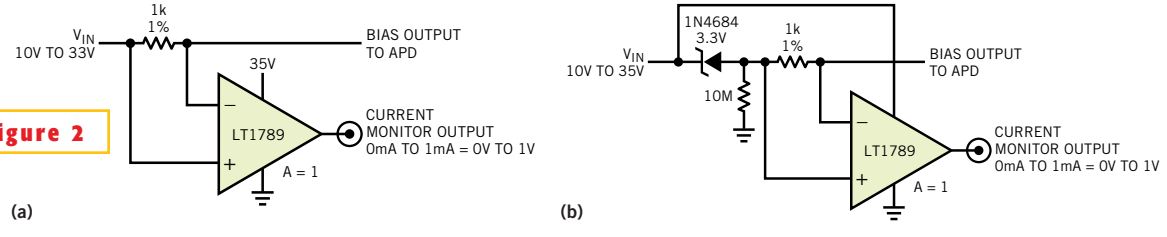


Figure 2

Instrumentation amplifiers extract current measurements from modest common-mode voltages but have limitations. One approach requires separate amplifier power and bias-supply connections (a); a similar approach derives both connections from a single point (b).

response under programming and power-up and -down conditions. Finally, it is desirable to power the support circuitry from a single 5V rail.

SIMPLE CURRENT MONITORS HAVE PROBLEMS

Straightforward approaches attempt to address the current-monitor problem (**Figure 2**). An instrumentation amplifier powered by a separate 35V rail measures current across the 1-kΩ shunt resistor (**Figure 2a**). A similar circuit derives its power supply from the APD bias line (**Figure 2b**). Although both approaches function, they do not meet APD current-sensing requirements. APD bias voltages can reach 90V, exceeding the amplifier's supply and common-mode-voltage limits. Additionally, the measurement's wide dynamic range requires the single-rail-powered amplifier to swing within 100 μV of zero, which is impractical. Finally, it is desirable for the amplifiers to operate from a single, low-voltage rail.

An alternative circuit divides down the high common-mode current-shunt voltage, theoretically permitting the 5V-powered amplifier to extract the current measurement over a 20 to 90V APD bias range (**Figure 3**). In practice, this arrangement introduces prohibitive errors, primarily because the circuit also divides down the desired signal. The current-measurement information is buried in the divider resistor's tolerance, even with 0.01% components. The circuit cannot achieve the desired 1% accuracy over a 100-nA to 1-mA range. Finally, although the amplifier operates from a single 5V supply, it cannot swing all the way to zero.

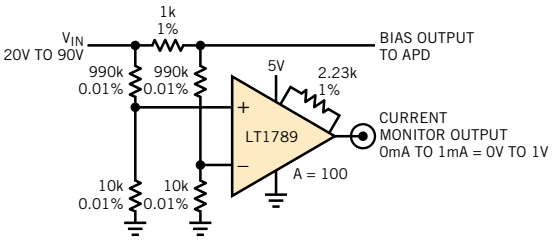


Figure 3 **Dividing down the high-common-mode voltage introduces huge errors, even with precision components, making this approach impractical.**

AC-carrier-modulation techniques help to meet APD current-monitor requirements (**Figure 4**). This circuit features 0.4% accuracy over the sensed current range, runs from a 5V supply, and has the high-noise-rejection characteristics of carrier-based "lock-in" measurements. Such measurements modulate the desired signal on a carrier, effecting narrowband amplification with extremely high out-of-band rejection.

An internal oscillator clocks the LTC1043 switch array. Oscillator frequency, set by the 0.56-μF capacitor at pin 16, is approximately 150 Hz. S_1 clocking biases Q_1 via level shifter Q_2. Q_1 chops the dc voltage across the 1-kΩ current shunt, modulating it into a differential square wave signal, which feeds instrumentation-amplifier IC_1 through 0.2-μF ac coupling capacitors. IC_1's single-ended output biases demodulator S_2, which presents a dc output to buffer amplifier IC_2. IC_2's output is the circuit output.

Switch S_3 clocks a negative-output charge pump that supplies the amplifier's V− pins, permitting output swing to 0V and below . The 100-kΩ resistors at Q_1 minimize its on-resistance error contribution and prevent destructive potentials from reaching IC_1 (and the 5V rail) if either 0.2-μF capacitor fails. IC_2's gain of 1.1 corrects for the slight attenuation introduced by IC_1's input resistors. In practice, it may be desirable to derive the APD bias voltage regulator's feedback signal from the indicated point, eliminating the 1-kΩ shunt resistor's voltage drop (see **sidebar** "Low-error feedback-signal-derivation techniques). Verifying accuracy involves loading the APD bias line with 100 nA to 1 mA and noting output agreement. Appropriate high-value load resistors, perhaps augmented with a monitoring current meter, are available from Victoreen (www.ohmite.com/victoreen/) and other suppliers. Tight resistor tolerance, although convenient, is not strictly necessary because the current-meter indication sets the output target value.

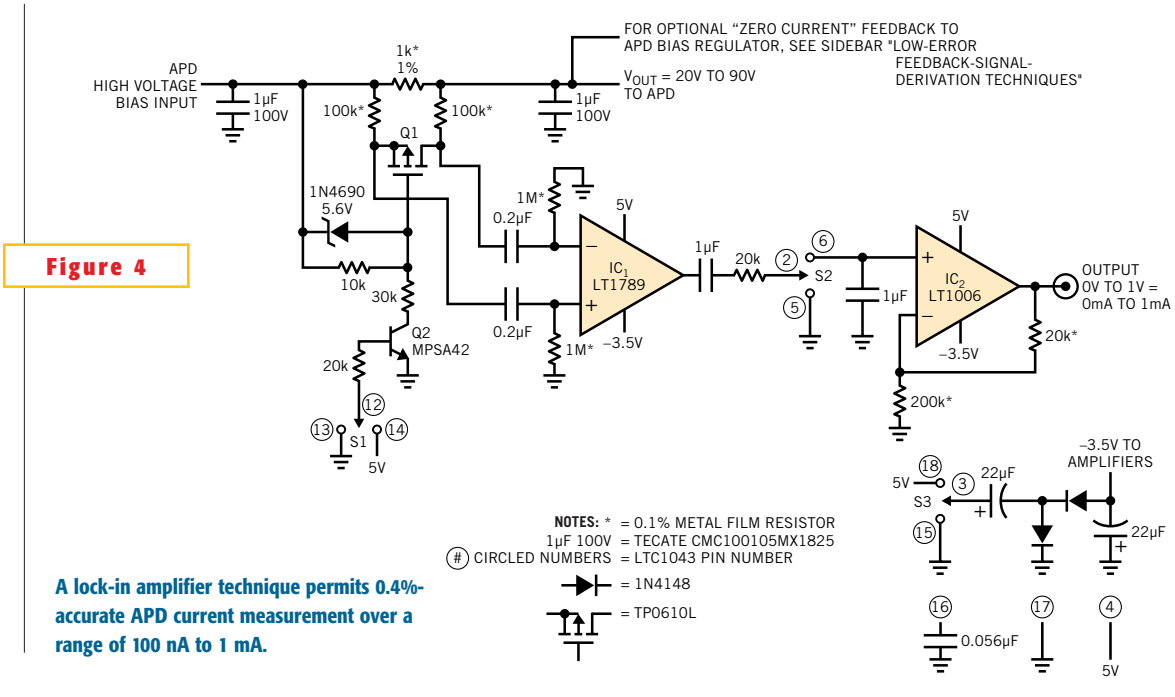


Figure 4 **A lock-in amplifier technique permits 0.4%-accurate APD current measurement over a range of 100 nA to 1 mA.**

A dc-coupled current monitor is simple but pulls more current from the APD bias supply (**Figure 5**). IC_1 floats, powered by the APD bias rail. The 15V zener diode and current source, Q_2, ensure that IC_1 never is exposed to destructive voltages. The 1-kΩ current shunt's voltage drop sets IC_1's positive input potential. Feedback via Q_1 to the negative input balances the inputs of IC_1. As such, Q_1's source voltage equals IC_1's positive input voltage, and its drain current sets the voltage across its source resistor. Q_1's drain current produces a voltage drop across the ground-referred 1-kΩ resistor identical to the drop across the 1-kΩ current shunt and, hence, the APD current. This relationship holds across the 20 to 90V APD bias-voltage range. The 5.6V zener diode assures IC_1's inputs are always within their common-mode operating range, and the 10-MΩ resistor maintains adequate zener current when APD current is at very low levels.

Two output options are possible. IC_2, a chopper-stabilized amplifier, provides an analog output. Its output can swing to zero or lower because its V− pin is supplied with a negative voltage. To generate this potential, IC_2's internal clock activates a charge pump, which in turn biases IC_2's V− pin. (Circuit veterans exercise extreme wariness when they confront this type of bootstrapped biasing scheme (**Reference 1**).

A second output option substitutes an A/D converter, providing a serial-format digital output. This option requires no V− supply because, the LTC2400 ADC converts inputs to—and slightly lower than 0V.

Resistors at strategic locations prevent destructive failures. The 51-kΩ unit protects IC_1 if the APD bias line shorts to ground. The 10-kΩ resistor limits current to a safe value if Q_1 fails, and the 100-kΩ resistor serves a similar purpose if Q_2 malfunctions. As in **Figure 4**, the circuit can take APD voltage-regulator feedback at the current shunt's output to maintain optimal regulation (see **sidebar** "Low-error

LOW-ERROR FEEDBACK-SIGNAL-DERIVATION TECHNIQUES

Various circuits either detail or make reference to counteracting loading effects of the APD (avalanche-photodiode) bias supply's output feedback divider. If the divider location is before the 1-kΩ current shunt, the current monitor's output does not include its current drain, and the circuit incurs no error. A potential difficulty with this approach is that the 1-kΩ shunt appears in series with the bias supply's output, degrading load regulation. The maximum 1-mA shunt current produces a 1V output-regulation drop. In some cases, this drop is permissible, and no further consideration is necessary. Circumstances dictating tighter load regulation require compensation techniques.

When the shunt is in a transformer's return path ("low-side shunt"), you can cancel divider error by introducing a compensatory term into the APD current-monitor circuitry (**Figure A**). This scheme prevents the output-voltage divider's current-loading error from appearing in IC_1's output by feeding forward a compensatory current from the APD bias-programming input. The circuit scales the compensating current, arriving at IC_1 via R_{LARGE}, to precisely balance out the portion of shunt output that the voltage divider's loading error contributes.

The situation differs when the shunt resides in the "high side." Such arrangements involve high common-mode voltages, seemingly mandating a high-voltage buffer amplifier to isolate the divider's current loading. However, you can alternatively use standard low-voltage amplifiers to process high-voltage signals (**Figure B**). IC_1, sensing after the 1-kΩ shunt, isolates the feedback divider's loading while permitting the APD bias regulator to include the shunt within its feedback loop.

The bias regulator's high-voltage output directly powers IC_1, but the zener diode clamps the IC's V− pin with respect to its V+ pin. Current sink Q_1 maintains this bias over the range of possible APD-regulator outputs. Although IC_1 processes high-voltage signals, the circuit holds the voltage across it to safe levels. The 5.6V zener diode in the APD bias line ensures that IC_1's inputs are always inside their common-mode operating range. The 10-MΩ resistor maintains adequate zener-diode bias when APD currents are extremely low. A 51-kΩ resistor protects IC_1 from destructive high voltage if the APD bias output shorts to ground. Similarly, the 100-kΩ resistor prevents high voltage from appearing on the 5V supply if Q_1 fails.

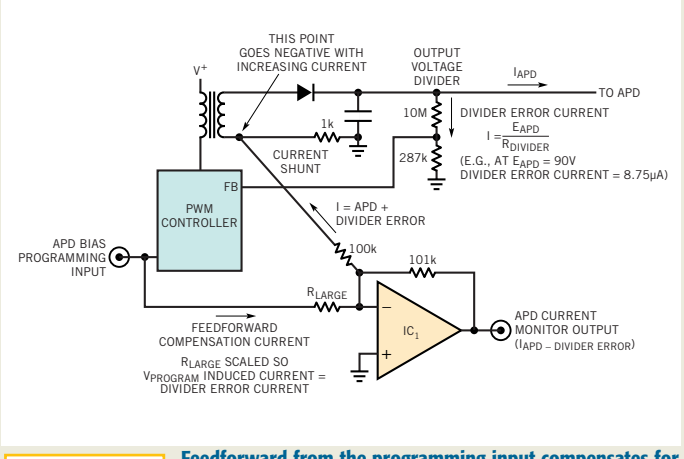


Figure A Feedforward from the programming input compensates for the output voltage divider's current-loading error.

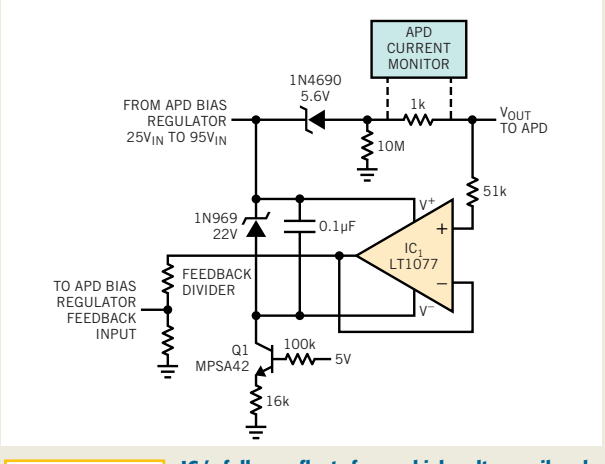


Figure B IC_1's follower floats from a high-voltage rail and eliminates feedback-divider current-loading error.

feedback-signal-derivation techniques). This circuit requires no trimming and maintains 0.5% accuracy. It does, however, pull current approximately equal to the current delivered to the APD, in addition to Q_2's collector current. This current can be an issue if the APD bias supply has restricted current capability.

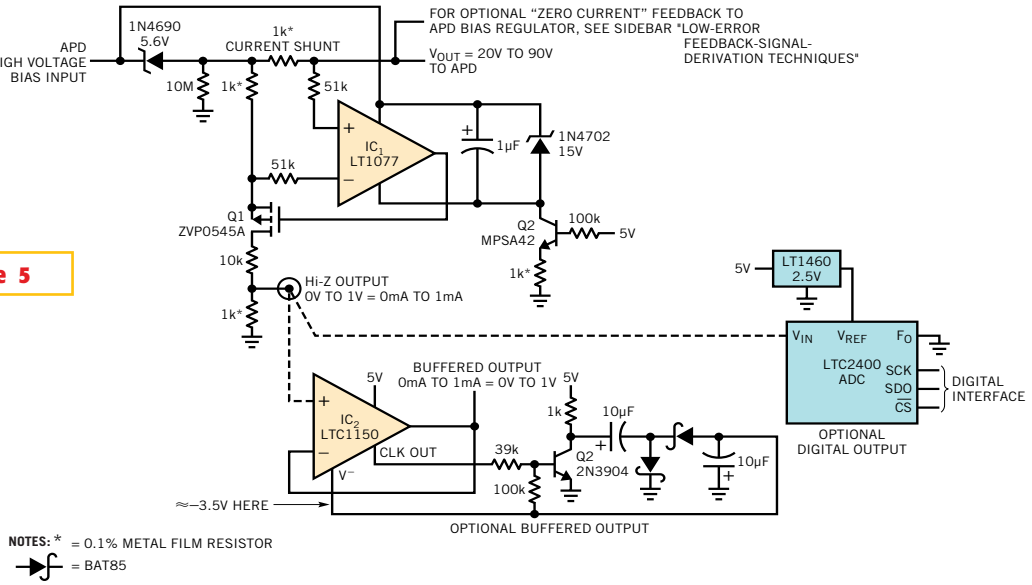


Figure 5

IC_1 and Q_1 float at the high-voltage rail and measure APD current to 0.5% via the 1-kΩ shunt. Q_1's ground-referred drain current provides a high-impedance output, but you can also choose a buffered-analog or digital-output option.

All these examples are current monitors. The circuit in **Figure 6a**, which Linear Technology application engineer Michael Negrete developed is a high-voltage APD bias supply (**Reference 2**). The LT1930A switching regulator and L_1 form a flyback-based boost stage. The flyback events pump a diode-capacitor network tripler, producing a high-voltage dc output. Feedback from the output via the R_1-R_2 combination stabilizes the regulator's operating point. D_6 and D_7 protect the switch and feedback pins, respectively, from parasitic negative excursions, and the 10Ω resistors prevent excessive switch current. C_8 and C_9, series-connected for high-voltage capability, minimize output noise. A 0 to 4.5V programming voltage results in a corresponding 90 to 30V output with 3% accuracy and approximately 2 mA of current capacity.

Circuit output noise is quite low (**Figure 6**). With 500 µA loading at V_{OUT}=50V, the ripple and harmonic residue in a 10-MHz bandwidth is approximately 200 µV. This noise level is adequate for most APD receivers.

ADD A CURRENT MONITOR

Figure 7, named the Martin configuration for work by Alan Martin, an application engineer at Linear Technology, combines the previous circuit with **Figure 5**'s current monitor, providing a complete APD signal conditioner. The programmable APD bias supply is as before, except that feedback comes via IC_2. IC_2, sensing after the 1-kΩ current shunt, isolates the R_1-R_2 path loading, preventing loading from influencing the shunt's voltage drop. IC_2's action also ensures tight output regulation, despite the current shunt's presence (see **sidebar** "Low-error feedback-signal-derivation techniques").

The current monitor borrowed from **Figure 5** measures across the 1-kΩ current shunt, presenting its output in Q_1's drain line. The output has an output impedance of approximately 1-kΩ, but you can also use one of **Figure 5**'s output options.

When considering circuit operation, note that the charge pump's high-voltage

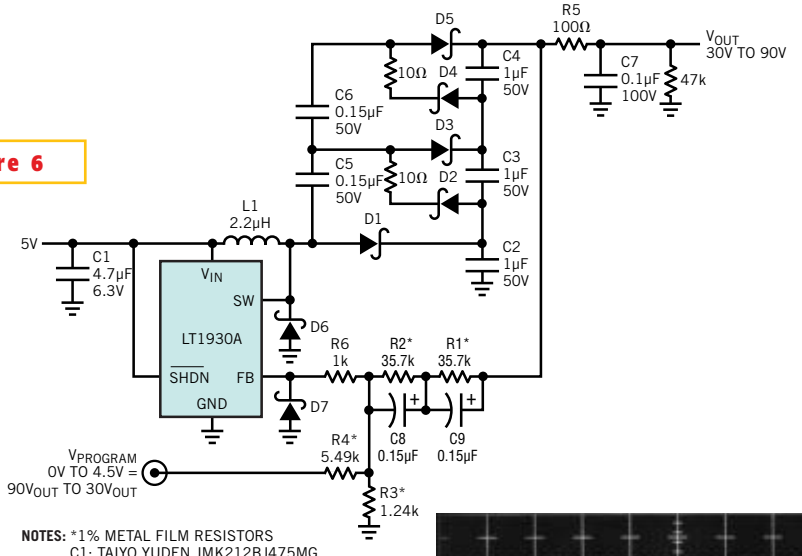


Figure 6

A boost regulator and charge pump supply APD bias of 30 to 90V (a) with only 200 µV p-p ripple and harmonic residue in a 10-MHz bandwidth (b).

output powers both amplifiers, and the circuit returns its V− pins to the "2/3 V_{OUT}" point. This biasing permits the amplifiers to process high-voltage signals, although the voltage across them never exceeds 30V.

Another complete APD bias supply and current monitor uses techniques that differ from the previous example's (**Figure 8a**). Advantages include 0.25% bias voltage and current-monitoring accuracy, compactness, and fewer high-voltage components for greater reliability. The LT1946 switching regulator and T_1 form a flyback-type boost configuration. T_1's turn ratio provides voltage gain, and the diode and capacitor in T_1's secondary winding rectify and smooth the high-voltage flyback events to dc. The circuit divides down this dc potential and feeds the resultant signal back to IC_1. IC_1 compares this signal with the APD-bias programming input and sets the LT1946's operating point, closing a control loop. A local roll-off at IC_1 and a lead network across the 10-MΩ feedback resistor furnish loop compensation. This loop establishes and maintains the APD bias output in accordance with the programming input's value. IC_3, active at V_{SUPPLY}=1.2V, prevents output overshoot at power turn-on by grounding the programming input command while forcing IC_1's output low. This action shuts off the switching regulator, which then stops producing a high voltage. When turn-on power reaches approximately 4V, IC_3 changes state, and IC_1's positive input ramps to the programming voltage. The switching regulator's output follows this turn-on profile, and no overshoot occurs. The LT1004 clamps spurious programming inputs beyond 2.5V, preventing excessive high-voltage outputs. Optional circuitry allows input clamping at any desired voltage (see **sidebar "APD protection circuits"**).

The circuit's current-monitor portion takes full advantage of T_1's floating secondary. Here, the 1-kΩ current shunt resides in T_1's secondary return path (Pin 3), eliminating the high common-mode voltages that the previous "high-side"-sensed examples encountered. Circuit ground is at the shunt's uncommitted terminal, meaning that Pin 3 of T_1 undergoes increasing negative excursions with greater APD current. Inverter IC_2 converts the shunt's negative voltage to a buffered positive output. IC_2's gain, which the circuit scales 1% above unity, compensates for the input resistor's shunt-loading error. The circuit facilitates a voltage swing to zero by returning IC_2's V− pin to a small negative potential derived from the LT1946's V_{SW} pin switching. A compensatory current from the APD bias-programming input prevents the 10-MΩ/287-kΩ divider's current-loading er-

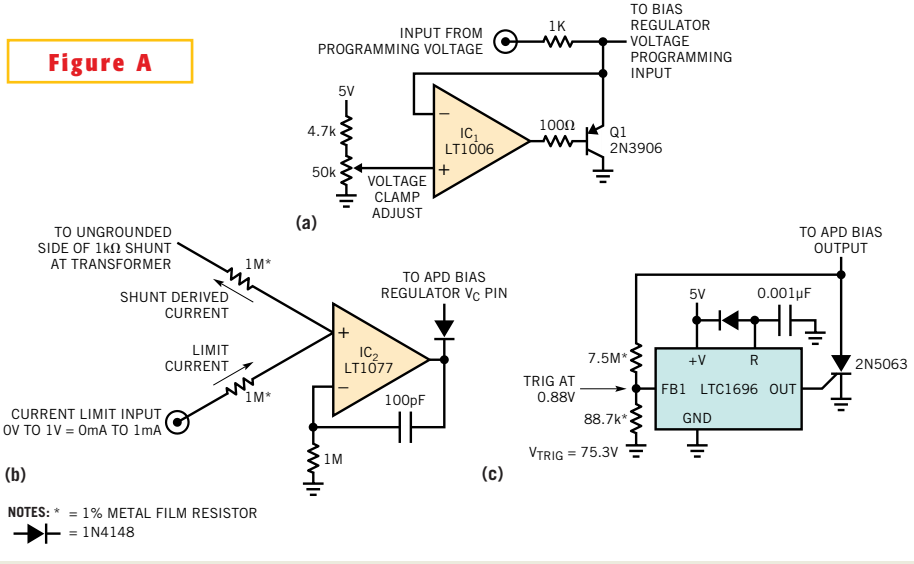
APD-PROTECTION CIRCUITS

APD (avalanche-photodiode)-receiver modules are electrically delicate and expensive devices. Thus, protection circuits may be of interest. Protection circuits can protect the APD module from bias-programming overvoltage error (**Figure Aa**), excessive current (**Figure Ab**), or destructive voltage (**Figure Ac**). In **Figure Aa**, Q_1 is normally off, and programming voltage passes to the bias-regulator voltage-programming input. Abnormally high inputs, defined by the potentiometer's setting, cause IC_1 to swing low, biasing Q_1 and closing IC_1's feedback loop. This situation causes Q_1's emitter to clamp at the potentiometer wiper's voltage, safely limiting the bias regulator's programming input.

Figure Ab is an APD current limiter. The circuit works with "low-side" shunts in transformer-coupled APD supplies, such as in **Figure 8a** of the main text, although the technique is generally applicable. As long as the shunt current's absolute value is below the current limit point, IC_2 is saturated high, and the associated APD bias regulator functions normally. Shunt overcurrent forces IC_2's output lower, pulling the regulator's control pin (V_C) lower and limiting current. The 100-pF/1-MΩ combination stabilizes IC_2, and the bias regulator assumes the characteristics of a current source.

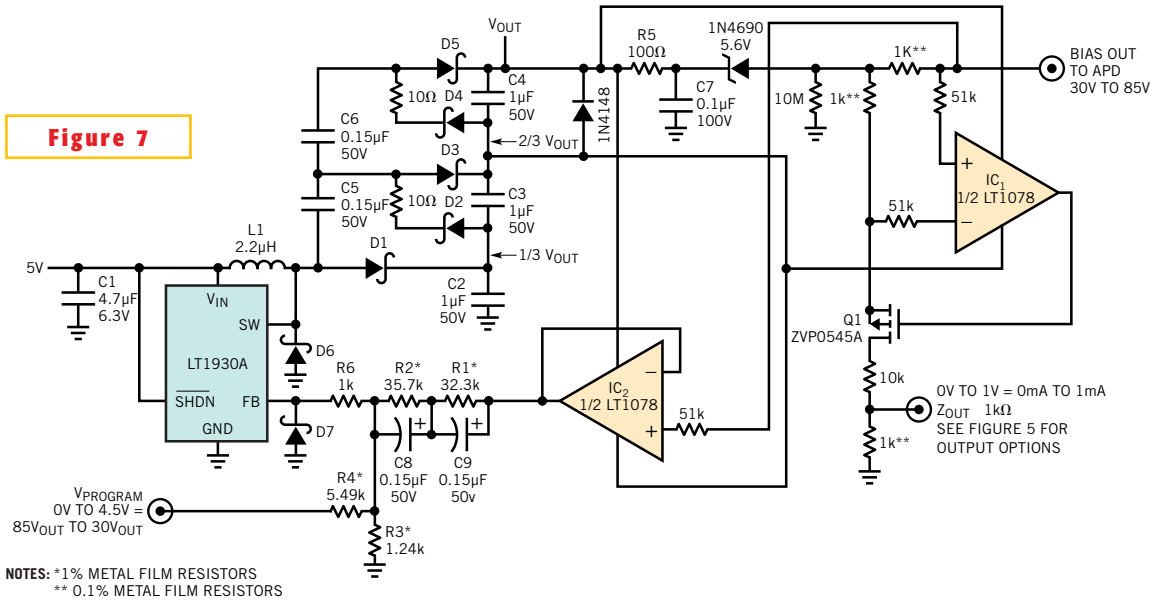
Figure Ac is an overvoltage crowbar. This circuit's purpose is as the last line of defense against uncontrolled APD bias-supply high-voltage outputs. Normally, the LTC1696 crowbar IC is below its 0.88V trigger threshold, and the SCR is off. If the APD bias rises too high, the LTC1696 triggers, firing the SCR. SCR turn-on "crowbars" the APD bias line, arresting the high voltage and maintaining a short across the line via its latch characteristic. If the APD bias supply has significant output impedance, prolonged SCR loading is not deleterious; if not, you should put a fuse in the bias supply line.

Figure A



Protection-circuit options include a programming-voltage clamp (a), a current limiter (b), and a bias-voltage crowbar (c).

Figure 7



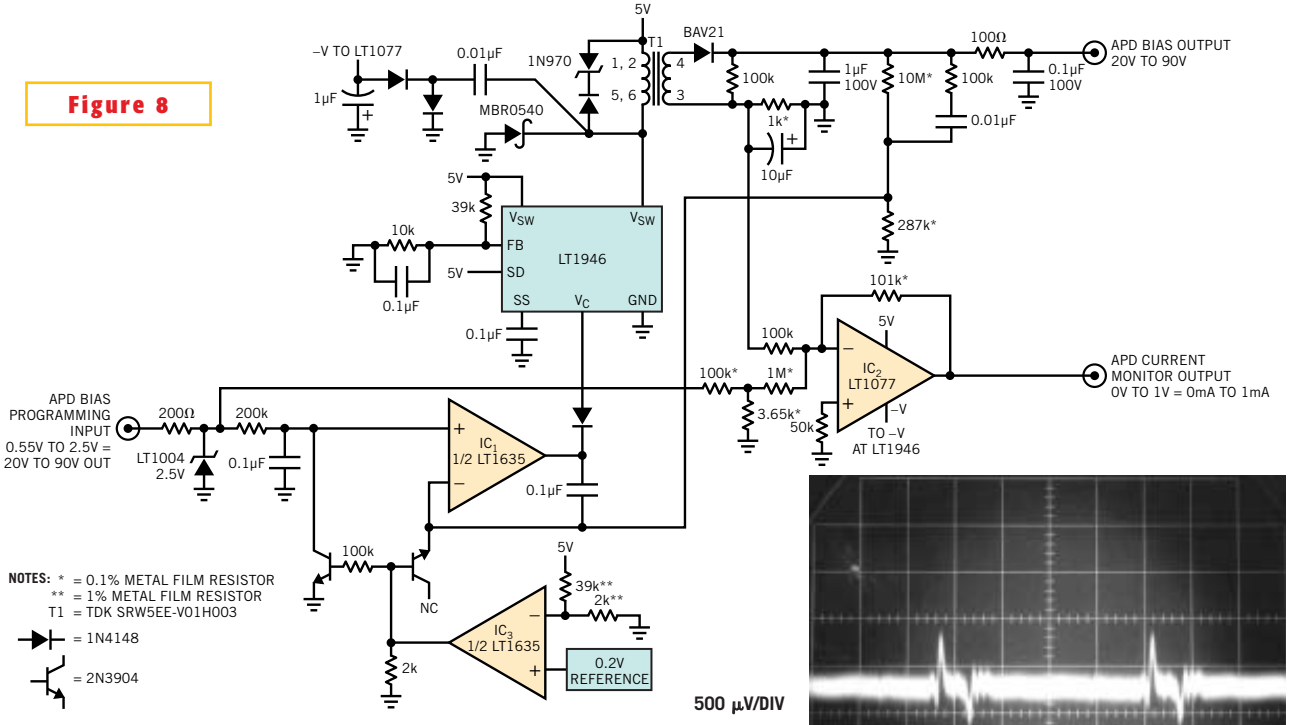
NOTES: *1% METAL FILM RESISTORS
** 0.1% METAL FILM RESISTORS
C1: TAIYO YUDEN JMK212BJ475MG
C2 TO C4: MURATA GRM42-2X7R105K050
C7: TAIYO YUDEN HMK316BJ104ML
C8, C9: VISHAY 695D154X9050AZ
D1 TO D7: CENTRAL SEMI CMDSH2-3TR
L1: MURATA LQH32C2R2M24

Figure 5's current monitor joins with Figure 6's bias supply to provide APD bias and 0.5% current measurement. IC_2 buffers the LT1930A's feedback-path loading from the bias supply's output, eliminating current error.

ror from appearing in IC_2's output. The circuit scales this compensating current, arriving at IC_2 via the 100-kΩ/3.65-kΩ/1-MΩ resistor network, to precisely balance out the shunt's output portion due to the 10-MΩ/287-kΩ path's loading error (see **sidebar** "Low-error feedback signal derivation techniques").

Output noise for this circuit is approximately 1 mV p-p in a 10-MHz bandwidth (**Figure 8b**). This noise level is characteristic of flyback regulators and somewhat

Figure 8



NOTES: * = 0.1% METAL FILM RESISTOR
** = 1% METAL FILM RESISTOR
T1 = TDK SRW5EE-V01H003
= 1N4148
= 2N3904

(a)

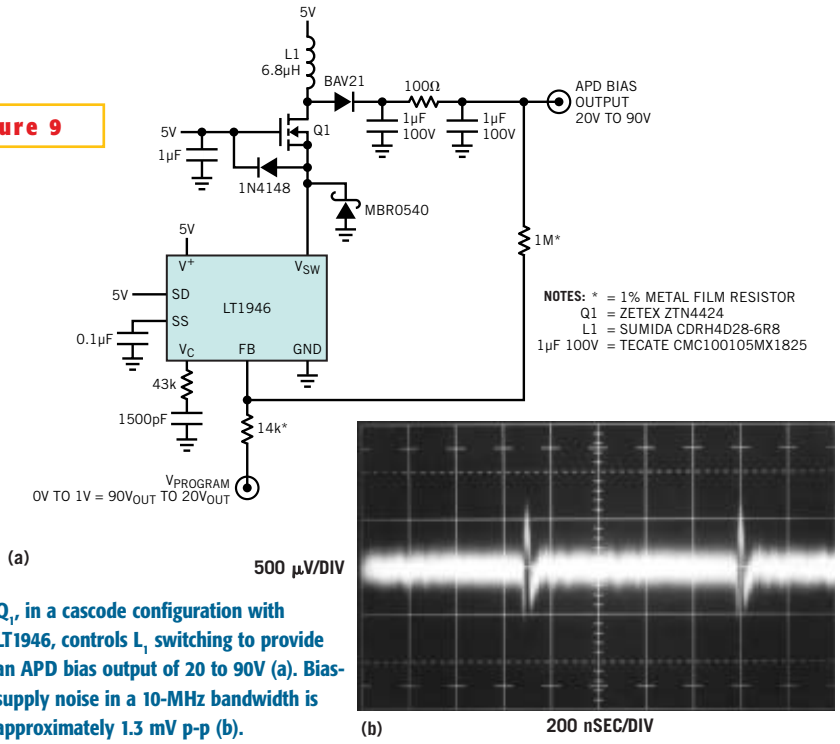
(b)

IC_1 controls an LT1946 boost regulator to provide a bias supply of 20 to 90V (a). IC_2 senses APD current to 0.25% across the 1-kΩ shunt in T_1's output return. Output noise measures 1 mV p-p in a 10-MHz bandwidth (b).

higher than **Figure 7**'s charge-pump-based arrangement. This noise is still acceptable for most APD receivers, although special switching-regulator techniques can considerably reduce this figure.

You can borrow from **Figure 8**'s flyback technique to form a simple, small-area APD bias supply (**Figure 9a**). This circuit provides only the bias supply and deletes **Figure 8a**'s current-monitor function. Additionally, a two-terminal inductor replaces **Figure 8a**'s transformer. The circuit is a basic-inductor flyback boost regulator with a single important deviation. Q_1, a high-voltage device, sits between the LT1946 switching regulator and the inductor, which permits the regulator to control Q_1's high-voltage switching without undergoing high-voltage stress. Q_1, operating as a cascode with the LT1946's internal switch, withstands L_1's high-voltage flyback events (**Reference 3**). The diodes associated with the source terminal of Q_1 clamp L_1-originated spikes arriving via Q_1's junction capacitance. The circuit rectifies and filters the high voltage to dc, forming the circuit's output. Feedback to the regulator stabilizes the output, which you can vary by appropriate biasing at the $V_{PROGRAM}$ input. Components at the LT1946's V_C pin compensate the loop. Over a 20 to 90V-output range, the circuit remains within 2% of the $V_{PROGRAM}$ input's dictated output voltage. Switching-related output noise is approximately 1.3 mV p-p in a 10-MHz bandwidth (**Figure 9b**).

Figure 9

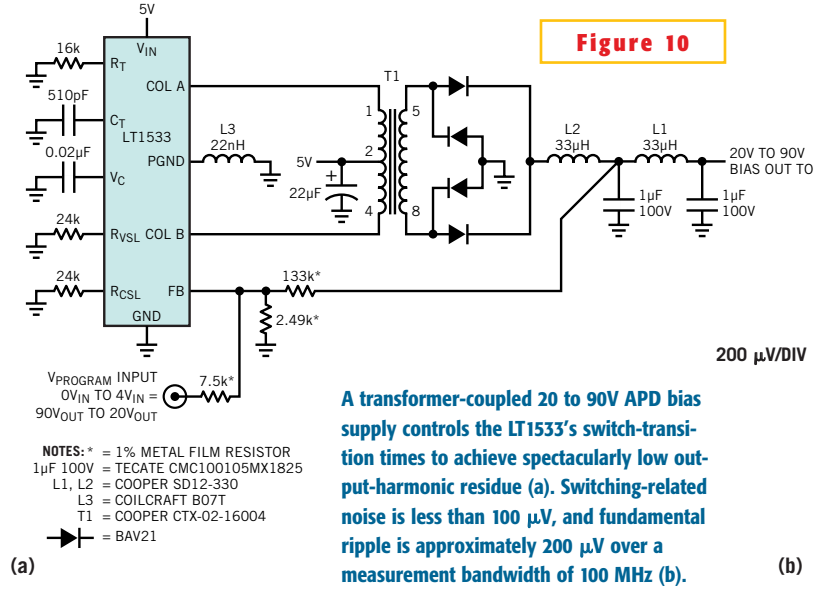


Q_1, in a cascode configuration with LT1946, controls L_1 switching to provide an APD bias output of 20 to 90V (a). Bias-supply noise in a 10-MHz bandwidth is approximately 1.3 mV p-p (b).

Some APD-receiver applications require extremely low noise in an extended bandwidth. An APD bias supply can use special switching regulator techniques to achieve 200-µV noise in a 100-MHz bandwidth (**Figure 10a**). The LT1533 is a "push-pull" output-switching regulator with controllable switch-transition times. Slower switch transitions notably reduce output harmonic content, or "noise." Noise contains no regularly occurring or coherent components. As such, switching-regulator output noise is a misnomer. Unfortunately, undesired switching-related components in the regulated output are almost always called noise. Accordingly, although technically incorrect, this article refers to all undesired output signals as "noise" (**Reference 4**).

Resistors at the R_{CSL} and R_{VSL} pins con-

Figure 10



A transformer-coupled 20 to 90V APD bias supply controls the LT1533's switch-transition times to achieve spectacularly low output-harmonic residue (a). Switching-related noise is less than 100 µV, and fundamental ripple is approximately 200 µV over a measurement bandwidth of 100 MHz (b).

trol the switch current and voltage-transition times, respectively. In all other respects, the circuit behaves as a classical push-pull, transformer-based, step-up converter. The $V_{PROGRAM}$ input biases a feedback loop, setting the output at 20 to 90V.

The controlled transition times result in a dramatic decrease in output noise (**Figure 10b**). The ripple and switching-related residue of 200 µV in a 100-MHz bandwidth is much less than that of conventional regulators, meeting the most stringent noise requirements.

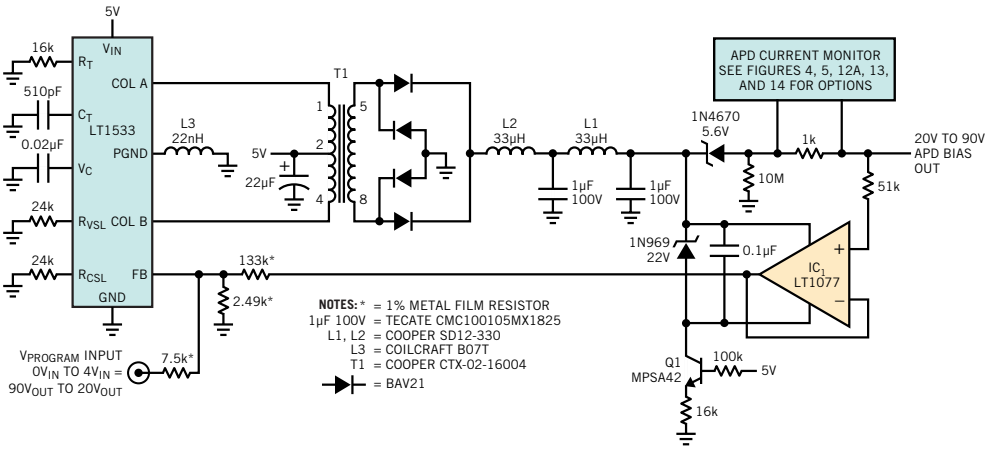
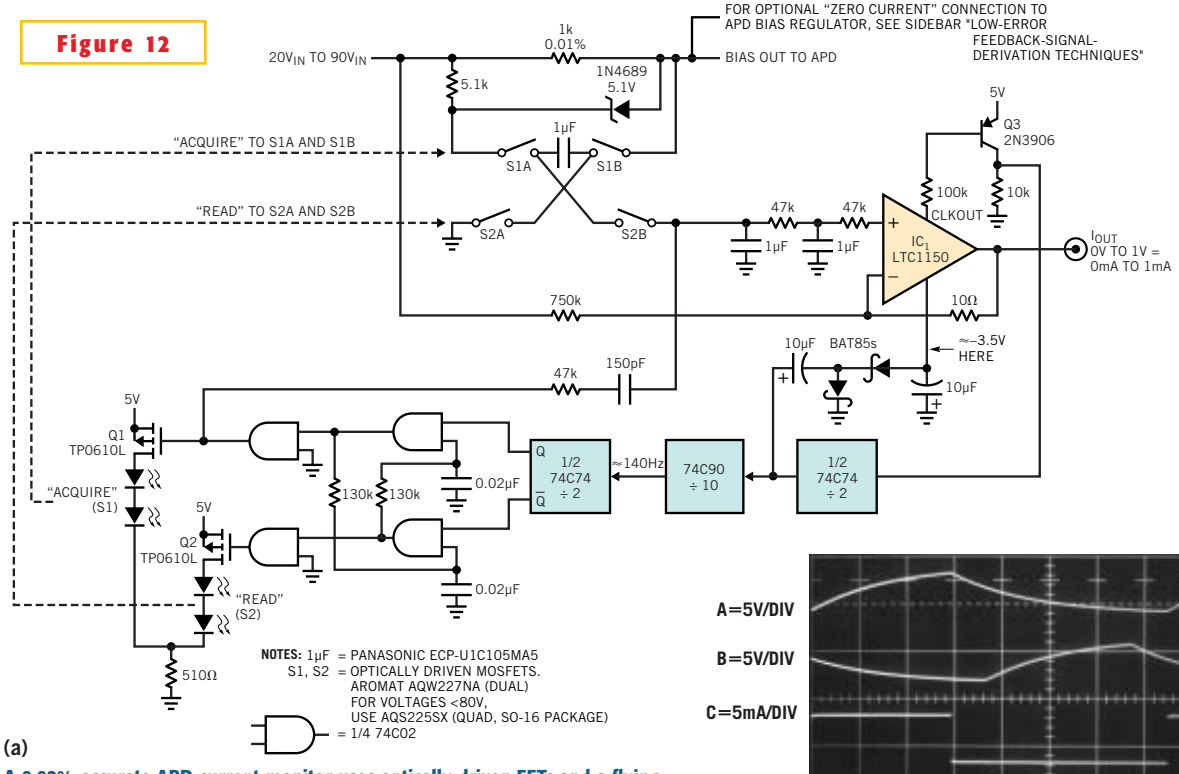


Figure 11 **Augmenting Figure 10a with a feedback-divider buffer and a current monitor provides a complete APD signal conditioner with 100 µV of noise.**

You can build on the previous circuit's performance to form a complete, high-performance APD-signal conditioner (**Figure 11**). The bias supply is identical to **Figure 10a**'s low-noise example, with the addition of the IC_1-based feedback buffer. This stage, similar to the one in **Figure 7**, isolates the regulator's feedback-path current from the 1-kΩ shunt, preserving current-monitor accuracy. IC_1's zener-current source-power biasing scheme permits this amplifier to process high-voltage signals even though it is a low-voltage device (see **sidebar** "Low-error feedback-signal-derivation techniques"). You can select the current monitor for this circuit, which the schematic shows in block form, from many circuits, depending on requirements.

Some APD current-monitor applications call for high accuracy and stability. An unusual optical-switching-based approach achieves 0.02% accuracy over a sensed range of 100 nA to 1 mA (**Figure 12a**). This scheme measures shunt current by switching a capacitor using switches S_{1A} and S_{1B} across the shunt ("ACQUIRE"). After a time, the capacitor charges to the voltage across the shunt. S_{1A} and S_{1B} open, and S_{2A} and S_{2B}

Figure 12

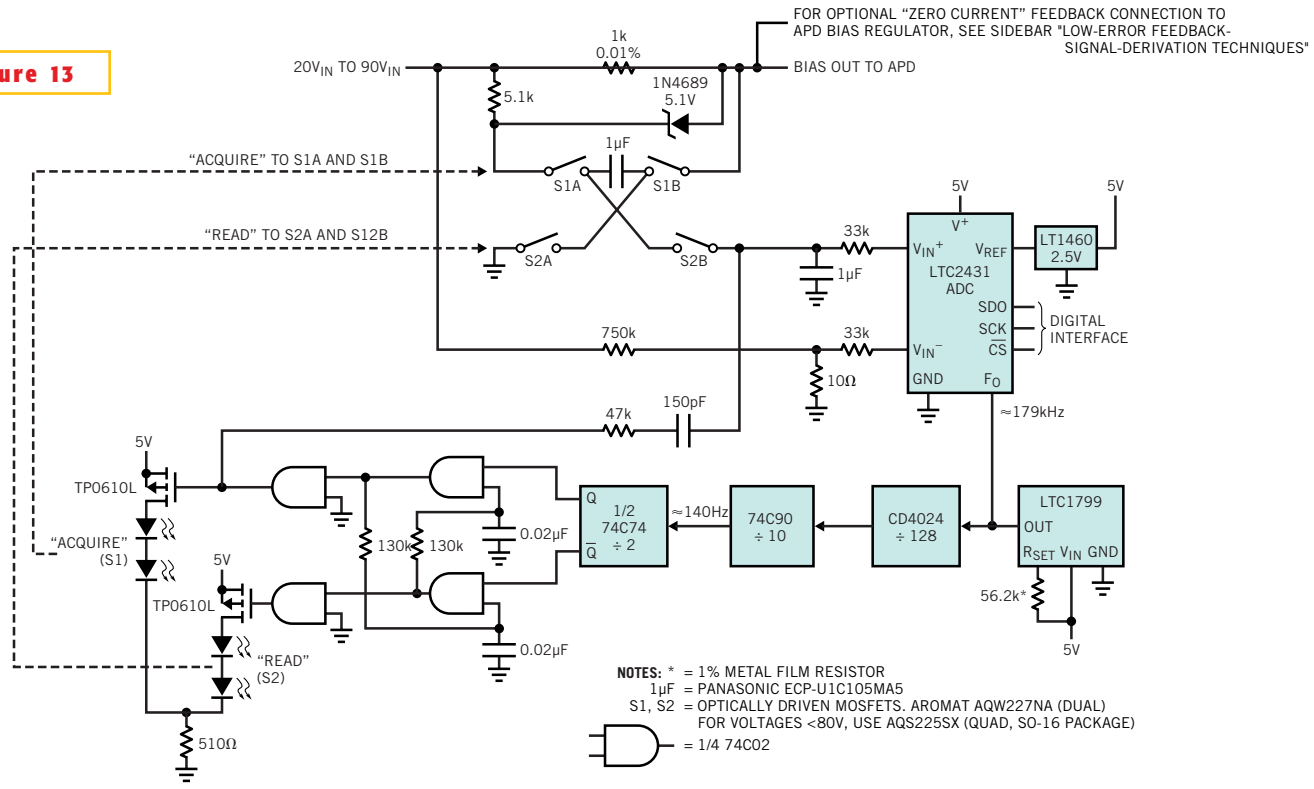


(a)

(b)

A 0.02%-accurate APD current monitor uses optically driven FETs and a flying capacitor (a). Clocked, cross-coupled capacitors (traces A and B) in 74C02-based network result in nonoverlapping drive (traces C and D) to S_1's and S_2's actuating LEDs (b).

Figure 13



Adding an A/D converter to Figure 12a's optically driven FET-based current monitor provides for a digital output with 0.09% accuracy.

close ("READ"). This action grounds one capacitor plate, and the capacitor discharges into the grounded 1-µF unit at S_{2B}. This switching cycle continuously repeats, resulting in IC_1's ground-referred positive input, assuming that the same voltage that is across the floating 1-kΩ shunt. The specified LED-driven MOSFET switches have no junction potentials, and the optical drive contributes no charge-injection error. A nonoverlapping clock prevents simultaneous conduction in S_1 and S_2, which would result in charge loss, causing errors and possible circuit damage. The 5.1V zener diode prevents switched-capacitor failure if the bias output shorts to ground.

IC_1, a chopper-stabilized amplifier, has a clock output. After level-shifting and buffering by Q_3, this clock drives a logic-divider chain. The first flip-flop activates a charge pump, pulling IC_1's V− pin negative, which permits amplifier swing to and below 0V. This scheme is a variant of the one in **Figure 5**. The divider chain terminates into a logic network. This network provides phase-opposed charging of the 0.02-µF capacitors (traces A and B in **Figure 12b**). The circuit arranges the gating associated with these capacitors, so the logic provides nonoverlapping, complementary biasing to Q_1 and Q_2. These transistors supply this nonoverlapping drive to the S_1 and S_2 actuating LEDs (traces C and D).

The extremely small parasitic-error terms in the LED-driven MOSFET switches result in nearly theoretical circuit performance. However, S_{1A}'s high-voltage switching, which pumps S_{2B}'s 3- to 4-pF junction capacitance, causes residual error of approximately 0.1%. This error results in the transfer of a slight quantity of unwanted charge to the 1-µF capacitor at S_{2B}. The amount of transferred charge varies with the APD bias voltage (20 to 90V) and, to a lesser extent, the varactorlike response of S_{2B}'s off-state capacitance. The feedforward of dc components to IC_1's negative input and ac feedforward from Q_1's gate to S_{2B} partially cancels these terms. The corrections compensate error by a factor of five, resulting in 0.02% accuracy.

Optical-switch failure could expose IC_1 to high voltage, destroying it and possibly presenting destructive voltages to the 5V rail. The 47-kΩ resistors in IC_1's positive input prevent this unwelcome state of affairs.

ADD DIGITAL OUTPUTS

You can modify many of these circuit types to have digital outputs. An optically based current monitor with a digital output (**Figure 13**) is essentially identical to **Figure 12a** with two significant differences. In this case, the LTC2431 A/D converter supplies a digital output. The converter's differential inputs allow the same feedforward-based error correction as in the previous example. The divider-chain countdown ratio is different to accommodate a higher speed clock, which the LTC1799 oscillator supplies. This higher speed clock, which times the converter's operation, centers the ADC's internal notch filter at the optical switches' commutation frequencies to maximize rejection. The LTC2431's internal digital filter's first null occurs at 1/2560 of the frequency at the F_0 pin. (See the data sheet for more details.)

This circuit's 0.09% accuracy does not equal the previous analog output's version because of the LT1460 reference's 0.075% tolerance, which you cannot

trim. You can adjust the circuit to 0.02% accuracy by trimming the 1-kΩ shunt so that the measured output current directly corresponds to the A/D output.

The current-monitor in **Figure 13** furnishes a digital output from a ground-referenced A/D converter fed from analog level-shifting stages. Alternatively, **Figure 14** directly digitizes shunt current by floating the converter in the APD bias line. The circuit level-shifts the A/D output in the digital domain, presenting ground-referred digital data. This simple approach is attractive, although the available APD bias supply must supply approximately 3 mA to the A/D converter and its attendant circuitry.

The LTC2410 and its LT1029 reference receive power directly from the high-voltage APD bias-supply input. Current sink Q_3 and the LT1029 bias the LTC2410 V− pin, maintaining 5V across the converter over the 20 to 90V bias-rail range. The converter's differential inputs measure across the 1-kΩ current shunt. Resistors and a zener-diode clamp protect the converter from excessive voltages if the APD bias line shorts to ground. The digital outputs, floating at high voltage, drive level-shift circuits that provide ground-referred data. The schematic shows one of the two identical stages and another in conceptual form. The design of the level-shift stage provides for low-quiescent and dynamic current consumption and maintains data fidelity. This type of design is necessary to minimize current drain from the APD bias supply and to avoid modulating the supply with transient loading artifacts. High-voltage common-emitter Q_1 sources current to Q_2, which provides a ground-referred, logic-compatible output. Capacitive feedforward maintains data-edge speed and minimizes standing current requirements.

This circuit's 0.25% untrimmed accuracy is due to shunt and LT1029 tolerances. Trimming the LT1029 permits

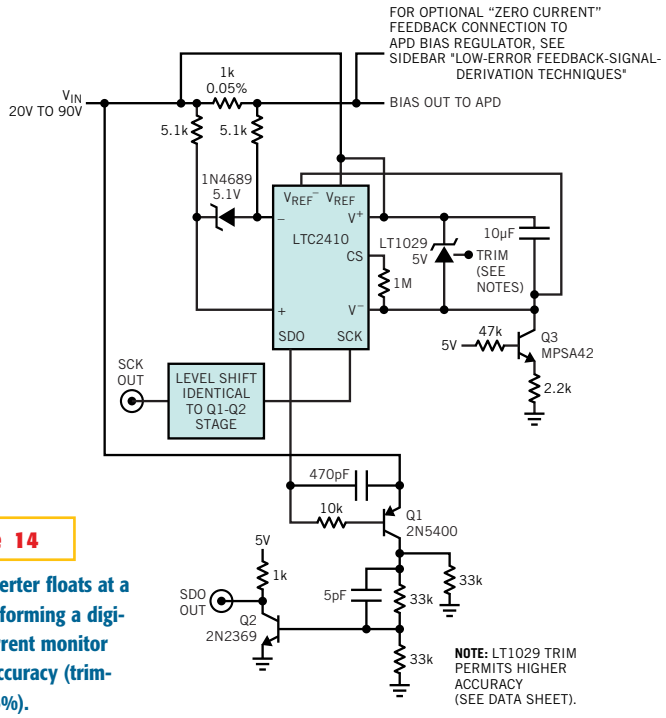
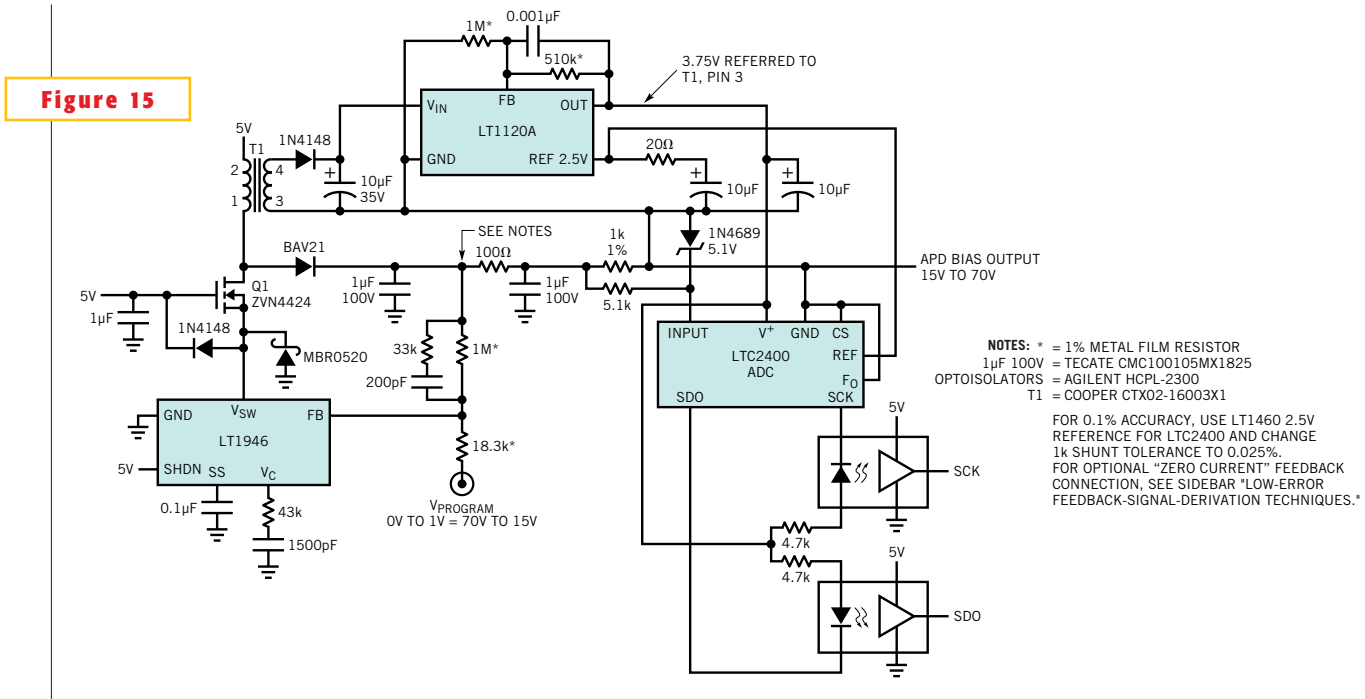


Figure 14

The A/D converter floats at a high voltage, forming a digital-output current monitor with 0.25% accuracy (trimmable to 0.05%).

Figure 15



In this APD bias supply with digital-output 2%-accurate current monitor, T_1's primary winding supplies the APD high-voltage source, and the secondary winding furnishes power to the floating circuitry.

higher accuracy of 0.05% (see data sheet).

Figure 15 also floats an A/D converter across the shunt and includes an APD bias supply. The LT1946 switching regulator and Q_1, operating in nearly identical fashion to **Figure 9a**'s circuit, generate the bias supply. The primary difference is that a transformer replaces **Figure 9a**'s inductor. The transformer's primary winding furnishes high-voltage step-up, similar to the one in **Figure 9a**. The floating secondary drives an isolated LT1120-based 3.75V regulator. This floating regulator's output, stacked on top of the APD bias line, powers the LTC2400 ADC. The isolated 3.75V supply permits the A/D converter to measure across the 1-kΩ shunt without pulling operating power from the APD supply. Resistive current limiting and the 5.1V zener diode protect the converter from high voltage if the APD bias output shorts to ground. Low-power optoisolators provide ground-referred digital output and eliminate floating-supply "starve-out" due to cross-regulation interaction with the APD-regulation loop. Specifically, low-power APD bias outputs could result in insufficient transformer flux to furnish the floating supply's loading requirements. Common optoisolators require significant current, mandating the specified low-power types. The previous circuit's discrete level-shift stage would draw even less power, but the optoisolators are simple and adequate.

The LT1120 2.5V reference and 1-kΩ shunt tolerances dictate 2% circuit accuracy. If you use the tighter tolerance components noted in the schematic, 0.1% accuracy is practical.

A table in the Web version of this article summarizes all of the previous circuits (www.ednmag.com). The chart reviews salient features, but such brevity breeds oversimplification. No substitute exists for a thorough investigation of any application's requirements.□

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge, MA). Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

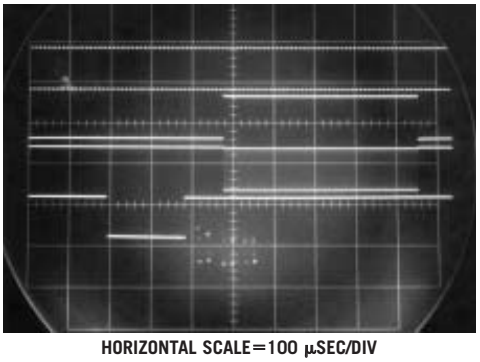
 By Jim Williams, Linear Technology Corp

IN ADDITION TO THEIR COMMON ROLE AS CLOCK SOURCES IN DIGITAL SYSTEMS, OSCILLATORS PLAY AN IMPORTANT ROLE IN INSTRUMENTATION APPLICATIONS. A SIMPLE AND TUNABLE OSCILLATOR BOOSTS THE PERFORMANCE OF A RANGE OF CIRCUITS. PART 1 OF THIS SERIES PRESENTS AN RTD DIGITIZER, THERMISTOR-TO-FREQUENCY CONVERTERS, AND RELATIVE-HUMIDITY DIGITIZERS.

A clock for all reasons, part 1: Monolithic oscillator invigorates instrumentation applications

Oscillators are fundamental circuit building blocks. A substantial percentage of electronic apparatus use oscillators as timekeeping references, as clock sources, for excitation, and for other tasks. The most obvious oscillator application is a clock source in digital systems. A second area is instrumentation. Transducer circuitry, carrier-based amplifiers, sine-wave generators, filters, interval generators, and data converters all use forms of oscillators. Although various techniques are common, a simply applied, broadly tunable oscillator with good accuracy widens the design possibilities of many of these circuits.

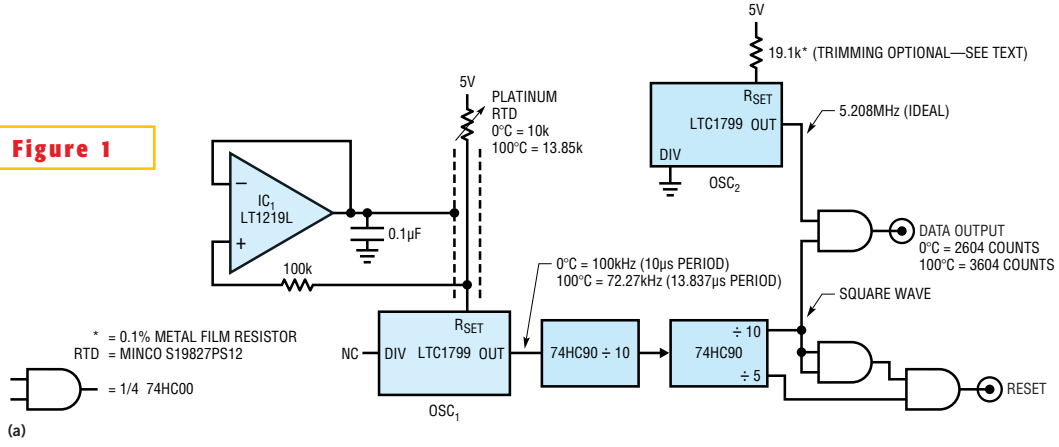
Commonly employed oscillators are resonant-element based or RC types (**Table 1**.) Quartz crystals and ceramic resonators offer high initial accuracy and low drift—particularly quartz types—but are



(b)

HORIZONTAL SCALE=100 µSEC/DIV
VERTICAL SCALE=5V/DIV

Figure 1



(a)

A platinum RTD digitizer is accurate to within 1° from 0 to 100°C (a). The circuit divides OSC1's output (Trace A) by 100 and gates the result with a 5.2-MHz clock, to produce data bursts (Trace C) that correspond to temperature (b).

essentially not tunable over any significant range. Typical RC types have lower initial accuracy and increased drift but are easily tunable over broad ranges. A problem with conventional RC oscillators is that considerable design effort is necessary to achieve good specifications. The LTC1799 is also an RC type, but its accuracy and drift specifications fit between resonator-based types and typical RC oscillators (see **sidebar** "A simple, high-performance oscillator"). The device's combination of simplicity, broad tuning range, and good accuracy invites use in instrumentation circuitry, as in the following examples.

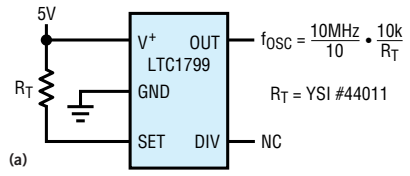
PLATINUM RTD DIGITIZER

Using a platinum RTD for R_{SET} of the LTC1799 oscillator results in a highly predictable OSC_1 output period versus temperature (**Figure 1a**). A series of counters scale the OSC_1 output and present the resultant signal to a clocked, period-determining logic network that delivers digital output data. Over a sensed-temperature range of 0 to 100°C, the circuit delivers 1000 counts with accuracy inside 1°C. You can extend the circuit's range for sensor limits of −50 to +400°C by using a monitoring processor to implement linearity correction in accordance with sensor characteristics. Linearity deviation over −50 to +400°C is several degrees (**Reference 1**).

If the RTD is at the end of a cable, IC_1 should drive the cable shield, as the **figure** shows. This action bootstraps the cable shield to the same potential as R_{SET}, eliminating jitter-inducing capacitive-loading effects at the R_{SET} node. The R_{SET} node of the LTC1799 is not unduly sensitive but does require management of stray capacitance (also see **sidebar**).

Waveforms show the circuit's operation (**Figure 1b**). The RTD determines OSC_1's output (Trace A), which the circuit divides by 100 and produces in square-wave form (Trace B). The logic network combines with OSC_2's fixed frequency to digitize the period measurement, which appears as output data bursts (Trace C). The logic also produces a reset output (Trace D), facilitating synchronization of monitoring logic.

The accuracy is approximately 1.5°C, primarily due to the initial error of the LTC1799. Obtaining accuracy inside 1°C involves simulating a temperature of 100°C, which is equivalent to 13,850Ω, at the sensor terminals and trimming R_{SET} for the appropriate output. A precision resistor decade box, such as the ESI DB62 (www.esi.com), allows convenient calibration.



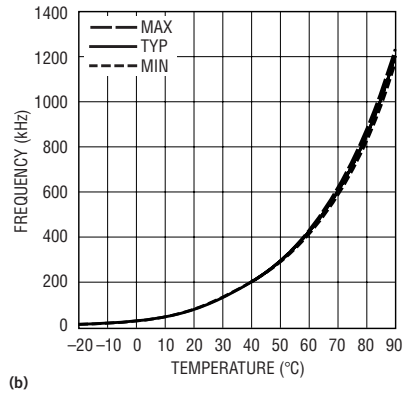


Figure 2

A simple temperature-to-frequency converter uses a thermistor to bias R_{SET} (a) and produces a predicable but nonlinear frequency output (b).

THERMISTOR-TO-FREQUENCY CONVERTER

A simple circuit also directly converts temperature to digital data (**Figure 2a**). In this case, a thermistor sensor, R_T, biases the R_{SET} pin. The LTC1799 frequency output is predictable although nonlinear. The inverse R_{SET}-versus-frequency relationship combines with the thermistor's nonlinear characteristic to give **Figure 2b**'s data. The curve is nonlinear although tightly controlled.

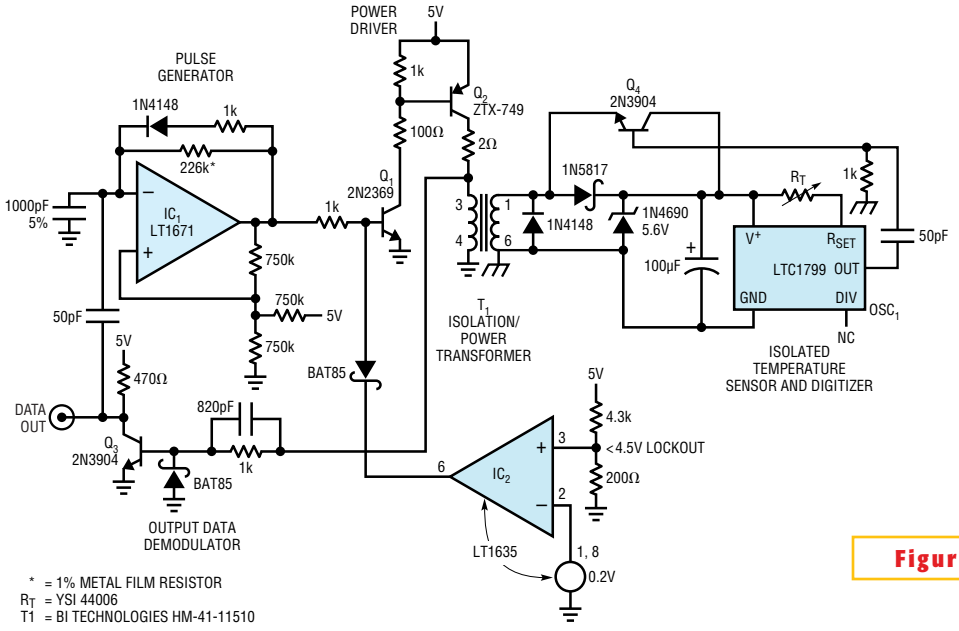
ISOLATED CONVERTER

An alternative circuit, which builds on the previous approach, galvanically isolates the thermistor from the circuit's power-and data-output ports (**Figure 3a**). The 3500V breakdown barrier between the thermistor and the power- and data-output ports permits operation at high common-mode voltages, which are common in industrial-measurement situations.

The pulse generator comprising IC_1 and associated components runs at approximately 10 kHz and produces a 2.5-µsec-wide output Trace A (**Figure 3b**). Q_1 and Q_2 provide power gain, driving T_1. (Trace B is Q_2's collector.) T_1's secondary responds by charging the 100-µF capacitor to a dc level via the 1N5817 rectifier. The capacitor powers OSC_1, which oscillates at the sensor-determined frequency. OSC_1's output, which the circuit differentiates to conserve power, switches Q_4. Q_4, in turn, drives T_1's secondary. T_1's primary receives Q_4's signal, and Q_3 amplifies this signal, producing the circuit's data output (Trace C). Q_3's collector also lightly modulates IC_1's negative input (Trace D), which synchronizes T_1's

TABLE 1–CHARACTERISTICS OF OSCILLATOR TYPES

Clock type	Typical frequency accuracy (%)	Typical frequency range	Tunability	Temperature coefficient	Power-supply-rejection ratio	Comments
Quartz	0.005	10 kHz to 200 MHz	Poor	0.5 ppm/°C, easily achieved	1 ppm/V	High stability and initial accuracy at expense of tunability; essentially no tunability; stability of 1×10^{-9} achievable with compensation techniques
Ceramic resonator	0.5	250 kHz to 60 MHz	Poor	30 ppm/°C	20 ppm/V	Lower performance and cost than quartz; essentially untunable
LTC1799	1.5	1 kHz to 33 MHz	Good	40 ppm/°C plus resistor-temperature coefficient	500 ppm/V	Add 10 to 50 ppm/°C temperature coefficient, depending on resistor type; extremely small footprint: SOT-23 and one resistor
Typical RC-based clock	10	1 Hz to 25 MHz	Good	200 ppm/°C	2500 ppm/V	Requires careful design and component selection for best results



(a)

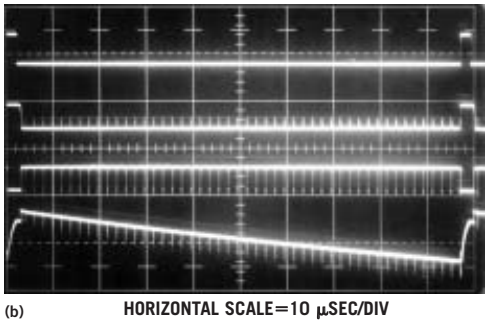
A galvanically isolated thermistor digitizer has a 3500V breakdown barrier (a). IC_1 provides pulsed power (Trace A) to OSC_1 via Q_1, Q_2, and T_1. Q_3 extracts data and presents it to the output (Trace C) (b).

A (IC_1 OUTPUT, 5V/DIV)

B (Q_2 COLLECTOR, 10V/DIV)

C (DATA OUTPUT, 10V/DIV)

D (IC_1 INPUT, 1V/DIV)



(b) HORIZONTAL SCALE=10 µSEC/DIV

Figure 3

primary drive to the data output. IC_2 prevents erratic circuit operation below 4.5V by removing Q_1's drive.

The pulse generator's clocking, while maintaining OSC_1's isolated dc power supply, generates periodic cessations in the frequency-coded output. You can use these interruptions as markers to control the operation of monitoring logic. Thermistor characteristics determine the output frequency as the **Table 2** shows.

HETERODYNE-BASED RH-SENSOR DIGITIZER

You can also design a circuit to convert the varying capacitance of a linearly responding RH (relative-humidity) sensor to a frequency output (**Figure 4a**). The 0-Hz to 1-kHz output corresponds to 0 to 100% sensed RH. Circuit accuracy is 2%, plus an additional tolerance dictated by the selected sensor's grade. Circuit temperature coefficient is 400 ppm/°C, and PSRR (power-supply rejection ratio) is less than 1% over 4.5 to 5.5V. Additionally, one sensor terminal attaches to ground, which is often beneficial for noise rejection.

This circuit is basically a heterodyne circuit. The circuit mixes two oscillators—one variable and one fixed—to produce sum and difference frequencies. The capacitive humidity sensor controls the variable oscillator. The demodulated difference frequency is the output. (Other examples have applied heterodyne techniques, which you usually associate with communications circuitry, to instrumentation. This circuit's operation is adapted from approaches in **references 2**, **3**, and **4**.) The heterodyne frequency-subtraction approach permits a sensed 0% RH to give a 0-Hz output, even though sensor capacitance is not zero at an RH of 0%.

IC_1 and associated components comprise a sensor-controlled variable oscillator that runs between the indicated output frequencies for the noted RH-

A SIMPLE, HIGH-PERFORMANCE OSCILLATOR

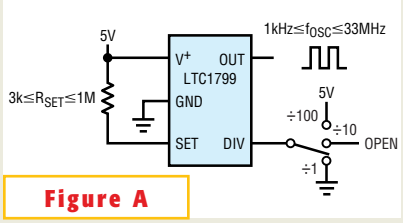
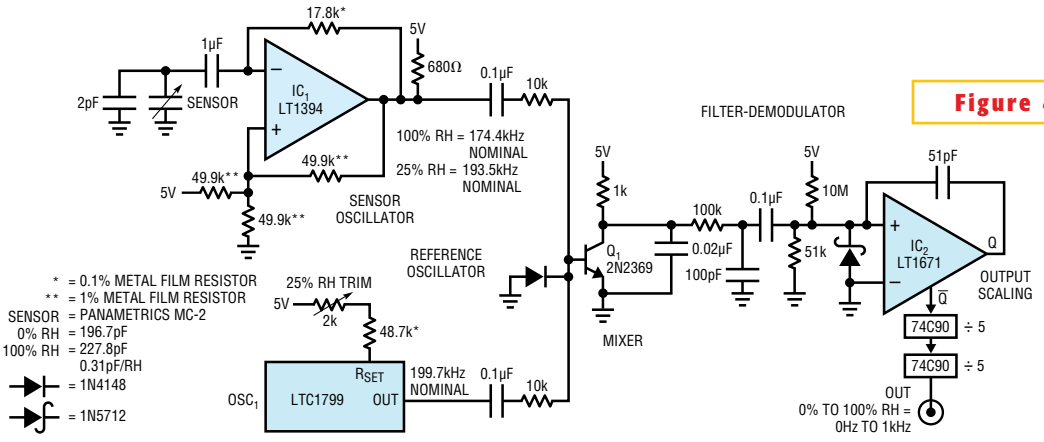


Figure A

The ratio of the voltage between the V^+ and SET pin and the current entering the SET pin controls the master-oscillator frequency of the LTC1799. A pin-programmable frequency divider permits output-frequency ranging.

The LTC1799 is a simple device with a sole analog input, the R_{SET} node (**Figure A**). A single R_{SET} resistor at this node programs the device's internal clock, and pin-settable decade dividers scale the output frequency. Various combinations of resistor value and divider choice permit outputs of 1 kHz to 33 MHz. An inverse relationship between resistance and frequency means that the LTC1799's period versus resistance is linear. Its board footprint, a five-pin SOT-23 package and a single resistor, is notably small, and an external timing capacitor is unnecessary.

The ratio of the voltage between the V^+ and SET pins and the current entering the SET pin controls the device's internal master oscillator. A PMOS transistor and its gate bias force the voltage on the SET pin to approximately 1.13V less than V^+. This voltage is accurate to ±7% at a particular input current and supply voltage. The effective input resistance is approximately 2 kΩ. The R_{SET} resistor connects internally between the V^+ and SET pins and locks together the variation between the voltage $V^+ - V_{SET}$ and current I_{RES}. This design provides the LTC1799's high precision.



(a)

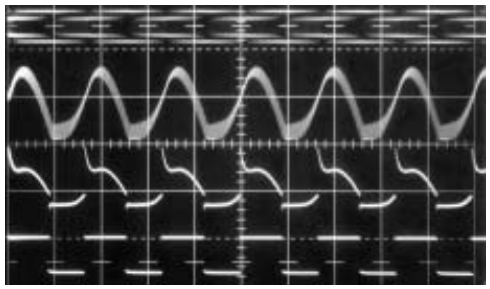
A heterodyne-based humidity-transducer digitizer has a grounded sensor and 2% accuracy (a). The circuit mixes sensor and stable oscillators at Q_1's base (Trace A), and the difference in frequency appears at Q_1's collector (Trace B). Filtering and ac hysteresis produce a clean IC_2 output (Trace D) (b).

A (Q_1 BASE, 2V/DIV)

B (Q_1 COLLECTOR, 2V/DIV)

C (IC_2 INPUT, 1V/DIV)

D (IC_2 OUTPUT, 5V/DIV)



(b) HORIZONTAL SCALE=50 µSEC/DIV

Figure 4

sensor excursion. The RH sensor is ac-coupled in accordance with its manufacturer's data sheet; dc coupling introduces destructive electromigration effects (**Reference 5**). You use the RH trim to tune reference oscillator OSC_1 to IC_1's nominal 0% RH-dictated frequency. The circuit mixes the two oscillators at Q_1's base, Trace A (**Figure 4b**). Q_1 amplifies the mixed-frequency components, although collector filtering attenuates the sum frequency. The RH-determined difference frequency, appearing as a sine wave at Q_1's collector (Trace B), remains. The circuit filters this waveform and ac-couples the result to zero-crossing detector IC_2. Hysteretic ac feedback at IC_2's input (Trace C) produces a clean IC_2 output (Trace D). Counter-based scaling at IC_2's output combines with slight sensor padding, via the 2-pF value across the sensor, to provide numeric output-frequency correspondence to RH. Calibration involves simulating the RH sensor's 25% value and trimming OSC_1 for a 250-Hz output. You can build the simulated value using known discrete capacitors or simply dial out the value using a precision, variable air capacitor (General Radio 1422D).

When evaluating the circuit's operation, it is useful to consider that the sensor oscillator's frequency changes inversely with sensor capacitance; oscillator period is linear versus sensor capacitance. This relationship would normally corrupt the desired linear output relationship between frequency and RH. Practically, because the sensor's excursion range is small compared with its 0% RH value, the error is similarly small. This term almost entirely accounts for the circuit's stated 2% accuracy.

CHARGE-PUMP-BASED RH-SENSOR DIGITIZER

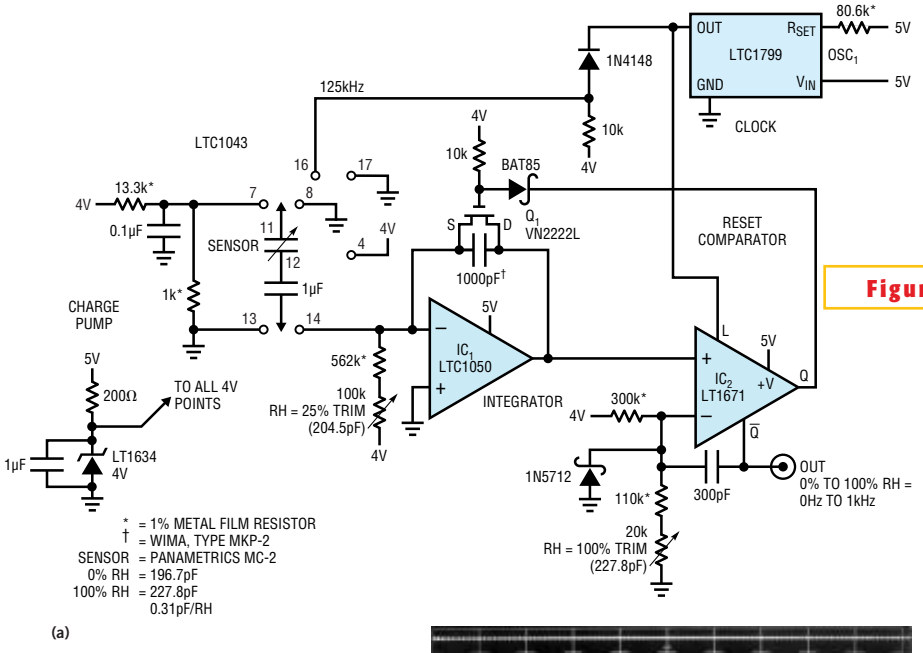
A circuit that digitizes the capacitive humidity sensor's output also has better specifications than the previous circuit (**Figure 5a**). Circuit accuracy is 0.3%, plus the selected sensor grade's tolerance. Temperature coefficient is approximately 300 ppm/°C, and PSRR is 0.25% for 5V±0.5V. Compromises include a floating sensor and somewhat more complex circuitry.

TABLE 2–OUTPUT FREQUENCY VERSUS THERMISTOR CHARACTERISTICS

Thermistor value (kΩ)	Sensor temperature (°F)	Output frequency
5	109	2.01 MHz
10	77	1.01 kHz
20	47	505 kHz
30	31	337 kHz
40	20	253 kHz
50	12	203 kHz
60	6	168 kHz
70	−1.3	145 kHz
80	−4.7	127 kHz
90	−8.5	113 kHz
100	−12	101 kHz

OSC_1 (Trace A, **Figure 5b**) clocks an LTC1043 switch-array-based charge pump. This configuration alternately connects the ac-coupled RH sensor to a 4V-reference-derived potential and then discharges the potential into IC_1's summing point. IC_1, an integrator, responds with a ramping output (Trace B). When IC_1's output exceeds IC_2's negative input voltage, IC_2's Q output (Trace C) goes high, triggering Q_1 and resetting the ramp. AC feedback to IC_2's negative input (Trace D) ensures long enough on-time for Q_1 to completely reset the ramp. This action's repetition rate depends on the RH sensor's value. OSC_1's output path to IC_2's latch input synchronizes the IC_1-IC_2 loop to the charge pump's clocking. In theory, if the charge pump, the offset term (25% trim current), and the ramp amplitude tie to the same potential, this circuit does not require a voltage reference. In practice, the sensor's extremely small capacitance shifts magnify the effect of charge-pump errors versus the supply, necessitating powering the LTC1043 from the 4V reference, which effectively ties all of these points to the 4V reference. Note that the 5V-powered OSC_1 output requires level shifting to drive the LTC1043.

A trimmed dc-offset current, via the 100-kΩ potentiometer, into IC_1's summing junction compensates the RH sensor's offset term (without compensation 0% RH≠0 pF). The 20-kΩ trim at IC_2 scales the output frequency so that 0 to 100% RH equates to a range of 0 to 1 kHz. Trimming involves substituting capacitance for the sensor's known 100 and 25% values and trimming the appropriate adjustments. The adjustments are somewhat interactive, necessitating repetition until convergence occurs. A precision variable capacitor (General Radio type 1422D) is invaluable in this regard, although you can achieve acceptable re-

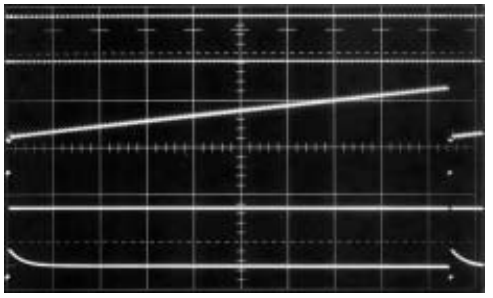


(a)

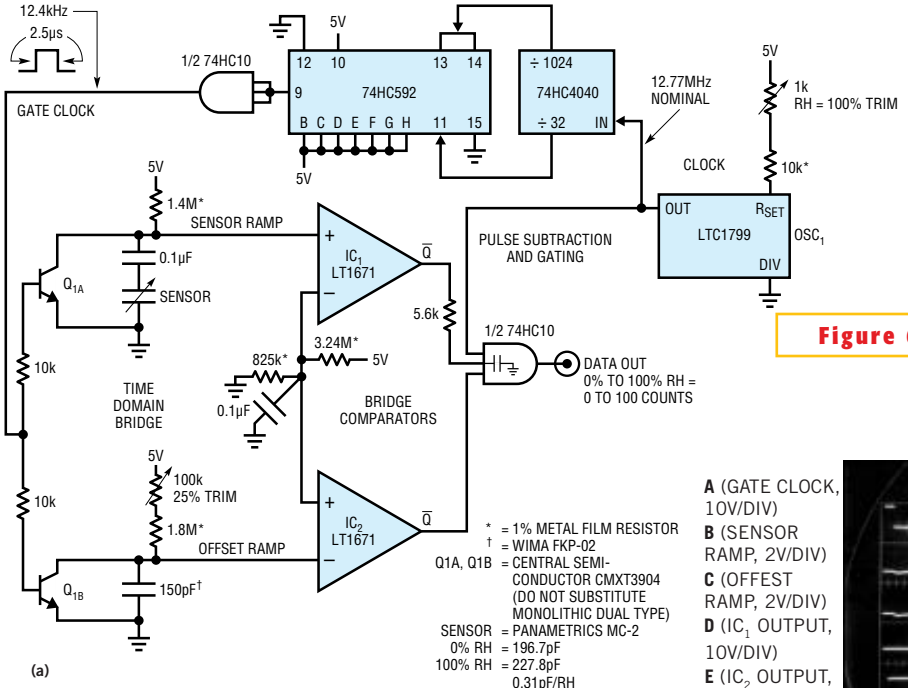
Figure 5

A hygrometer digitizer has 0.3% accuracy, but the sensor must float off-ground (a). OSC_1 drives an RH-sensor-based charge pump, producing a ramp at IC_1 (Trace B). IC_2's Q output biases Q_1 to reset the ramp (Trace C), and the frequency output at $\overline{Q}$ varies with humidity (b).

A (OSC_1 OUTPUT, 5V/DIV)
B (IC_1 OUTPUT, 1V/DIV)
C (IC_2 Q OUTPUT, 5V/DIV)
D (IC_2 −INPUT, 5V/DIV)



(b) **HORIZONTAL SCALE=100 µSEC/DIV**

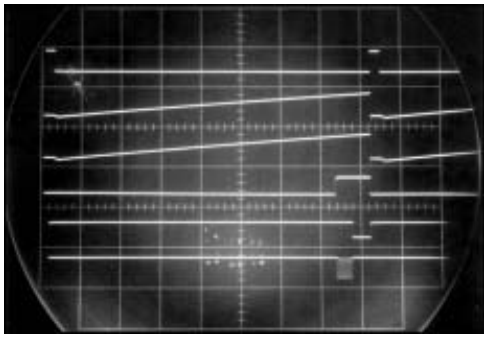


(a)

Figure 6

A humidity-transducer digitizer has a grounded sensor and 1% accuracy (a). Q_{1A} and Q_{1B} produce ramp outputs (Traces B and C), and IC_1 and IC_2 digitize the ramp times (Traces D and E). The digitized output consists of 0 to 100 counts for 0 to 100% RH (Trace F) (b).

A (GATE CLOCK, 10V/DIV)
B (SENSOR RAMP, 2V/DIV)
C (OFFEST RAMP, 2V/DIV)
D (IC_1 OUTPUT, 10V/DIV)
E (IC_2 OUTPUT, 10V/DIV)
F (DIGITIZED OUPUT, 10V/DIV)



(b) **HORIZONTAL SCALE=10 µSEC/DIV**

sults with built-up calibrated discrete capacitors.

RH-SENSOR DIGITIZER

Another RH digitizer features 1% accuracy, PSRR of 1% over 4.5 to 5.5V, temperature coefficient of 350 ppm/°C, and a ground-referred sensor (**Figure 6a**). Additionally, the circuit's trim scheme accommodates RH sensors with a wide tolerance grade. The circuit is basically a time-domain bridge; it subtracts time intervals representing sensor and sensor-offset values to determine the sensor value extrapolated to RH=0%. This measurement is digitized and scaled so that 0 to 100 counts corresponds to 0 to 100% RH at the output.

OSC_1's nominal 12.77-MHz output, which the circuit conditions using a counter chain and an inverter-configured gate, presents a 12.4-kHz, 2.5-µsec pulse, Trace A (**Figure 6b**), to Q_{1A} and Q_{1B}. The transistors' collectors fall to 0V. (Trace B is Q_{1A}'s collector, Trace C is Q_{1B}'s collector.) When the base drive ceases, both collectors ramp toward 5V. The slope of Trace B's ramp varies with the RH sensor's capacitance; the slope of Trace C's ramp represents the sensor's offset value (0% RH≠0 pF). IC_1 and IC_2 switch when their associated ramp inputs cross the comparators' common dc-input potential. The comparator outputs (Trace D=IC_1, Trace E=IC_2) define a "both-high" time region proportional to the ramp slopes' difference and, hence, an offset-corrected version of the sensor's value. The circuit gates this time interval with OSC_1's output to provide the data output (Trace F).

Circuit operation is fairly straightforward, although some details bear

mention. Q_1, a dual transistor, promotes cancellation of the individual transistors' V_{CE}-versus-temperature terms, minimizing their error contribution. Q_1's transistor is a two-die type to minimize crosstalk; do not substitute monolithic types. Similarly, do not substitute a dual comparator for the single types of IC_1 and IC_2. Also, the comparators operate at high source impedance relative to their input characteristics, but symmetry provides adequate error cancellation. Finally, the 5.6-kΩ resistor combines with the output gates' input capacitances, forming a lag of approximately 20 nsec. This delay prevents false output-data transients when the ramps are resetting.

The trimming procedure is similar to that of the previous RH circuit. Trimming involves substituting capacitance for the sensor's known 100 and 25% values and trimming the indicated adjustments. The adjustments are somewhat interactive, necessitating repetition until convergence occurs. As with the previous circuits, a precision variable capacitor (General Radio type 1422D) is invaluable for this work, although acceptable results are possible with calibrated discrete-capacitor assemblies.□

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Laboratory at the Massachusetts Institute of Technology (Cambridge). Williams enjoys art, collecting antique scientific instruments, and restoring old Tektronix oscilloscopes.

PART 1 OF THIS SERIES PRESENTED A VARIETY OF CIRCUITS THAT USE A MONOLITHIC OSCILLATOR IN VARIOUS APPLICATIONS. PART 2 CONTINUES WITH MORE EXAMPLES: CHOPPED AMPLIFIERS, SINE-WAVE GENERATORS, AN INTERVAL GENERATOR, AND AN ADC.

A clock for all reasons, part 2: Monolithic oscillator invigorates instrumentation applications

Although the most obvious application for an oscillator is as a clock source in digital systems, a second application area is instrumentation. A variety of circuits, continued here from part 1 of this series, which appeared in *EDN*'s June 26 issue, attests to the usefulness of a simple and accurate monolithic oscillator.

CHOPPED BIPOLAR AMPLIFIER

An adaptation of a previous circuit (**Reference 1**) combines a low-noise op amp with a chopper-based carrier-modulation scheme to achieve an extraordinarily low-noise, low-drift dc amplifier (**Figure 1a**). The dc drift and noise performance exceed any currently available monolithic amplifier. Offset is inside 1 µV with drift less than 0.05 µV/°C. Noise in a 10-Hz bandwidth is less than 40 nV, far below monolithic chopper-stabilized amplifiers. Bias current, set by the bipolar LT1028 op amp's input, is approximately 25 nA. One 5V supply powers the circuit, although its output swings ±2.5V. Additionally, a carefully selected chopping frequency prevents deleterious interaction with 60-Hz related components at the amplifier's input. These specifications suit demanding transducer-signal-conditioning sit-

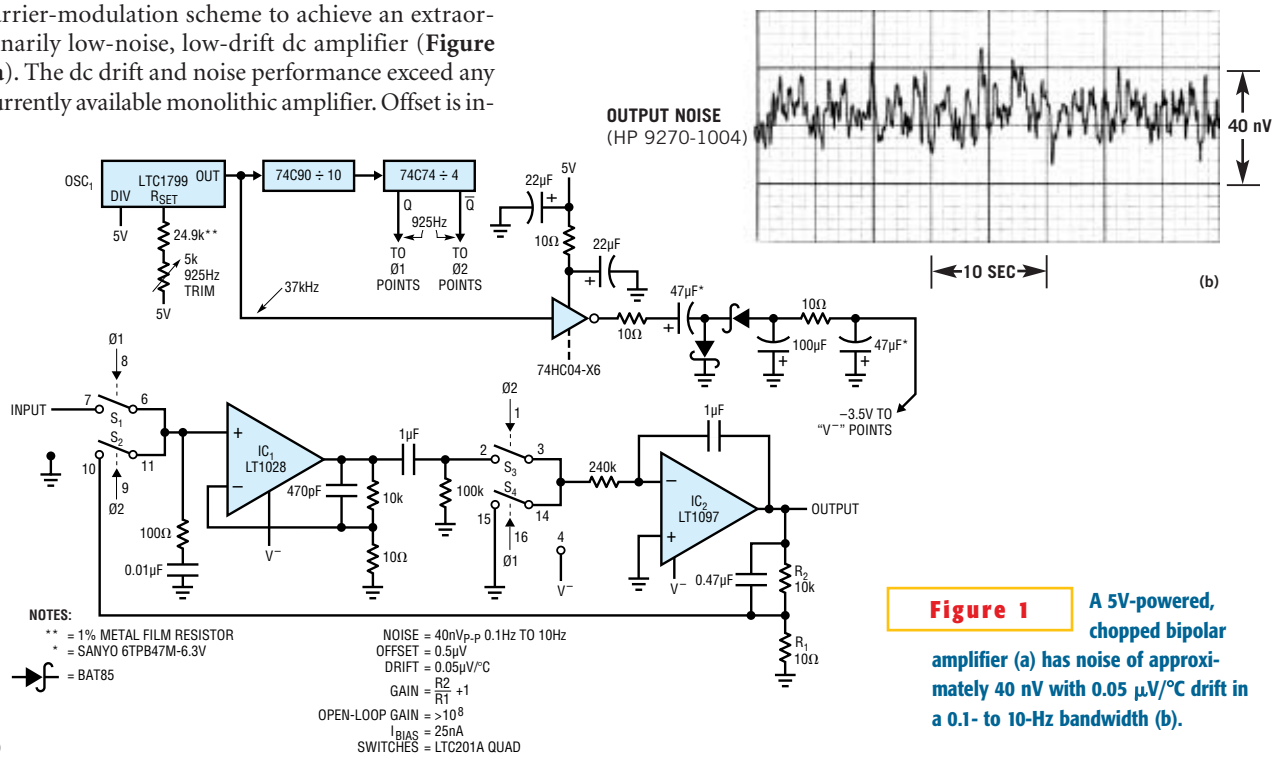


Figure 1 A 5V-powered, chopped bipolar amplifier (a) has noise of approximately 40 nV with 0.05 µV/°C drift in a 0.1- to 10-Hz bandwidth (b).

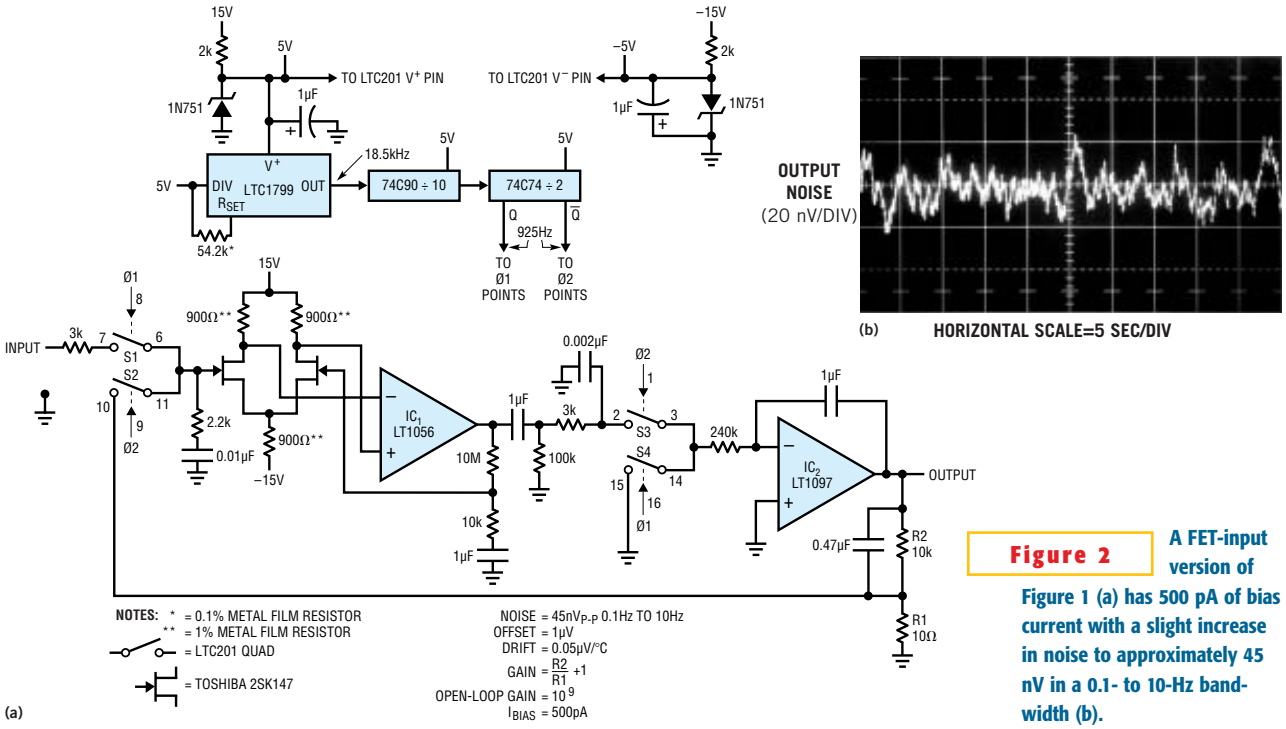


Figure 2 A FET-input version of Figure 1 (a) has 500 pA of bias current with a slight increase in noise to approximately 45 nV in a 0.1- to 10-Hz bandwidth (b).

uations, such as high-resolution scales and magnetic search coils.

The circuit divides OSC_1's 37-kHz output to form a two-phase, 925-Hz square-wave clock. This frequency, harmonically unrelated to 60 Hz, provides excellent immunity to harmonic beating or mixing effects, which could cause instabilities. S_1 and S_2 receive complementary drive, causing IC_1 to see a chopped version of the input voltage. IC_1 amplifies this ac signal. S_3 and S_4 synchronously demodulate IC_1's square-wave output. Because the input chopper synchronously drives these switches, the circuit presents the proper amplitude and polarity information to IC_2, the dc output amplifier. This stage integrates the square wave into a dc voltage, providing the output. The circuit divides down the output via R_2 and R_1 and feeds back the result to the input chopper where the feedback signal serves as a zero-signal reference. The R_1-to-R_2 ratio sets the gain, which is 1000 in this case. Because IC_1 is ac-coupled, its dc offset and drift do not affect overall circuit offset, resulting in the extremely low offset and drift performance. IC_1's input damper minimizes offset-voltage contribution due to nonideal switch behavior.

Normally, this single-supply amplifier's output would be unable to swing to ground. However, powering the circuit's negative rail from a charge pump eliminates this restriction. OSC_1's 37-kHz output excites the charge pump, which comprises paralleled logic inverters and discrete components. Deliberate 10Ω loss terms combine with the specified 47-µF capacitors to form a very-low-noise power source. These precautions eliminate charge-pump noise that might otherwise de-

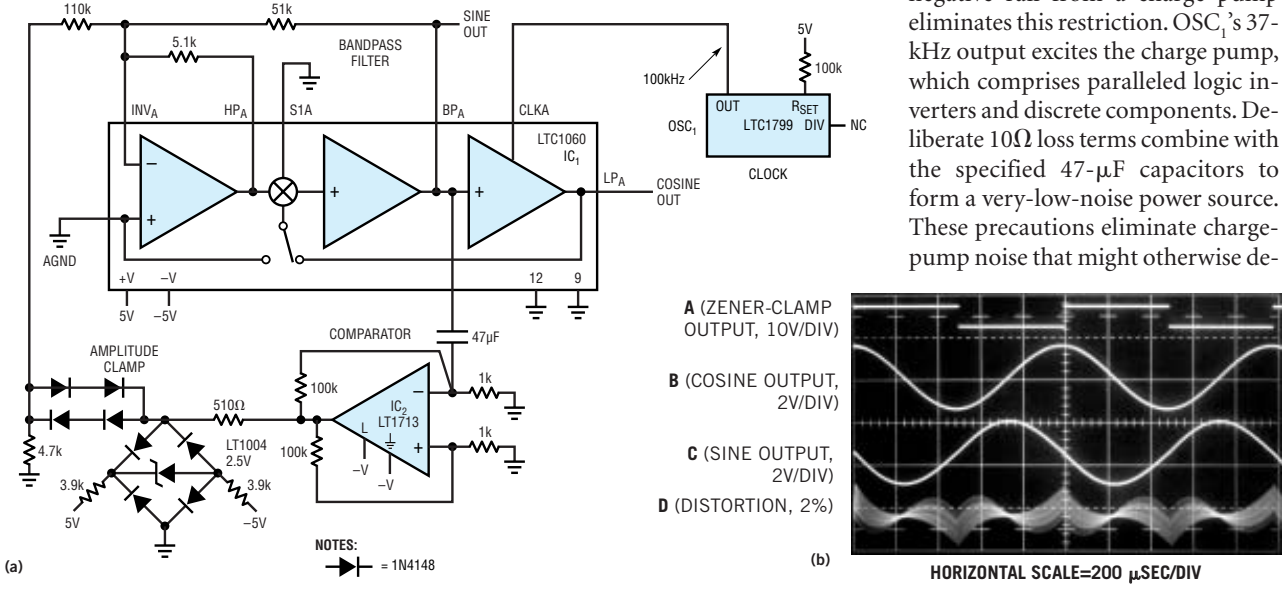


Figure 3 A bandpass filter, driven by IC_2's oscillation loop (a), continuously rings at resonance to produce cosine and sine outputs (b, traces B and C, respectively). A zener clamp (Trace A) sets the sine and cosine outputs' amplitude.

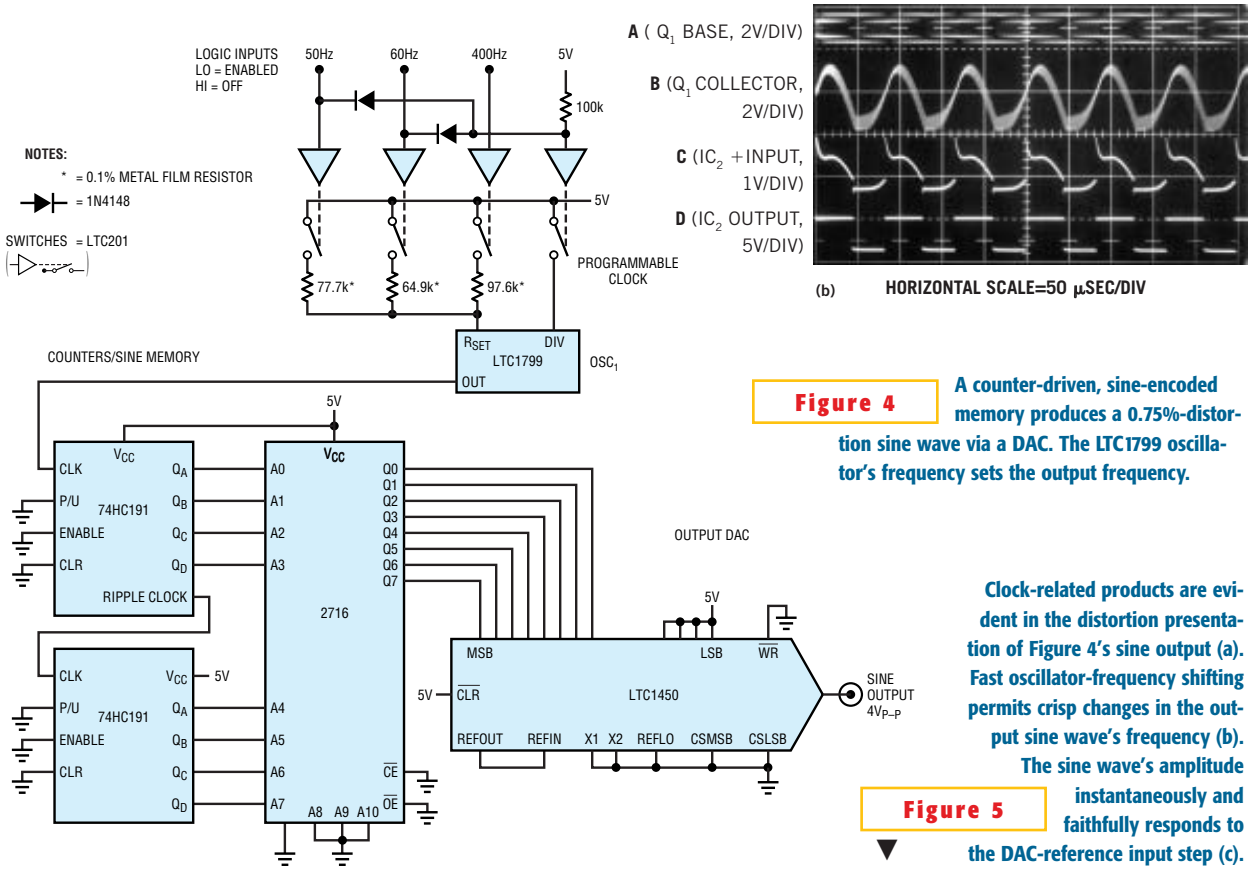


Figure 4 A counter-driven, sine-encoded memory produces a 0.75%-distortion sine wave via a DAC. The LTC1799 oscillator's frequency sets the output frequency.

Figure 5 Clock-related products are evident in the distortion presentation of Figure 4's sine output (a). Fast oscillator-frequency shifting permits crisp changes in the output sine wave's frequency (b). The sine wave's amplitude instantaneously and faithfully responds to the DAC-reference input step (c).

grade amplifier-noise performance.

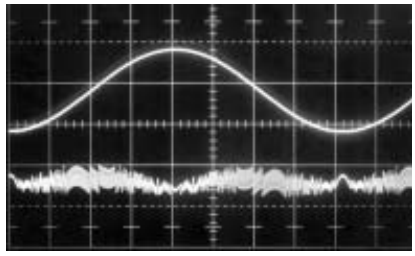
A noise plot of the amplifier in a 0.1- to 10-Hz bandwidth shows approximately 40 nV of peak-to-peak noise (**Figure 1b**). IC_1 and the 60Ω resistance of the S_1-S_2 pair contribute approximately equally to form this noise. When using this amplifier, it is important to realize that IC_1's bias current flowing through the input source impedance causes additional noise. In general, to maintain low-noise performance, the design should keep the source resistance at less than 500Ω. Fortunately, the output resistances of transducers, such as strain-gauge bridges, RTDs, and magnetic detectors, are well below this resistance figure.

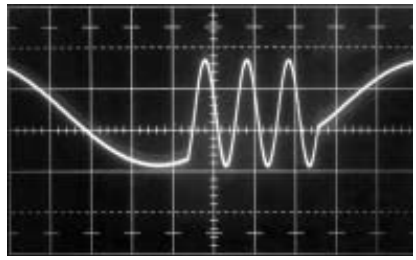
CHOPPED FET AMPLIFIER

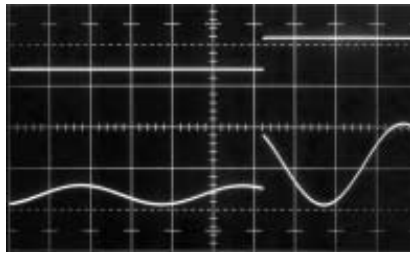
You can replace the previous circuit's input stage with a pair of extremely low-noise J-FETs to achieve noteworthy noise performance for a FET-input amplifier (**Figure 2a**). In most other respects, circuit operation is similar to that of the circuit in **Figure 1a**. Noise increases slightly to approximately 45 nV, but bias current decreases to 500 pA, which is 50 times lower than the previous circuit. The noise performance is noteworthy because it is almost 17 times better than currently available monolithic chopper-stabilized amplifiers and nearly equals the best bipolar designs. Other performance specifications, appearing in **Figure 2a**, are similar to those in **Figure 1a**.

This circuit retains the 925-Hz clock, although this ±15V-powered design uses zener diodes to derive internal ±5V points. The clock and logic run from 5V, and the LTC201 switches use ±5V. The switches' low-voltage rails reduce charge injection, minimizing its effect on offset voltage. RC damper networks further attenuate parasitic switch-behavior effects, resulting in the 1-µV offset specification.

Noise measured over a 50-sec interval is approximately 45 nV in a 0.1- to 10-Hz bandwidth (**Figure 2b**). This noise is spectacularly low for a J-FET based design and is directly attributable to the input pairs' die size and current density (**references 2** and **3**).







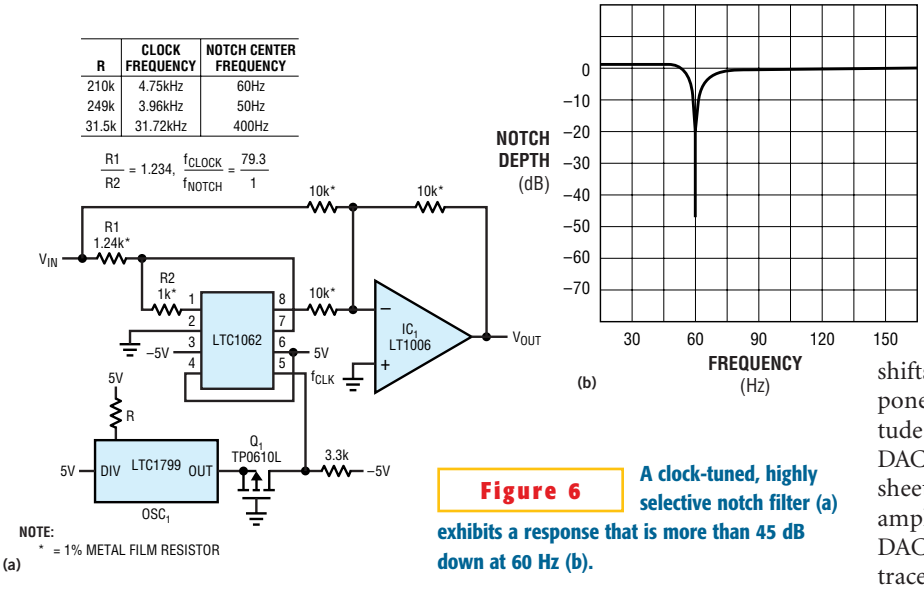


Figure 6 A clock-tuned, highly selective notch filter (a) exhibits a response that is more than 45 dB down at 60 Hz (b).

A sine-wave generator takes advantage of the fact that you can purposely design a feedback-loop-enclosed resonator that oscillates (**Figure 3a**). This circuit eliminates the need for an amplitude-control loop. This circuit, a mildly modified form of the Regan resonant-bandpass loop, is clock-tunable and produces sine and cosine outputs (**Reference 4**).

The circuit sets up IC_1's switched-capacitor filter as a clock-tunable bandpass filter with a Q of 10. OSC_1 clocks the filter at 100 kHz, resulting in a 1-kHz bandpass. The sine output switches IC_2, which supplies square-wave drive to the filter input in regenerative fashion. The loop is self-sustaining, resulting in continuous sine-wave outputs at the indicated points. Zener-bridge clamping of IC_2's output stabilizes the square-wave amplitude that the circuit applies to the filter and, hence, stabilizes the sine-wave outputs. This form of amplitude control eliminates AGC loop-settling times and potential instabilities. Changes in OSC_1's clock frequency permit bandpass tuning with no amplitude shifts during or after tuning.

The bandpass filter, responding to IC_2's clamped output (Trace A, **Figure 3b**), produces sine (Trace C) and cosine (Trace B) outputs (**Figure 3b**). Distortion (Trace D), which filter-clock residue dominates, is 2%.

The continuous clocking of a sine-coded look-up-table memory generates a variable-frequency sine wave (**Figure 4**). A DAC converts the memory's state to an analog output. The strength of this technique is its rapid, high-fidelity response to frequency- and amplitude-change commands. OSC_1's output, which digital-control inputs set to one of three output frequencies, clocks the 74HC191 counters. These counters parallel load a 2716 EPROM programmed to produce an 8-bit (256 states) digitally coded sine wave (For a copy of the sine-wave-generation code, see the Web version of this article at www.edn.com.)

The circuit in **Figure 4** tunes the sine-wave output in this case to 60 Hz (Trace A, **Figure 5a**). Distortion mostly comprises clock residue and measures approximately 0.75% (Trace B). The digital inputs abruptly change the output frequency to 400 Hz and then promptly return it to 60 Hz (**Figure 5b**). These frequency shifts occur crisply, with no alien components or untoward behavior. Amplitude shifts, accomplished by driving the DAC's reference input (see LTC1450 data sheet), are similarly well-behaved. The amplitude faithfully responds to the DAC-reference input step (**Figure 5c**, traces B and A, respectively). As before, the lack of control-loop time constants promotes the uncorrupted response.

A quick, clean way to tune a notch filter's center frequency is by varying a single, switchable resistor (**Figure 6a**). The LTC1062 switched-capacitor filter and LT1006 amplifier form a clock-tunable notch. OSC_1, running from the 5V supply, furnishes the clock, which Q_1 level-shifts to drive the ±5V-powered LTC1062. The table in the figure shows three common notch frequencies; you can select others by tuning OSC_1 using the equations in the **figure**.

The filter's performance at a 60-Hz center frequency shows that the response is down more than 45 dB, with steep slopes on either side of the notch (**Figure 6b**). The circuit maintains this characteristic over broad ranges of the clock-tuned center frequency.

An accurate interval generator, or "one shot," with a large dynamic range includes a clock, a counter, and a dual flip-

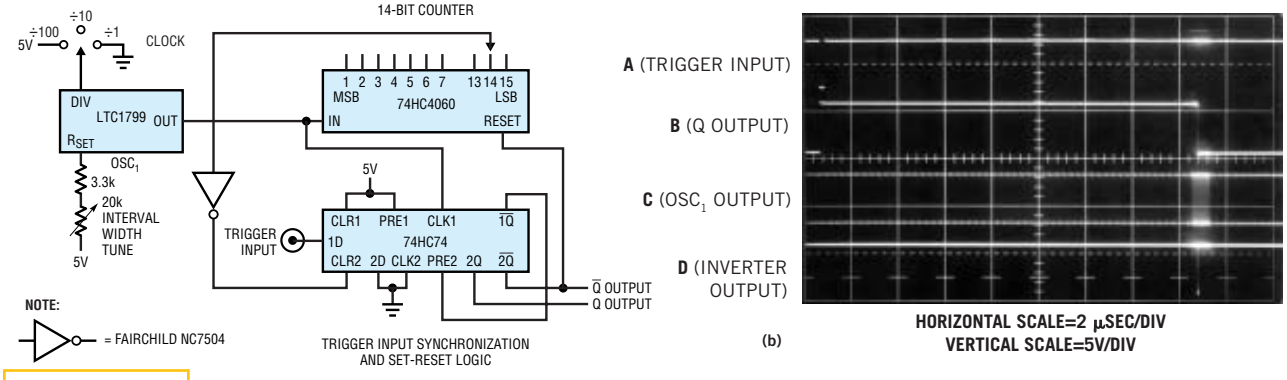


Figure 7 A 1%-accurate interval generator has a dynamic range of 20×10^6 to 1 (a). The trigger-input pulse (b, Trace A) sets the circuit's Q output high (Trace B), and the LTC1799 oscillator (Trace C) clocks the counter until the counter output-biases the inverter low to reset the circuit output (Trace D).

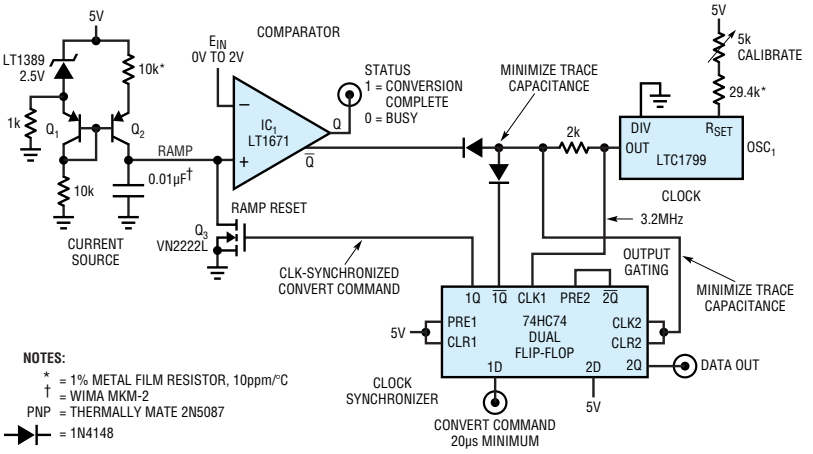
flop (**Figure 7a**). The clock frequency and counter modulo are programmable. A trigger input passes to the flip-flop IC's $\overline{1Q}$ output (Trace A, **Figure 7b**) synchronously with OSC_1's clock (Trace C). This output going low sets the 2Q output—the same as the circuit's Q output—high (Trace B). Simultaneously, the $\overline{2Q}$ output resets the 4060 counter, allowing it to accumulate clock pulses (Trace C, **Figure 7b**). When enough clock pulses occur to set the selected 4060 output high, the flip-flop IC's CLR2 clear input (Trace D) goes low, ending the circuit's output width. OSC_1's frequency and the counter's modulo, which are both variable over many decades, set the output width. In **Figure 7a**'s circuit, the interval is programmable from 800 nsec to 16 sec, although other counters can extend this range. Interval accuracy and stability almost entirely depend on OSC_1's programming resistor.

8-BIT, 80-µSEC, PASSIVE-INPUT ADC

In general, monolithic ADCs have replaced discrete types. Occasionally, specific desirable circuit characteristics dictate a discrete design. Examples of such special cases include the need for a passive analog input, a particular output data format or control protocol, and economic constraints. An 8-bit design has 90-ppm/°C drift (less than 1 LSB at 0 to 70°C) and converts in 80 µsec (**Figure 8a**). The circuit, a modern incarnation of an early electronic ADC, consists of a current source, an integrating capacitor, a comparator, logic, and a clock (**Reference 5**).

Applying a pulse to the convert-command input causes the flip-flop's 1Q output to go high (Trace A) when OSC_1 clocks the CLK_1 input (**Figure 8b**). This action turns on Q_3, resetting the 0.01-µF capacitor (Trace B). Simultaneously, the flip-flop's $\overline{1Q}$ output goes low, pulling the CLK2 and CLR2 inputs down. IC_1's Q output, which is the circuit's status output (Trace C), also goes low, and IC_1's $\overline{Q}$ output rises high. This logic state prevents any of OSC_1's clock pulses from transmitting to the circuit's data output (Trace D). When the convert command falls, the flip-flop's 1Q output goes low, Q_3 turns off, and the 0.01-µF capacitor's voltage begins to ramp. Concurrently, $\overline{1Q}$ goes high, allowing clock pulses to appear at the data output. When the ramp crosses the voltage at E_{IN}, IC_1's outputs exchange state, pulling the CLK2 and CLR2 lines low, and data-output pulses cease. Thus, the OSC_1-originated clock burst appearing at the data output is directly and solely proportional to E_{IN}. For the arrangement in **Figure 8a**, 256 pulses appear for a 2V full-scale input. Conversion time decreases with the time required for the ramp to cross E_{IN}. A full-scale conversion requires 80 µsec, linearly descending to 8 µsec at 0.1 scale.

The circuit connects the second flip-flop in the 74HC74 as a logic buffer that duplicates the high-impedance diode and 2-kΩ resistor node's logic state. Thus, you should minimize this node's trace capacitance, which this design accomplishes by locating the diodes and 2-kΩ resistor adjacent to the CLK2 and CLR2 inputs. You can trim the circuit by applying a 2V input and adjusting OSC_1's frequency output using the 5-kΩ calibrating potentiometer for 256 data-output pulses per conversion.□



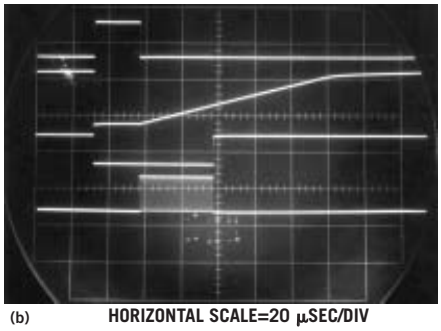


Figure 8 **A simple 8-bit ADC has a passive, high-impedance input and an 80-µsec conversion time (a). A synchronized convert command (b, Trace A) begins a reference ramp and forces the circuit status output low (Trace C). When the ramp crosses E_{IN}'s voltage, the circuit output's clock burst ceases (Trace D).**

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DERIVING A SLEW-RATE-MEASUREMENT APPROACH REQUIRES UNDERSTANDING SLEW RATE'S RELATIONSHIP TO AMPLIFIER DYNAMICS.

The taming of the slew

Slew rate defines an amplifier's maximum rate of output excursion. This specification sets limits on undistorted bandwidth, an important capability in ADC-driver applications. Slew rate also influences achievable performance in DAC-output stages, filters, video amplification, and data acquisition. You must verify an amplifier's slew rate by measurement if your application's performance depends on that parameter.

AMPLIFIER DYNAMIC RESPONSE

Amplifier-dynamic-response components include delay, slew, and ring times (**Figure 1**). The delay time is small and is almost entirely due to amplifier propagation delay. During this interval, no output movement occurs. During *slew time*, the amplifier moves at its greatest possible speed toward the final value. *Ring time* defines the region during which the amplifier recovers from slewing and ceases movement within some defined error band. *Settling time* is the total elapsed time from input application until the output arrives at and remains within a specified error band around the final value (**references 1**, **2**, and **3**).

You measure slew rate during the middle two-thirds of output movement at unity gain and express the result in volts per microsecond. By discounting the initial and final movement intervals, you ensure that amplifier-gain-bandwidth limitations during partial input overdrive do not influence the measurement.

Historically, slew-rate measurement has been relatively simple. Early amplifiers had typical slew rates of 1V/µsec, and later versions sometimes reached hundreds of volts per microsecond. Standard laboratory pulse generators easily supplied rise times well beyond amplifier speeds. As slew rates have reached 1000V/µsec, the pulse generator's finite rise time has become a concern. At least one recent device, the LT1818, has a 2500V/µsec slew rate, or 2.5V/nsec, comparable with a Schottky TTL gate's transition time. Such speed eliminates almost all pulse generators as candidates for putting the amplifier into slew-rate limiting.

PULSE-GENERATOR RISE TIME AFFECTS MEASUREMENT

Pulse-generator-rise-time limitations are a significant concern when attempting to accurately determine slew rate, as a unity gain amplifier's response to progressively faster pulse-generator rise times demonstrates (**Figure 2**). The data shows a nonlinear slew-rate increase as pulse-generator rise time decreases. The continuous slew-rate increase with decreasing generator rise time, although approaching a zero rise-time-enforced boundary, hints that the source has not yet driven the amplifier to its slew-rate limit. Determining whether this condition is satisfied requires a faster pulse generator than one with a 1-nsec rise time.

Most general-purpose pulse generators have rise times in the region of 2.5 to 10 nsec. Instrument rise times of less than 2.5 nsec are relatively rare, and only a select few can reach 1 nsec (**Reference 2**). The ranks of generators that offer rise times of less than 1 nsec

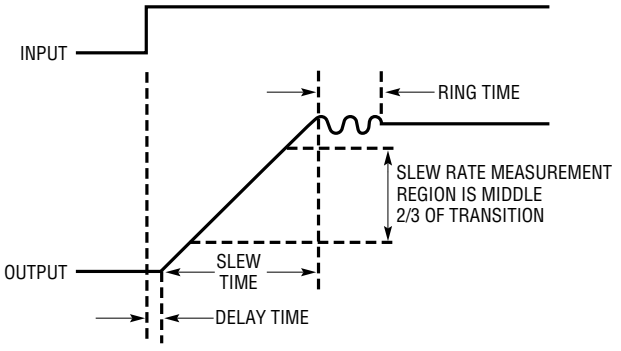


Figure 1 Amplifier-response components include delay, slew, and ring times. You typically measure slew rate during the middle two-thirds of the slew time.

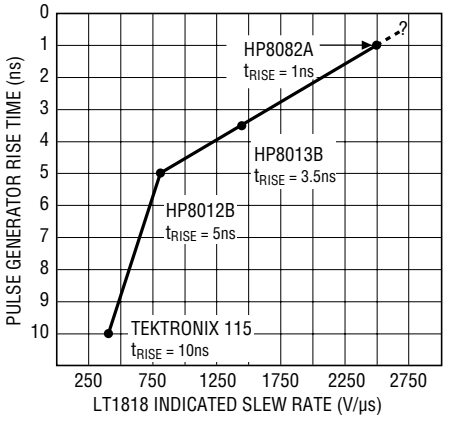


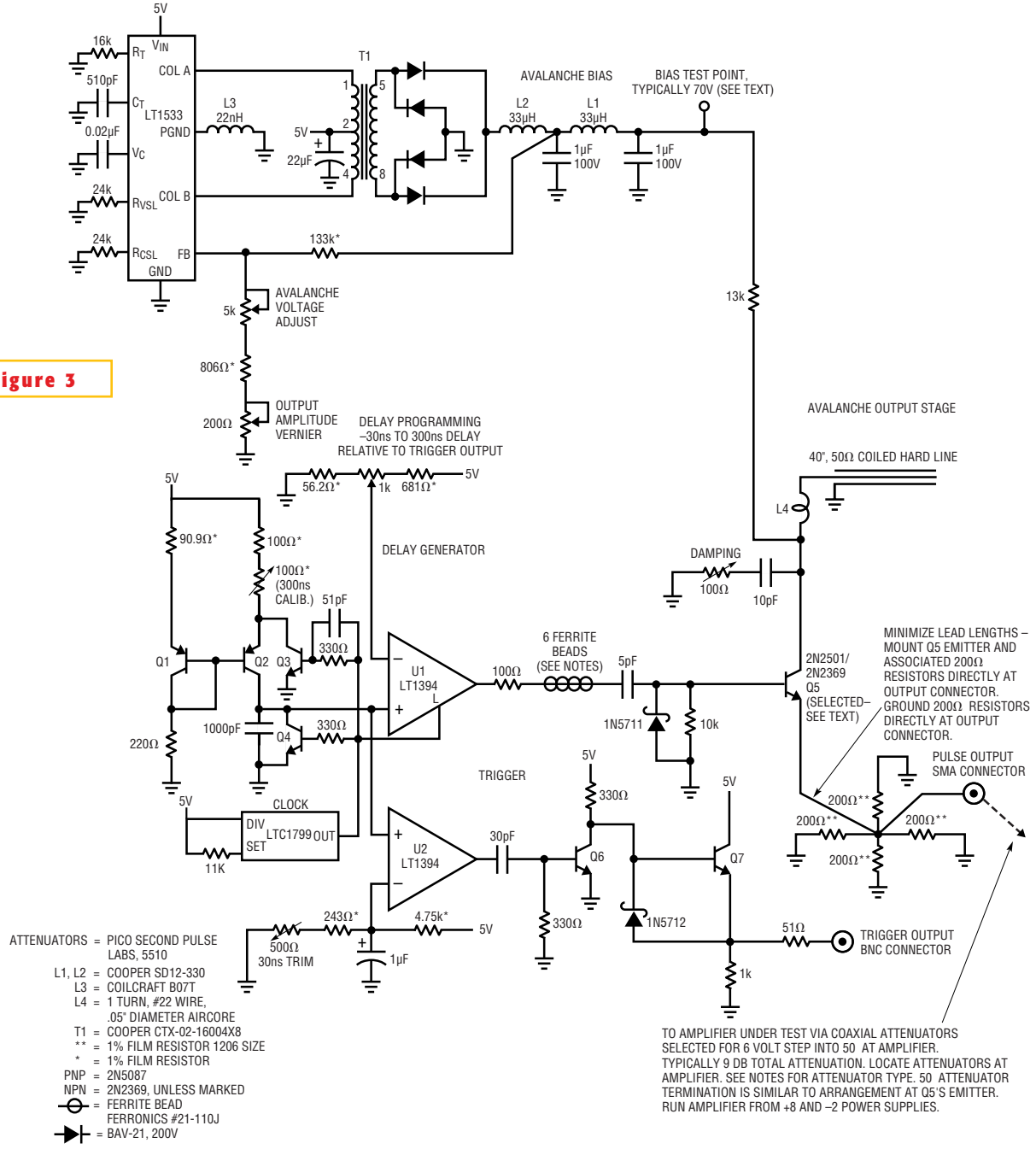
Figure 2 Summarized data for the pulse generators demonstrates that decreasing rise time promotes higher observed slew rate. Verifying slew-rate-limiting occurrence requires a pulse generator with a rise time of less than 1 nsec.

are even thinner. They employ arcane technologies and exotic construction techniques, particularly in situations that require relatively large swings of 5 to 10V (**references 4** to **16**). Available instruments in this class work well but can easily cost $10,000; prices rise toward $30,000, depending on features. For slew-rate testing in a laboratory or production environment, there is a substantially less expensive alternative.

Figure 3 shows a circuit for producing rise-time pulses of less than 1 nsec. The circuit's rise time is 360 psec, and its pulse amplitude is adjustable. You can set the output pulse to occur either before or after a trigger output. This circuit uses an avalanche pulse generator to create extremely fast rise-time pulses.

Q1 and Q2 form a current source that charges the 1000-pF capacitor. When the LTC1799 clock is high both Q3 and Q4 are on (**Trace A**, **Figure 4**). Under the same conditions, the current source is off and Q2's collector (**Trace B**) is at ground. U1's latch input prevents it from responding, and its output remains high. When the clock goes low, comparator U1's latch input is disabled, and its output drops low. The Q3 and Q4 collectors lift, and Q2 turns on, delivering constant current to the 1000-pF capacitor (**Trace B**). The resulting linear ramp appears on

Figure 3



A variable delay triggers a pulse generator with a rise time of less than 1 nsec. The charge line at Q5's collector determines the output width: about 10 nsec. You can set the output pulse occurrence before, during, or after the trigger output.

U1 and U2's positive inputs. U2, biased from a potential derived from the 5V supply, goes high 30 nsec after the ramp begins, providing the "trigger output" (**Trace C**) via its output network. U1 goes high when the ramp crosses the potentiometer-programmed delay at its negative input—in this case, about 170 nsec. U1's going high triggers the avalanche-based output pulse (**Trace D**). This arrangement permits the delay programming control to vary output-pulse occurrence from 30 nsec before to 300 nsec after the trigger output.

When U1 applies its output pulse to Q5's base, the NPN transistor avalanches. The result is a quickly rising pulse across Q5's emitter-termination resistor. The 10-pF collector capacitor and the charge line discharge, Q5's collector voltage falls, and breakdown ceases. The 10-pF collector capacitor and the charge line then recharge. At U1's next pulse, this action repeats. The 10-pF capacitor supplies the initial pulse response, and the charge lines prolonged discharge contributes the pulse body. The 40-in. charge line forms an output pulse width of about 12 nsec.

Avalanche operation requires high voltage bias. The low-noise LT1533 switching regulator and associated components supply this high voltage. The LT1533 is a push-pull output switching regulator with controllable transition times.

Slower switch transitions notably reduce noise in the form of output harmonic content (**Reference 4**). Resistors at the RCSL and RVSL pins control the switch current and voltage transition times, respectively. In all other respects, the circuit behaves as a classical push-pull, step-up converter.

You begin optimizing the circuit by setting the output-amplitude vernier to its maximum and grounding Q4's collector. Next, set the avalanche-voltage adjust so that free-running pulses begin to appear at Q5's emitter, noting the bias test points voltage. Readjust the avalanche-voltage 5V below this voltage, and unground Q4's collector. Set the 30-nsec trim so that the trigger output goes low 30 nsec after the clock goes low. Adjust the delay programming control to maximum and set the 300-nsec calibration so that U1 goes high 300 nsec after the clock goes low. You may have to repeat the adjustments for the 30- and 300-nsec trims until you've calibrated both points, due to a slight interaction.

Select Q5 from a population for optimal avalanche behavior. Such behavior, although characteristic of the device specified, is not guaranteed by the manufacturer. During one recent selection experiment, a sample of 30 Semelab 2N2501s spread over a 17-year date-code span produced a yield of about 90%. All "good" devices switched in less than 475 psec, and some switched in less than 300 psec. You may substitute a 2N2369, available from a number of suppliers, including Philips Semiconductors and Central Semiconductor, though their switching times are rarely less than 450 psec. In practice, you should select Q5 for an in-circuit rise time of less than 400 psec and then optimize the output-pulse shape for slew-rate testing by adjusting Q5's collector damping trim. The optimization procedure takes full advantage of the freedom that slew-rate testing does not require pulse purity.

Slew-rate testing permits overshoot and post-transition aberrations if they do not influence amplifier response in the measurement region. A simple procedure allows you to optimize the waveform (**Figure 5**). Set the damping trim for significant effect, resulting in a reasonably clean pulse but sacrificing rise time (**Figure**

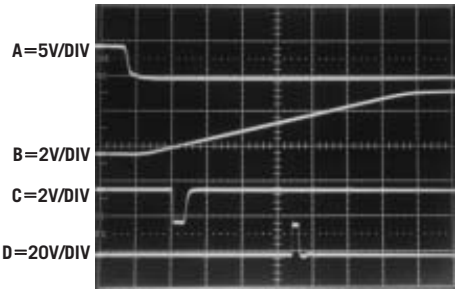


Figure 4 The pulse generator's waveforms include the clock (Trace A), Q2's collector ramp (Trace B), the trigger output (Trace C), and the pulse output (Trace D). A delay sets the output pulse to occur about 170 nsec after the trigger output.

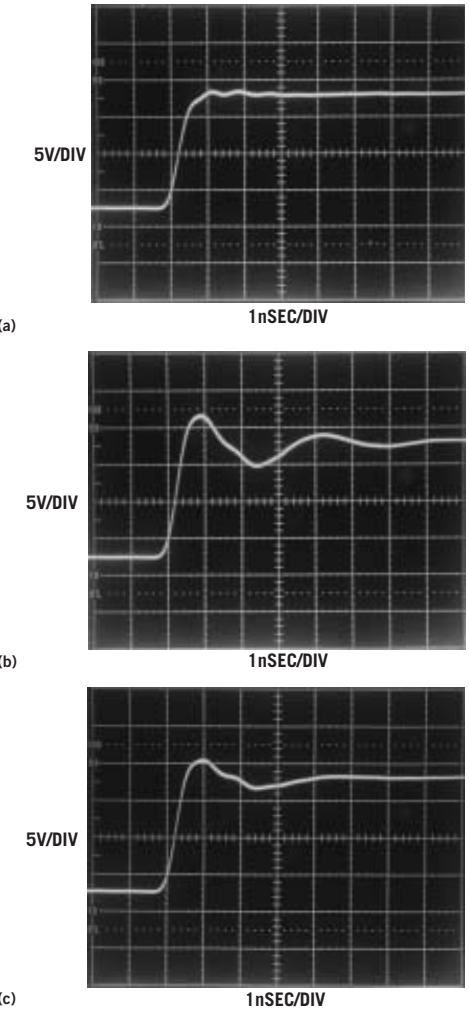


Figure 5 Excessive damping trades off the rise time and rounds the front corner but minimizes pulse-top aberrations (a). Minimal damping accentuates rise time, but pulse-top ringing is excessive (b). Optimal damping retards pulse-top ringing and preserves rise time in the slew-rate-measurement region (c).

FOR MORE INFORMATION...

For more information on products such as those discussed in this article, contact any of the following manufacturers directly, and please let them know you read about their products in *EDN*.

Avtech
www.avtechpulse.com

Agilent
www.agilent.com

Central Semiconductor
www.centralsemi.com

Linear Technology
www.linear.com

Picosecond Pulse Labs
www.picosecond.com

Philips Semiconductor
www.semiconductors.philips.com

Semelab
www.semelab.co.uk

Stanford Research Systems
www.srsys.com

Tektronix
www.tektronix.com

5a). Notice the waveform with the control at the opposite extreme (**Figure 5b**). Minimal damping accentuates rise time, but pronounced post-transition ring may influence amplifier operation during slew testing. A damping point corresponding to a realistic compromise only slightly reduces the edge rate but significantly attenuates post-transition ring (**Figure 5c**). A 1-GHz- real-time-bandwidth oscilloscope (Tektronix 7104/7A29/7B15) with a 350-psec-rise-time limit produced the traces that the photographs depict. Accurately determining the rise time for the circuit in **Figure 5c** requires more bandwidth and verification of the measurement signal-path integrity, including cables, attenuators, probes, and the oscilloscope (see **sidebar** "Verifying rise-time-measurement integrity"). Subsequent photos (see the

VERIFYING RISE-TIME-MEASUREMENT INTEGRITY

Any measurement requires the experimenter to ensure measurement confidence. Some form of calibration check is always in order. High-speed time-domain measurement is particularly prone to error, and various techniques can promote measurement integrity.

A battery-powered, 200-MHz crystal oscillator produces 5-nsec markers, useful for verifying oscilloscope timebase accuracy (**Figure A**). A single 1.5V AA cell supplies the LTC3400 boost regulator, which produces 5V to run the oscillator. A peaked attenuation network delivers the oscillator output to the 50Ω load. This circuit provides well-defined 5-nsec markers and prevents overdriving low-level sampling oscilloscope inputs (**Figure B**).

Once you confirm timebase accuracy, you must check rise time. You should include the lumped signal-path rise time, including attenuators, connections, cables, oscilloscope, and anything else in the path in this measurement. Such end-to-end rise-time checking is an effective way to promote meaningful results. A guideline for ensuring accuracy is to have four-times-faster measurement- path rise time than the rise time of interest. Thus, a 360-psec rise-time measurement requires a verified 90-psec measurement-path rise time to support it. Verifying the 90-psec-measurement path rise time, in turn, necessitates a faster-than-22.5-psec rise-time test step. **Table A** lists some very fast edge generators for rise-time checking.

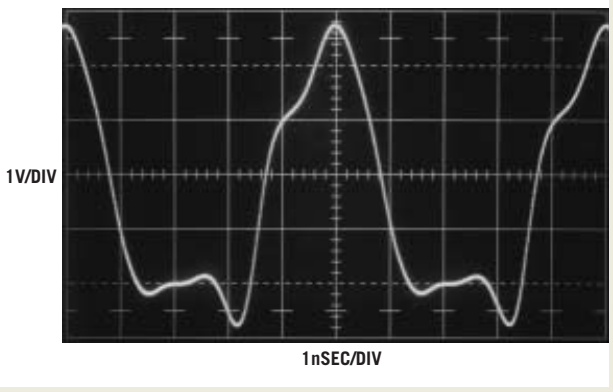


Figure B The time-mark generator output terminated into 50Ω produces a peaked waveform, which is optimal for verifying timebase calibration.

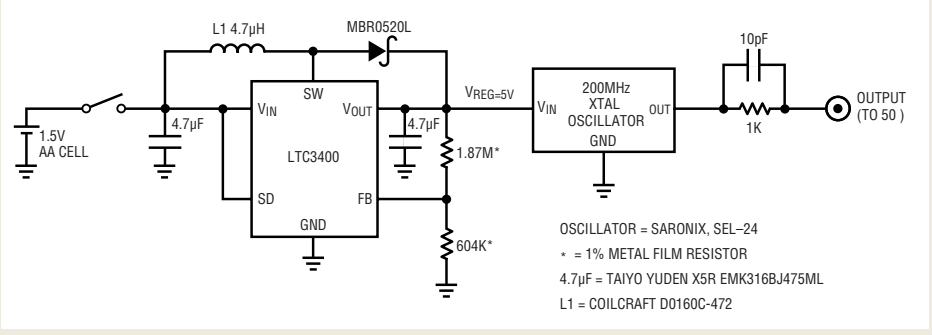


Figure A A 1.5V battery powers a 200-MHz crystal oscillator that provides 5-nsec time markers. A switching regulator converts the 1.5V source to 5V to power the oscillator.

TABLE A–FAST EDGE DETECTORS FOR RISE-TIME CHECKING

Manufacturer	Model	Rise time (psec)	Amplitude	Availability	Comments
Avtech	AVP2S	40	0V to 2V	Current production	Free-running or triggered operation, 0 to 1 MHz
Agilent	213B	100	≈175 mV	Secondary market	Free-running or triggered operation to 100 kHz
	1105A/1108A	60	≈200 mV	Secondary market	Free-running or triggered operation to 100 kHz
	1105A/1106A	20	≈200 mV	Secondary market	Free-running or triggered operation to 100 kHz
Picosecond Pulse Labs	TD1110C/TD1107C	20	≈230 mV	Current production	Similar to discontinued HP1105/1106/8A; see above
Stanford Research Systems	DG535 OPT 04A	100 psec	0.5V to 2V	Current production	Must be driven with stand-alone pulse generator
Tektronix	284	70 psec	≈200 mV	Secondary market	50-kHz repetition rate; pre-trigger 75 to 150 nsec before main output; calibrated 100-MHz and 1 GHz sine-wave auxiliary outputs
	111	500 psec	≈±10V	Secondary market	10- to 100-kHz repetition rate; positive or negative outputs; 30- to 250-nsec pretrigger output; external trigger input; pulse width set with charge Lines
	067-0513-00	30 psec	≈400 mV	Secondary market	60-nsec pretrigger output; 100-kHz repetition rate
	109	250 psec	0V to ± 55V	Secondary market	≈600-Hz repetition rate (high-pressure Hg Reed-relay based); positive or negative outputs; pulse width set by charge lines

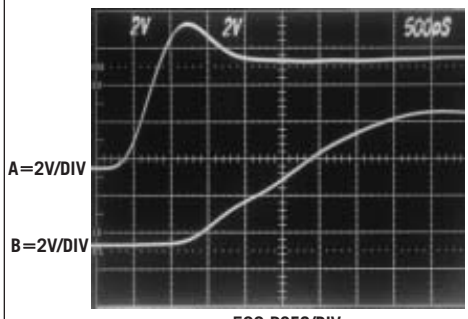


Figure 6 Trace A's 360-psec rise-time pulse completes its transition before the amplifier output (Trace B) begins moving. Trace A's rise time is actually about 150 psec faster than depicted due to the 1-GHz measurement bandwidth that limits the observed response.

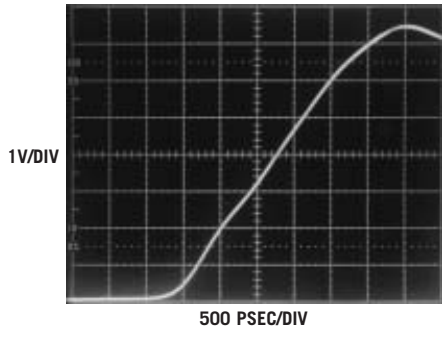


Figure 7 A close examination of the LT1818's response indicates an approximate 2800V/µsec slew rate, revealing an 11% error in the measurement with a 1-nsec rise-time pulse in Figure 2.

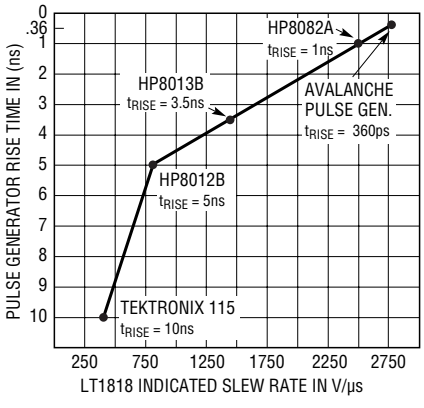


Figure 8 This restatement of the data from Figure 2 includes the avalanche pulse generator results. A further significant slew rate increase is unlikely as the required input step rise time approaches zero.

Web version of this article at www.edn.com), using a 3.9-GHz-bandwidth oscilloscope, the Tektronix 556 with 1S2 sampling plug-in capable of a 90-psec-rise-time, indicate a 360-psec output rise time. The other photo, using a 6-GHz-bandwidth oscilloscope, the Tektronix TDS 6604, which offers a 60-psec rise time, aids measurement confidence by verifying the 360-psec rise time. The 360-psec rise time is almost three times faster than the 1-nsec rise-time pulse generator, which is the fastest of those that generated the data in **Figure 2** and that promoted a 2500V/µsec slew rate. **Figure 6** puts this kind of speed into perspective. Trace A's 360-psec rise time completes its transition before Trace B's 400-MHz LT1818 amplifier begins to move. Trace A's rise time is actually faster than depicted, because the 1-GHz real-time-measurement bandwidth limits observed response. Applying this faster rise-time pulse should add useful information to **Figure 2**'s data.

REFINING SLEW-RATE MEASUREMENT

The unity gain amplifier's response to the 360-psec rise-time pulse in a 1-GHz real-time bandpass indicates a measurement-region slew rate of about 2800V/µsec (**Figure 7**). This measure reveals an 11% error in the earlier assessment (**Figure 8**). The new data suggests that, although slew-rate "hard" limiting may not be occurring, little practical improvement is possible, because rise time is approaching zero. A faster rise-time pulse generator could confirm this assessment, but any slew-rate improvement would likely be academic. Realistically, you rarely encounter the large-signal, 360-psec-rise-time input required to promote 2800V/µsec slew rate in practical circuitry.□

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You can find all the references for this article in its Web version at www.edn.com.

Author's biography

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web only

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By Jim Williams and Albert Wu, Linear Technology Corp

SUCCESSFULLY IMPLEMENTING FLASH LAMPS INVOLVES UNDERSTANDING NUMEROUS PRACTICAL CONSIDERATIONS.

Simple circuitry for cellular-telephone/ camera-flash illumination

Next-generation cellular telephones will include high-quality photographic capabilities. To support their improved image sensors and optics, they will need high-quality "flash" illumination, which requires special design attention. This lighting is crucial for yielding good photographic performance and requires careful consideration.

Two practical choices exist for flash illumination: LEDs and flash lamps (**Table 1**). LEDs feature continuous operating capability and low-density support circuitry, among other advantages. Flash lamps, however, have some important characteristics for high-quality photography. Their line-source light output is hundreds of times greater than point-source LEDs, which results in dense, easily diffused light over a wide area. Additionally, the flash lamp's color temperature of 5500° to 6000°K is close to the temperature of natural light, which eliminates the color correction needed by a so-called white LED's blue-peaked output.

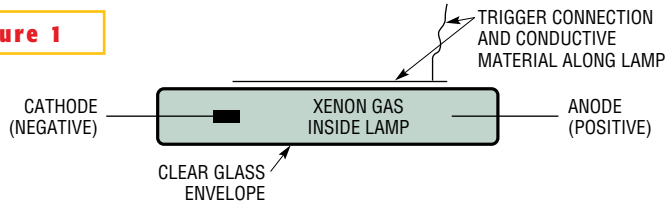
Figure 1 shows a conceptual flash lamp, with a cylindrical glass envelope that is filled with xenon. Anode and cathode electrodes directly contact the gas; the trigger electrode, distributed along the lamp's outer surface, does not. The gas breakdown potential voltage is in the multikilovolt range; once breakdown occurs, lamp impedance drops to less than 1Ω. High current flow in the broken-down gas produces intense visible light. Practically, the large current necessary requires that the circuitry must put the lamp into its low-impedance state before it emits light.

The trigger electrode serves this function. It transmits a high-voltage pulse through the glass envelope, ionizing the xenon along the lamp length. This ionization breaks down the gas, placing it into a low-impedance state. The low impedance permits large current to flow between anode and cathode, producing intense light. The energy involved is so high that current flow and light output are limited to pulsed operation. Continuous operation would quickly produce extreme temperatures, damaging the lamp. When the current pulse decays, lamp voltage drops to a low point, and the lamp reverts to its high-impedance state. It then needs another trigger event to initiate conduction.

SUPPORT THOSE HOT FLASHES

Figure 2 diagrams conceptual support circuitry for flash-lamp operation. A trigger circuit and a storage capacitor that generates the high transient current service the flash lamp. In operation, the flash capacitor is typically charged to 300V. Initially, the capacitor cannot discharge, because the lamp is in its high-impedance state. A command to the trigger circuit produces the multikilovolt trigger pulse at the lamp. The lamp breaks down, allowing the capacitor to discharge. (Strictly speaking, the capacitor does not fully discharge, because the lamp reverts to its high-impedance state when the potential across it decays to some low value—typically, 50V.)

Figure 1



The flash lamp consists of xenon gas-filled glass cylinder with anode, cathode, and trigger electrodes.

Capacitor, wiring, and lamp impedances typically total a few ohms, resulting in transient current flow in the 100A range. This large current pulse produces the intense flash of light.

The ultimate limitation on flash-repetition rate is the lamp's ability to safely dissipate heat. A secondary limitation is the time required for the charging circuit to fully charge the flash capacitor. The large capacitor charging toward a high voltage combines with the charge circuit's finite output impedance, limiting how quickly charging can occur. Charge times of 1 to 5 sec are possible, depending upon available input power, capacitor value, and charge-circuit characteristics.

The scheme shown in **Figure 2** discharges the capacitor in response to a trigger command. It is sometimes desirable to have a partial discharge, resulting in less intense light flashes. Such operation permits "redeye" reduction, in which one or more reduced-intensity flashes immediately precede the main flash. (Redeye in a photograph is caused by the human retina reflecting the light flash with a distinct red color. You eliminate it by causing the eye's iris to constrict in response to a low-intensity flash immediately preceding the main flash.) The modifications of **Figure 3** provide this operation, where you might have added a driver and a high-current switch to **Figure 2**.

These components permit stopping flash-capacitor discharge by opening the lamp's conductive path. This arrangement allows the "trigger/flash-command" control-line pulse width to set current-flow duration and, hence, flash energy. The low-energy, partial capacitor discharge allows rapid recharge, permitting several low-intensity flashes in rapid succession immediately preceding the main flash, without lamp damage.

The flash-capacitor charger of **Figure 4** is basically a transformer-coupled step-up converter with some special capabilities. When the "charge" control line goes high, the regulator clocks the power switch, allowing step-up transformer T_1 to produce high-voltage pulses. These pulses are rectified and filtered, producing the 300V-dc output, with conversion efficiency of about 80%. The circuit regulates by stopping the drive to the power switch when it reaches the desired output. It also pulls the "done" line low, indicating that the capacitor is fully charged. Intermittent power-switch cycling compensates for any capacitor-leakage-induced loss.

Normally, the circuit would obtain feedback by resistor-chain-dividing down the output voltage. This approach is unacceptable here, because it would require excessive switch cycling to offset the feedback resistor's constant power drain. Although this action would maintain regulation, it would also drain excessive power from the primary source, presumably a battery. Instead, the circuit obtains its regulation by monitoring T_1's flyback-pulse characteristic, which reflects T_1's secondary amplitude. The output voltage is set by T_1's turns ratio. This feature permits tight capacitor-voltage regulation, necessary to ensure consistent flash intensity without exceeding lamp-energy or capacitor-voltage ratings. Also, the capacitor value conveniently determines

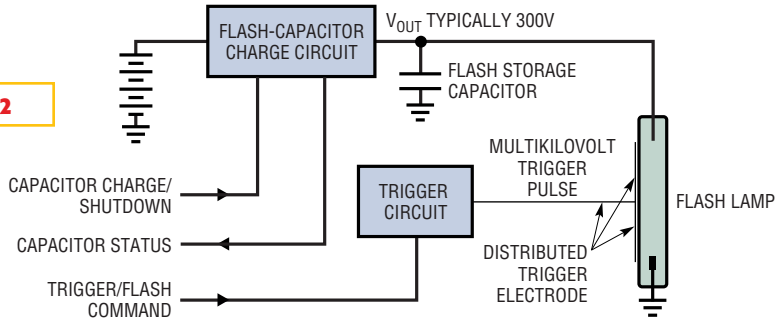


Figure 2

Conceptual flash-lamp circuitry includes a charge circuit, storage capacitor, trigger, and lamp.

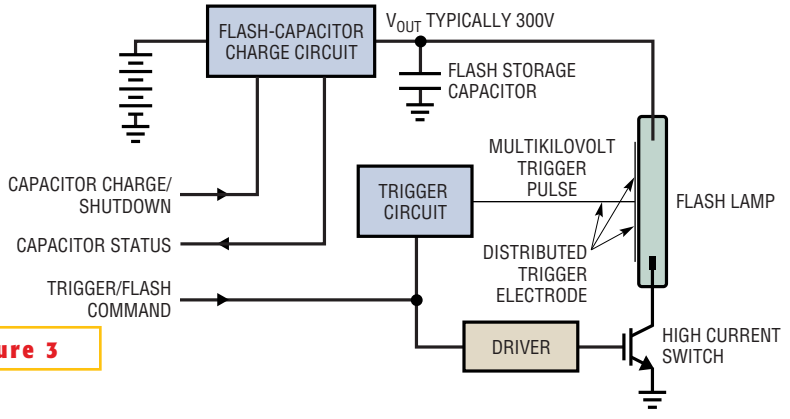


Figure 3

Adding a driver/power switch to Figure 2 permits partial capacitor discharge, allowing pulsed low-level light before main flash, thus minimizing "redeye" phenomena.

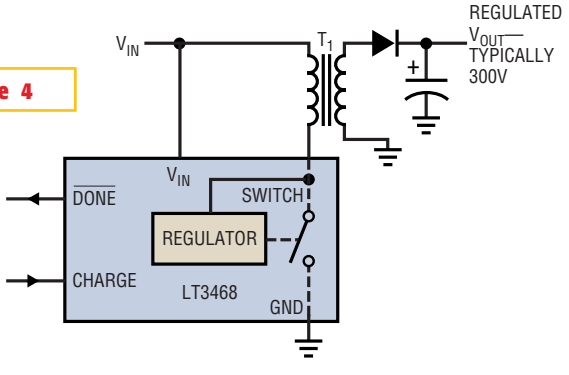


Figure 4

A flash-capacitor charger circuit includes an IC regulator, a step-up transformer, a rectifier, and a capacitor.

flash-lamp energy without any other circuit alterations.

THE NEXT CHALLENGE IS THE DETAILS

Figure 5 is a complete flash-lamp circuit based on the previous discussion. **WARNING: This circuit contains high-voltage, lethal potentials. Use extreme caution in its construction, testing, and usage.** The capacitor-charging circuit, similar to **Figure 4**, appears at the upper left. Diode D_2 has been added to safely clamp reverse-transient-voltage events, which originate at T_1. FETs Q_1 and Q_2 drive high-current switch Q_3. Step-up transformer T_2 forms the high-voltage trigger pulse. Assuming that C_1 is fully charged, when Q_1 and Q_2 turn on Q_3, C_2 deposits current into T_2's primary winding. T_2's secondary winding delivers a high-voltage trigger pulse to the lamp, ionizing it to permit conduction. C_1 discharges through the lamp, producing light.

Figure 6 details the capacitor-charging sequence. In Trace A, the "charge" input goes high, which initiates T_1 switching, causing C_1 to ramp up (Trace B). When C_1 arrives at the regulation point, switching ceases, and the resistively pulled-up "done" line drops low (Trace C), indicating C_1's charged state. The "trigger" command (Trace D), resulting in C_1's discharge via the lamp-Q_3 path, may occur any time (in this case, approximately 600 msec) after "done" goes low. Note that this **figure**'s trigger command is lengthened for photographic clarity; it is normally 500 to 1000 µsec in duration for a complete C_1 discharge. Short trigger-input commands facilitate low-level flash events, such as for redeye reduction.

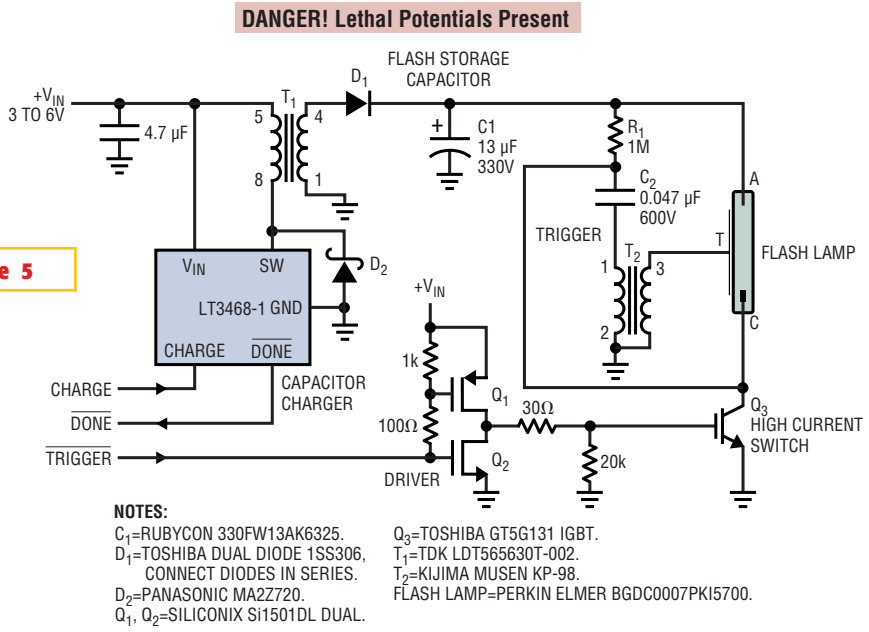


Figure 5

A complete flash-lamp circuit includes capacitor-charging components (left side), flash capacitor C_1, trigger (R_1, C_2, T_2), Q_1-Q_2 driver, Q_3 power switch, and flash lamp.

Figure 7 shows a high-speed detail of the high-voltage trigger pulse (Trace A) and resultant flash-lamp current (Trace B). Some amount of time is required for the lamp to ionize and begin conduction after triggering. Here, 10 µsec after the 8-kV p-p trigger pulse, flash-lamp current begins its rise to nearly 100A. The current rises smoothly in 5 µsec to a well-defined peak before beginning its descent. The resultant light produced, **Figure 8**, rises more slowly and peaks in about 25 µsec before decaying. Slowing the oscilloscope sweep permits capturing all the current and light events. **Figure 9** shows that the light-output (Trace B) profile follows the lamp-current (Trace A) profile, although current-peaking is more abrupt. Total event duration is approximately 500 µsec, with most of the energy expended in the first 200 µsec. The leading edge's discontinuous presentation is due to the oscilloscope's chopped-display-mode operation.

LAMP, LAYOUT, AND RFI ISSUES

Several lamp-related issues require your attention. First, you must thoroughly understand and adhere to lamp-triggering requirements. Otherwise, you can end up with an incomplete flash or even no lamp flash. Most trigger-related problems involve trigger-transformer selection, drive, and physical location with

TABLE 1–PERFORMANCE CHARACTERISTICS FOR LED- AND FLASH-LAMP-BASED ILLUMINATION

Performance category	Flash lamp	LED
Light output	High–typically 10 to 400× higher than LEDs. Line source output makes even light distribution relatively simple.	Low–point source output makes even light distribution somewhat difficult.
Illumination versus time	Pulsed--good for sharp, still picture.	Continuous--good for video.
Color temperature	5500 to 6000°K–very close to natural light. No color correction necessary.	8500°K–blue light requires color correction.
Solution size	Typically 3.5×8×4 mm for optical assembly; 27×6×5 mm for circuitry--dominated by flash capacitor (6.6 mm in diameter, may be remotely mounted).	Typically 7×7×2.4 mm for optical assembly; 7×7×5 mm for circuitry
Support-circuitry complexity	Moderate	Low
Charge time	1 to 5 sec, depending on flash energy	None–light always available.
Operating voltage and currents	Kilovolts to trigger, 300V to flash. I_{SUPPLY} to charge is approximately 100 to 300 mA, depending on flash energy. Essentially zero standby current.	Typically 3.4 to 4.2V at 30 mA per LED continuous, 100 mA peak. Essentially zero standby current.
Battery power consumption	200 to 800 flashes per battery recharge, depending on flash energy.	Approximately 120 mW per LED (continuous light) and 400 mW per LED (pulsed light).

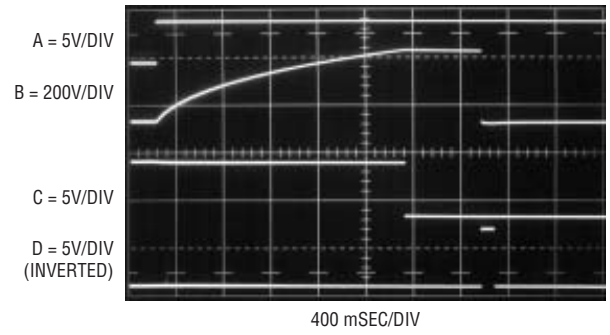


Figure 6 Capacitor-charging waveforms include charge input (Trace A), C_1 (Trace B), "done" output (Trace C), and "trigger" input (Trace D).

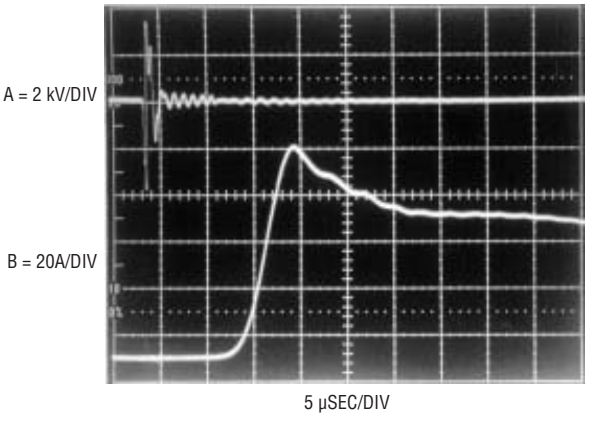


Figure 7 High-speed detail of the trigger pulse (Trace A) and resultant flash-lamp current (Trace B) show that some amount of time is required for the lamp to ionize and begin conduction after triggering.

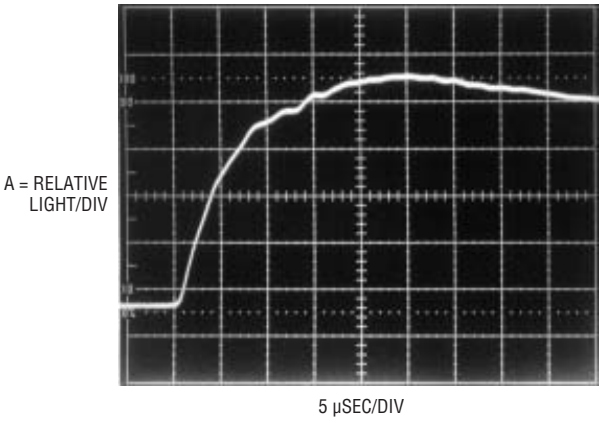


Figure 8 The smoothly ascending flash-lamp light output peaks in 25 µsec.

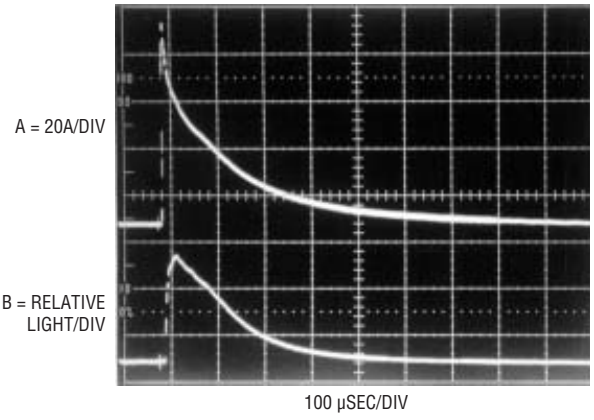


Figure 9 A photograph captures all current (Trace A) and light (Trace B) events; light output follows current profile, although peaking is less defined.

respect to the lamp. Some lamp manufacturers supply the trigger transformer, lamp, and light diffuser as a single, integrated assembly (**Reference 3**). This type of offering obviously implies trigger-transformer approval by the lamp vendor, assuming that you trigger it properly. When the lamp is triggered with a user-selected transformer and drive scheme, it is essential that you obtain lamp-vendor approval before going to production.

The lamp's anode and cathode have access to the lamp's main discharge path. The circuit must respect electrode polarity, or the lamp's lifetime will be severely reduced. Similarly, respect the lamp-energy dissipation restrictions, so lamp lifetime doesn't suffer. Severe lamp-energy overdrive can result in lamp cracking or disintegration. Energy is easily and reliably controlled by selecting capacitor value and charge voltage and restricting flash-repetition rate. As with triggering, lamp-flash conditions promoted by the user's circuit require lamp-manufacturer approval before production.

Assuming proper triggering and flash energy, you can expect lamp lifetimes of approximately 5000 flashes. Lifetimes for various lamp types do differ from this typical figure, but all vendors specify the lifetime of their particular lamps. Note that lifetime is typically defined as the point at which lamp luminosity drops to 80% of its original value.

The high voltages and currents of lamp-related circuits mandate layout planning. Referring back to **Figure 5**, C_1's discharge path is through the lamp, Q_3, and back to ground. The approximately 100A peak current means you must maintain this discharge path at low impedance. Conduction paths between C_1, the lamp, and Q_3 should be short and well below 1Ω.

Additionally, Q_3's emitter and C_1's negative terminal should be directly connected—the goal being a tight, highly conductive loop between C_1's positive terminal, the lamp, and Q_3's return back to C_1. Avoid abrupt trace discontinuities and vias, as the high current flow can cause conductor erosion in local high-resistivity regions. If you must employ vias, they should be filled, verified for low resistance, or used in multiples. Unavoidable capacitor ESR, lamp, and Q_3 resistances typically total 1 to 2.5Ω, so total trace resistance of 0.5Ω or less is adequate. Similarly, the relatively slow rise time of the high current (**Figure 7**) means trace inductance does not have to be tightly controlled.

C_1 is the largest component in the circuit; space considerations may make it

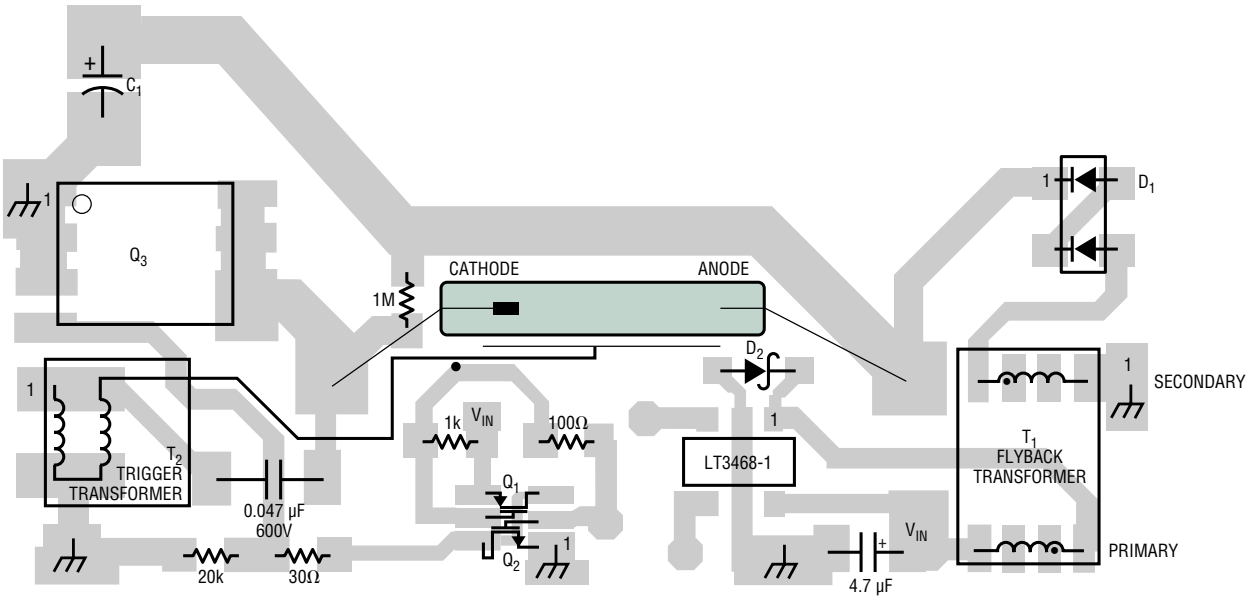


Figure 10

In this magnified demonstration layout for Figure 6, lamp connections are wires, not traces, and wide T_1 secondary spacing accommodates 300V output.

desirable to remotely mount it. You can facilitate this mounting with long traces or wires, as long as you maintain interconnect resistance within the limits stated above.

Capacitor charger-IC layout is similar to conventional switching-regulator practice. The electrical path formed by the IC's V_{IN} pin, its bypass capacitor, the transformer primary, and the switch pin must be short and highly conductive. The IC's ground pin should directly return to a low-impedance, planar ground connection. The transformer's 300V output requires larger than minimum spacing for all high-voltage nodes to meet circuit-board breakdown requirements. Verify board-material-breakdown specifications and ensure that board-washing procedures do not introduce conductive contaminants.

T_2's multikilovolt trigger winding must connect directly to the lamp's trigger electrode, preferably with less than $^1/_4$-in. of conductor. You must employ adequate high-voltage spacing. In general, what little conductor there is should not contact the circuit board. Excessive T_2 output length can cause trigger-pulse degradation or RFI; therefore, modular flash-lamp-trigger transformer assemblies are excellent choices.

Figure 10 contains a demonstration layout for **Figure 5**, showing its topside component layer. Power and ground are distributed on internal layers. The LT-3468 layout is typical of the switching-regulator practice previously described, although its wide trace spacing accom-

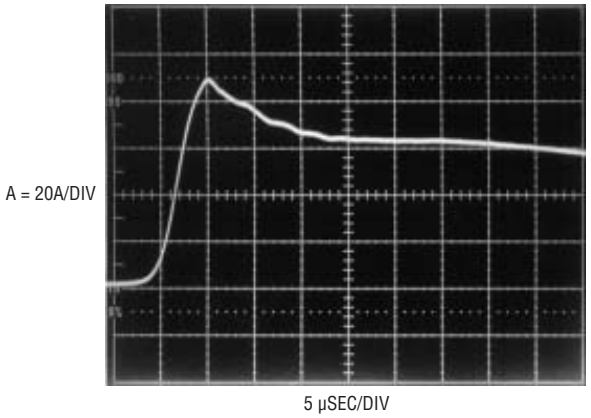


Figure 11 **The peak current of 90A is confined within 70-kHz bandwidth by 5-µsec rise time, minimizing noise concerns.**

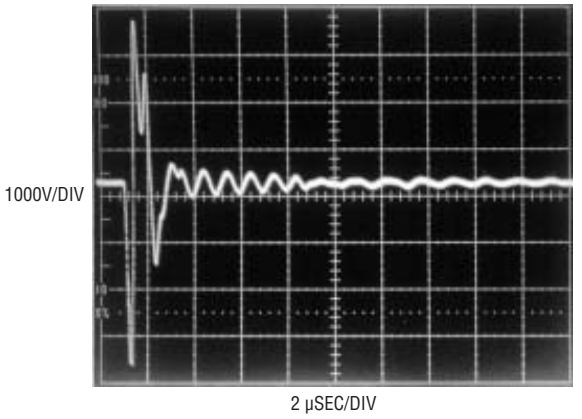


Figure 12 **Trigger pulses with high amplitude and fast rise time promote RFI, but energy and path exposure are small, simplifying radiation management.**

modates T_1's 300V output. The approximately 100A pulsed current flows in a tight, low-resistance loop from C_1's positive terminal, through the lamp, into Q_3, and back to C_1. In this case, lamp connections are made with wires, although modular flash-lamp-trigger transformers allow trace-based connections (**Reference 3**).

The flash circuit's pulsed high voltages and currents make RFI a concern. The capacitor's high-energy discharge is actually far less offensive than you might suppose. **Figure 11** shows that the 90A current peak of the discharge is confined to a 70-kHz bandwidth by its 5-µsec rise time. Therefore, there is little harmonic energy at radio frequencies, easing the RFI concern. Conversely, **Figure 12**'s T_2 high-voltage output has a 250-nsec rise time (bandwidth is approximately 1.5 MHz), qualifying it as a potential RFI source. Fortunately, the energy involved and the exposed path length are small, making interference management possible.

The simplest interference management you can use involves placing radiating components away from sensitive circuit nodes or employing shielding. Another option takes advantage of the predictable time when the flash circuit operates. You can blank sensitive circuitry within the telephone during flash events, which typically last much less than 1 msec.□

You can find a table listing standard transformers available for LT3468 circuits on the Web version of this article at www.edn.com.

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2. Wu, Albert, "Photoflash Capacitor Chargers Fit Into Tight Spots," Linear Technology.

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STANDARD TRANSFORMERS AVAILABLE FOR LT3468 CIRCUITS

For use with	Transformer name	Size (W×L×H, mm)	L_{PRI} (μH)	$L_{PRI-LEAKAGE}$ (nH)	N	R_{PRI} (mΩ)	R_{SEC} (Ω)	Vendor
LT3468/LT3468-2/	SBL-5.6-1	5.6×8.5×4.0	10	200 max	10.2	103	26	Kijima Musen, Hong Kong Office
LT3468-1	SBL-5.6S-1	5.6×8.5×3.0	24	400 max	10.2	305	55	852-2489-8266, kijimahk@netvigator.com
LT3468	LDT565630T-001	5.8×5.8×3.0	6	200 max	10.4	100 max	10 max	TDK, Chicago Sales Office
LT3468-1	LDT565630T--002	5.8×5.8×3.0	14.5	500 max	10.2	240 max	16.5 max	847-803-6100, www.components.tdk.com
LT3468-2	LDT565630T-003	5.8×5.8×3.0	10.5	550 max	10.2	210 max	14 max	
LT3468/LT3468-1	T-15-089	6.4×7.7×4.0	12	400 max	10.2	211 max	27 max	Tokyo Coil Engineering, Japan Office
LT3468-1	T-15-083	8.0×8.9×2.0	20	500 max	10.2	675 max	35 max	0426-56-6336, www.tokyo-coil.co.jp

Edited by Bill Schweber

Digitally control room light intensity

Donal McNamara, Analog Devices, Limerick, Ireland and Kieran Kelly, Analog Devices, Limerick, Ireland.

Many people favor different light and temperature settings for different rooms depending upon their mood or whether they are working or relaxing. The circuit in **Figure 1** controls the intensity of the artificial light in a room and monitors the temperature of two zones. The two main circuit blocks are the PIC16C67 master controller and the ADT7516 temperature-sensor interface, which includes a four-channel ADC and a quad voltage-output DAC. Other components include a photodiode and an op amp that monitor the ambient light; a rotary potentiometer that sets the light intensity; an LED bar array and display driver, which indicate the light-intensity setting; a light-dimmer-control circuit; and a 16×two-character LCD, which indicates the temperature of the two zones.

On power-up, the PIC16C67 configures its ports to control the LCD and the ADT7516. The ADT7516 has a dual interface, comprising I^2C and SPI, so the master communicates in SPI mode. The ADT7516 operates in SPI mode, once the controller initializes the LCD.

The ADT7516 senses both its internal temperature and the temperature of a remote thermal diode (Q_1 configured as a diode), and the PIC16C67 displays these temperatures on the LCD. One of the ADT7516's analog inputs monitors a potentiometer that you adjust to set the required light intensity. The PIC controller reads the potentiometer value from the ADT7516 and outputs a corresponding DAC value. The DAC controls an LM3914 LED-bar-array controller that shows the potentiometer setting on the array. If you set the potentiometer half-

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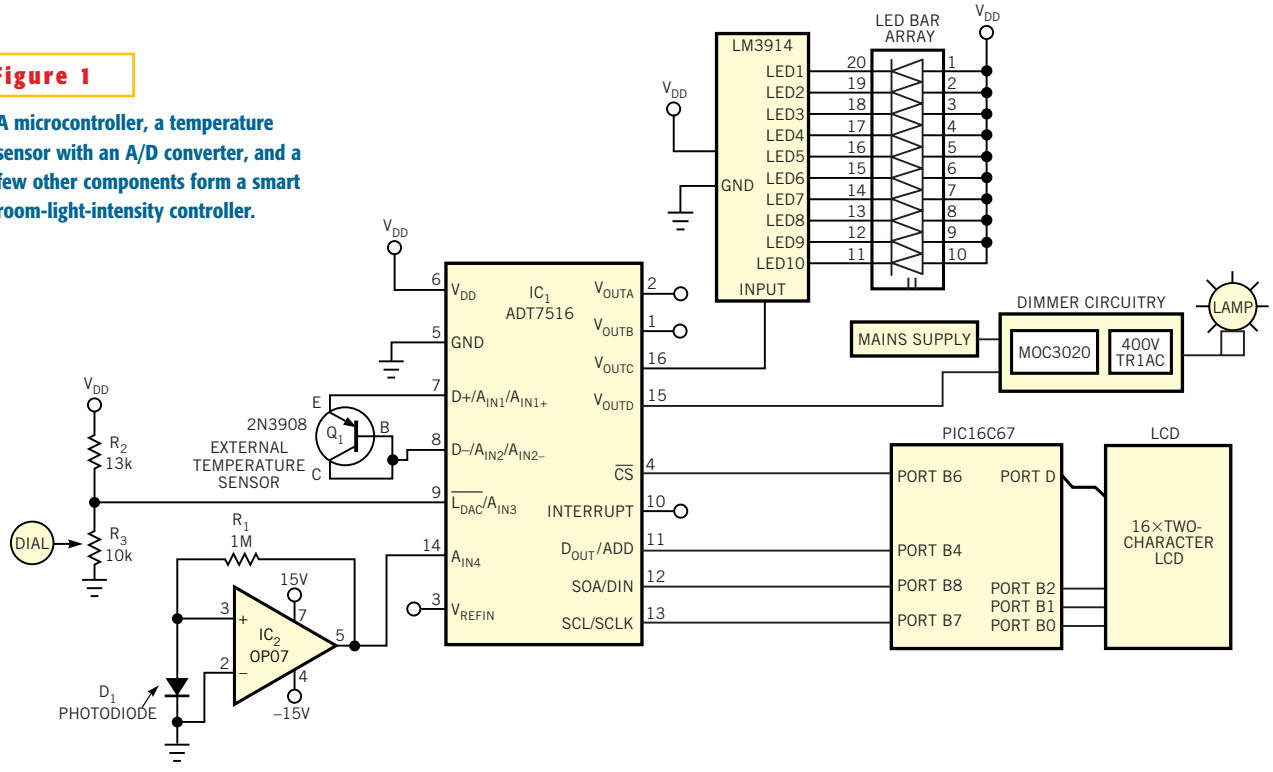
Figure 1

A microcontroller, a temperature sensor with an A/D converter, and a few other components form a smart room-light-intensity controller.



way, for example, then half of the LEDs turn on, indicating that you want an intensity that is half of what the light source can deliver.

A second DAC output controls a DIAC-based (X1) light-dimmer circuit. This dimmer circuit operates like any other light dimmer, except that the DAC controls it instead of a potentiometer. A photodiode monitors the intensity from the light bulb. An OP07 amplifies its output and feeds it into one of the ADT7516's analog inputs. The PIC controller uses the potentiometer and photodiode values, which the ADT7516 digitizes, to maintain equilibrium between the light intensity and the required light setting. If the photodiode reading is less than the potentiometer setting, the controller increases the dimmer DAC value; it decreases the dimmer DAC value if the reading is greater.

One of the features of the ADT7516 is its round-robin mode, in which it constantly monitors all of its measurement channels. The master need not initialize any conversions during its operation; all it has to do is read back from four value registers and act according to its program. This circuit ensures a constant light intensity within a room, saving power when daylight takes over as the main light source. It also extends the lifetime of a light bulb, thus saving on maintenance bills in a large office environment. You can also extend the application to include control of air conditioning and to memorize heat and light settings that suit individuals tastes.□

Circuit tests V_{COM} drivers

Soufiane Bendaoud, Analog Devices, San Jose, CA

Flat-panel LCD monitors offer excellent image quality and more compact form factor than CRTs—hence, their steadily increasing popularity. Unfortunately, the complexity of their manufacturing process makes LCD monitors considerably more expensive than CRTs. The amplifier that drives V_{COM}, the voltage on the backplane of the LCD panel, must be able to drive large capacitive loads, deliver high peak output currents, and maintain a constant output voltage. This Design Idea describes a simple test to measure the usefulness of an amplifier used as a V_{COM} driver. First, consider some video theory. Flat-panel television screens differ in the rate at which the screen refreshes. The refresh rate for TVs depends on the standard you use, such as NTSC, PAL, or SECAM. Computers, on the other hand, typically refresh the screen at a 75-Hz rate. A single picture element, or pixel, on an LCD screen comprises three subpixels, one each of red, green, and blue.

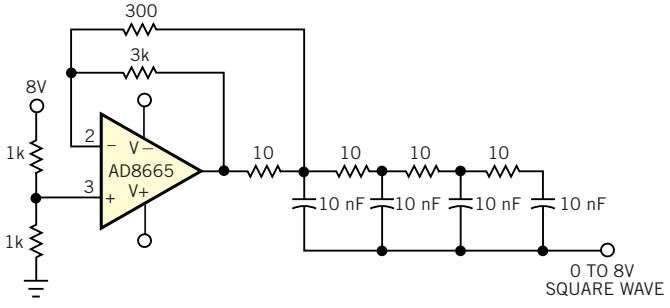


Figure 1 In this typical V_{COM} driver, an array of capacitors simulates the subpixel load.

Electrically, the subpixels behave like capacitors, storing a certain voltage until the next voltage arrives. Changing the voltages on the subpixels, one row at a time, refreshes the screen. These voltages use V_{COM} as a reference. The absolute value of the voltage differences, V_{COM}, represents the brightness of the subpixels. The video signal undergoes inversion on a frame-by-frame basis to ensure that the time average of the pixel voltages is zero, thus preventing screen burnout. The circuit of **Figure 1** tests the V_{COM} driver by applying a square wave to a capacitor array representing the subpixels in the panel. This circuit simulates the worst-case condition, in which all the subpixels switch on or off simultaneously. A pair of high-power, low-on-resistance MOSFETs generates the square wave. A nonoverlapping drive

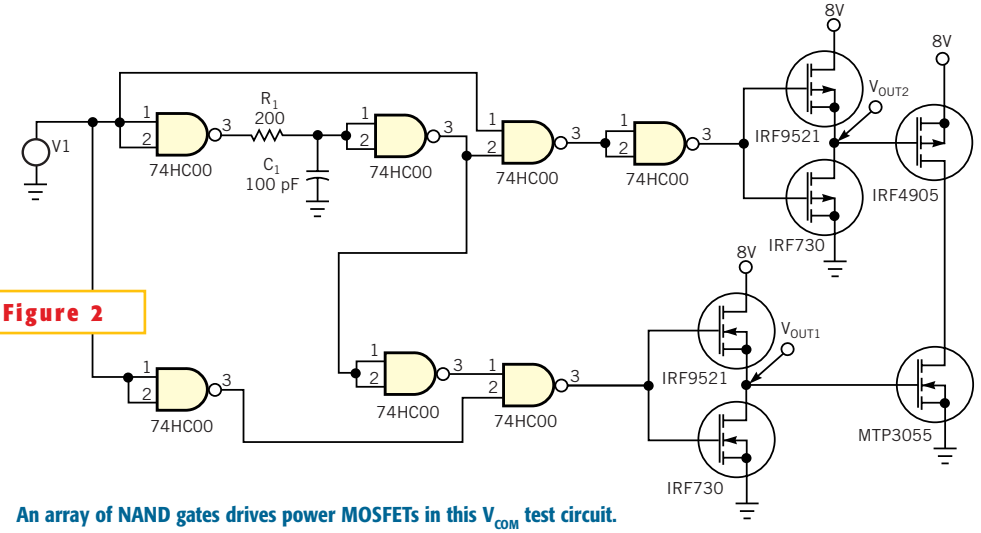


Figure 2 An array of NAND gates drives power MOSFETs in this V_{COM} test circuit.

scheme ensures that both MOSFETs do not turn on at the same time. Otherwise, simultaneous conduction would give rise to high shoot-through currents. **Figure 2** shows the MOSFETs and the nonoverlapping drive scheme. The drive scheme uses high-speed NAND gates. An RC network at the input of the second NAND gate controls the nonoverlap delay. The first pair of MOSFETs acts as predrivers to provide the current needed to drive the power-MOSFET output stage. **Figure 3** shows the nonoverlapping drive to the gates of the output stage. **Figure 4** shows the instantaneous peak output current of the AD8565 in **Figure 1** in response to a pulse from the test circuit.□

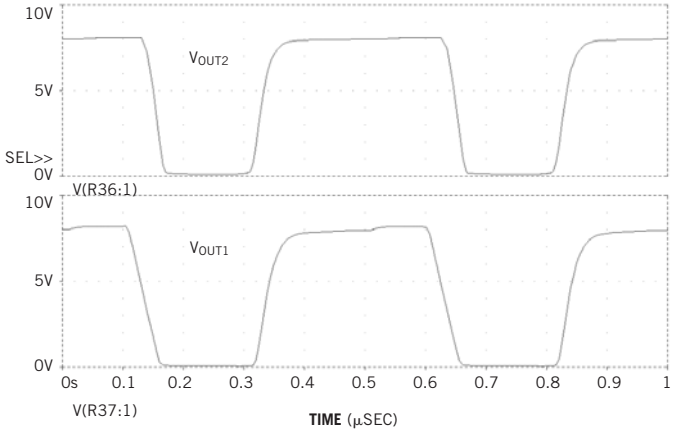


Figure 3 Nonoverlapping gate drive prevents large shoot-through currents in the output stage of Figure 2's circuit.

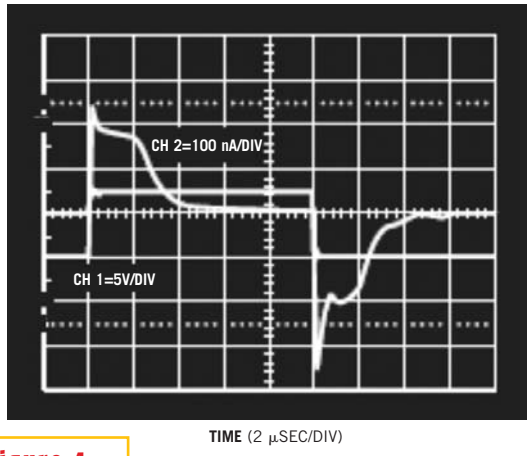


Figure 4 The AD8565 exhibits peak currents greater than 250 mA in response to a test-circuit pulse.

Use two picogate devices for bidirectional level-shifting

Bob Marshall, Philips Semiconductors

In new mixed-voltage systems, it is often necessary to level-shift a control signal from a high level to a low level. An open-drain device, such as the 74LVC1G07, easily performs this shift. However, when a bidirectional signal requires level-shifting, it takes a bit more circuitry, because simply tying two open-drain devices pins together generates just a latch function.

The circuit in **Figure 1** shows how to connect the 74LVC2G241 and 74LVC2G07 devices together to shift the signal at A from a high level to a low voltage at B and to shift a low level at B to a higher level at A. The $\overline{DIR}$ signal controls the direction of the transfer. When $\overline{DIR}$ is low, the A side is the input, and the B side is output. When $\overline{DIR}$ is high, B becomes the input, and A becomes the output. To have B behave as an input when the $\overline{DIR}$ signal is low, redo the circuit so that Pin 3 of the 74LVC2G241 becomes the input to Pin 1 of the 74LVC2G07 and Pin 4 of the 74LVC2G07 becomes the input to Pin 2 of the 74LVC2G241.

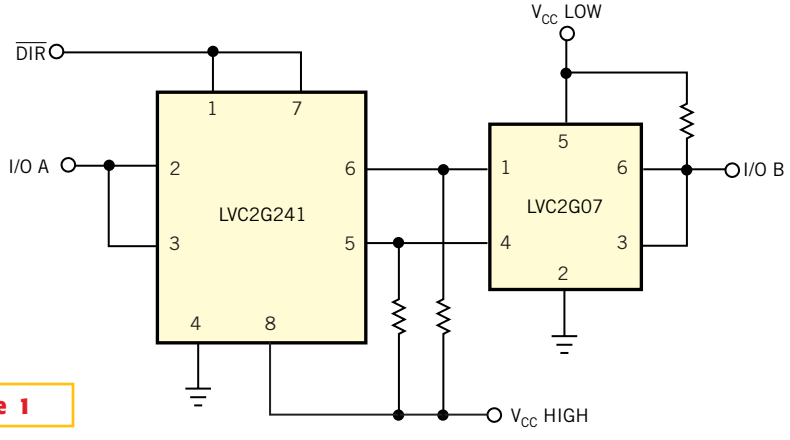


Figure 1 A two-IC circuit allows signal level-shifting in both directions; signal-flow direction is under circuit control.

The highest voltage V_{CC} should supply the 74LVC2G241, and the lowest voltage level supply necessary should supply the 74LVC2G07. For example, to shift a signal from 3.3 to 1.8V, the 1.8V_{CC} should supply the 74LVC2G07 device. The size

of the pullup resistor is unimportant, but, for best speed, it should be as small as practical to reduce the RC change time of the output signal of the 74LVC2G07. The current output of the74LVC07A is 24 mA at 3.3V; at that V_{CC}, the pullup resistor could be as low as 150Ω. It should be as large as possible to reduce power consumption.

The 74LVC2G07 supply level determines V_{OL} and V_{OH} at B. At 1.8V, the V_{OH} would be near V_{CC}, and V_{OL} is 0.45V or lower when driving a 4-mA load. The 74LVC2G07 and 74LVC2G241 provide a quick and easy way to obtain a bidirectional level translation and take up little board space.□

Simple nanosecond-width pulse generator provides high performance

Jim Williams, Linear Technology Corp

If you need to produce extremely fast pulses in response to an input and trigger, such as for sampling applications, the predictably programmable short-time-interval generator has broad uses. The circuit of **Figure 1**, built around a quad high-speed comparator and a high-speed gate, has settable 0- to 10-nsec output width with 520-psec, 5V transitions. Pulse width varies less than 100 psec with 5V supply variations of 65%. The minimum input-trigger width is 30 nsec, and input-output delay is 18 nsec.

Comparator IC_1 inverts the input pulse (**Figure 2**, Trace A) and isolates the 50Ω termination. IC_1's output drives fixed and variable RC networks. Programming resistor R_G primarily determines the networks' charge-time difference and, hence, delay at a scale factor of approx 80Ω/nsec.

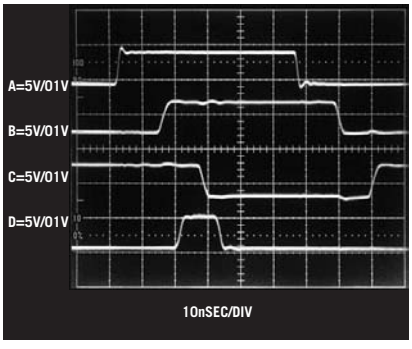


Figure 2 Pulse-generator waveforms, viewed in 400-MHz real-time bandwidth, include input (Trace A), IC_3 (Trace B) fixed and IC_2 (Trace C) variable outputs and output pulse (Trace D). RC networks differential delay manifests as IC_2-IC_3 positive overlap. G_1 extracts this interval and presents circuit output.

Comparators IC_2 and IC_3, arranged as complementary-output-level detectors, represent the networks' delay difference as edge-timing skew. Trace B is IC_3's fixed-path output, and Trace C is IC_2's variable output. Gate G_1's output (Trace D), which is high during IC_2-IC_3 positive overlap, presents the circuit output pulse. **Figure 2** shows a 5V, 5-nsec width, measured at 50% amplitude, output pulse with R=390Ω. The pulse is clean and has well-defined transitions. Post-transition aberrations, within 8%, derive from G_1's bond-wire inductance and an imperfect

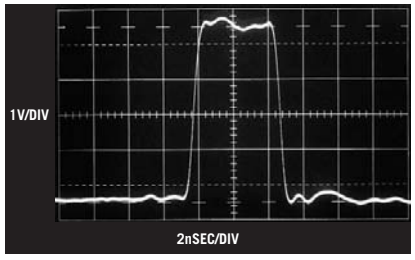


Figure 3 The 5-nsec-wide output with R=390Ω is clean with well-defined transitions. Post-transition aberrations are within 8% and derive from G_1 bond-wire inductance and an imperfect coaxial probe path.

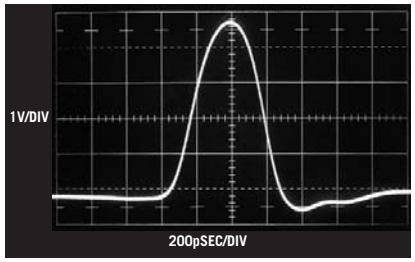


Figure 4 The narrowest amplitude pulse width is 1 nsec, and the base width measures 1.7 nsec. Measurement bandwidth is 3.9 GHz.

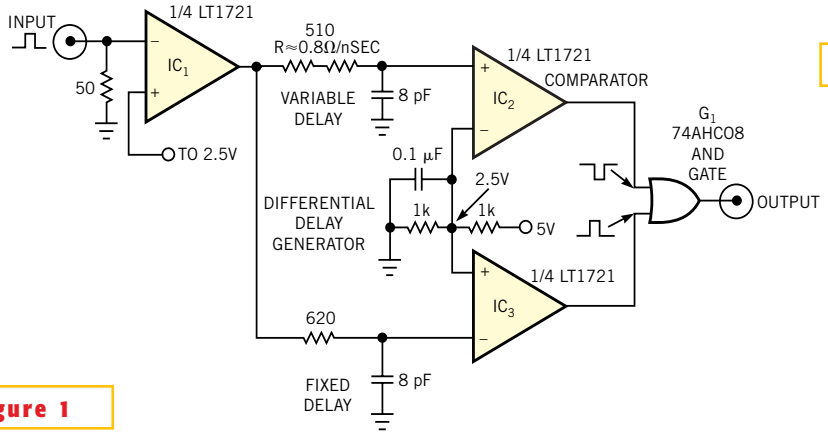


Figure 1 This pulse generator has 0- to 10-nsec width and 520-psec transitions. IC_1 unloads termination and drives the differential delay network. The IC_2-IC_3 complementary outputs represent delay difference as edge timing skew. G_1, which is high during IC_2-IC_3's positive overlap, presents circuit output.

coaxial probing path. **Figure 3** shows the narrowest full amplitude, 5V pulse available. Width measures 1 nsec at the 50% amplitude point and 1.7 nsec at the base in a 3.9-GHz bandwidth. Shorter widths are available if partial amplitude pulses are acceptable. **Figure 4** shows a 3.3V, 700-psec width (50%) with a 1.25-nsec base. G_1's rise time limits minimum achievable pulse width. The partial-amplitude pulse, 3.3V high, measures 700 psec with a 1.25-nsec base (**Figure 5**). **Figure 6**, taken in a 3.9-GHz sampled bandpass, measures 520-psec rise time. Fall time is similar. The transition of the probe edge is well-defined and free of artifacts.□

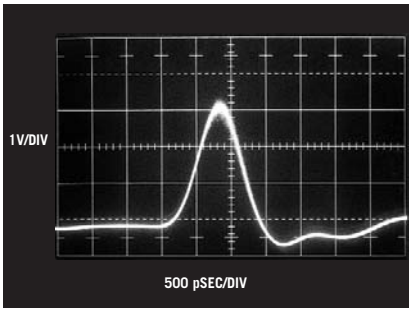


Figure 5 The partial-amplitude pulse, 3.3V high, measures 700 psec wide with a 1.25-nsec base. The trace granularity is an artifact of the 3.9-GHz-sampling-oscilloscope operation.

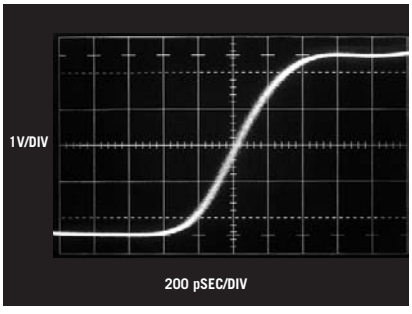


Figure 6 A transition detail in the 3.9-GHz bandpass with rise time of 90 psec shows 520-psec rise time; fall time is similar. The granularity derives from sampling-oscilloscope operation.

Accurately measure resistance with less-than-perfect components

Dave Van Ess, Cypress Semiconductor

For transducers, such as strain gauges or thermistors, you must accurately and inexpensively measure resistance using circuitry built with imperfect components and in which gain and offset errors can significantly limit the accuracy of ohmic measurements. The right circuit topology makes it possible to eliminate most error terms while measuring ohms, leaving the accuracy to be determined by just a single reference resistor.

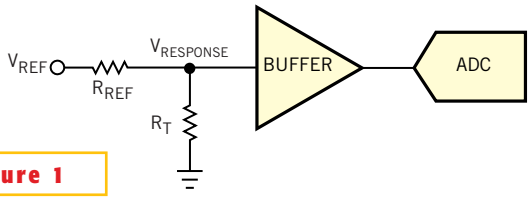


Figure 1 The resistive-divider topology provides a lower cost alternative to a current source and a precision resistor for calibration.

Unlike measuring voltage or current, measuring a passive attribute, such as resistance, requires a stimulus. One method of measuring resistance is to force a known current through a resistor and measure the voltage across the resistor. Measuring ohms in this way means that, with the correct selection of stimulus current, you need do no math, so this method was popular when the cost of computation was more than the cost of building an accurate current source. However, the accuracy of the current source directly limits the accuracy of the reading and any gain or offset errors from measuring the response voltage offsets the accuracy, as well. Additionally, the range of measurement is limited to the ADC's signal range, as the following equation shows:

$$R_T(MAX) = \frac{V_{RESPONSE}(MAX)}{I_{STIM}}.$$

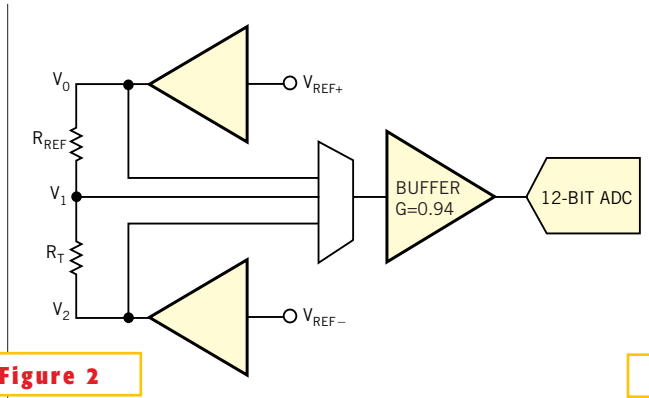


Figure 2 Remove most gain and offset errors using two measurements and a ratio calculation.

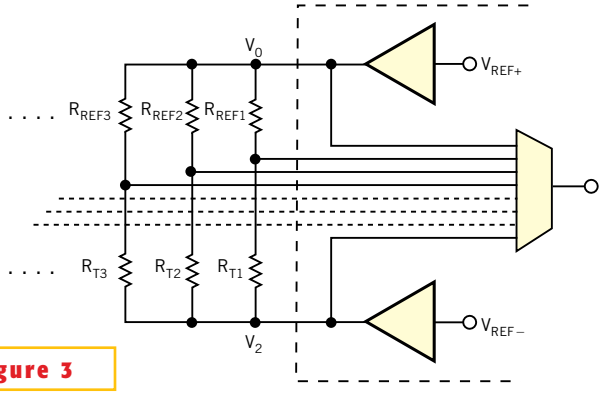


Figure 3 Extend the idea to handle multiple sensors and signal paths, using multiplexing through a single buffer and A/D converter.

With the development of more powerful microcontrollers and on-chip ratiometric ADCs, a resistor-divider block architecture (**Figure 2**) provides a less expensive approach:

$$R_T = R_{REF} \times \frac{V_{RESPONSE}}{V_{REF} - V_{RESPONSE}}.$$

This architecture has a theoretical range of measurement from short circuit to open circuit, but any offset error from measuring the response voltage limits the actual range; the reference resistance limits overall accuracy and any gain and offset errors from measuring the response voltage.

The cost of the reference resistor determines the error that the reference resistor introduces, and you derive the supply voltage, V_{CC}, from the reference voltage, V_{REF}. The gain error of a ratiometric ADC is generally small and does not contribute much to the overall error, but this situation is not the case for the offset error, which can be the largest contributor of error to the overall accuracy. Using more expensive and precise components reduces the offset error of any op amps in the measurement path.

Figure 2 shows how to significantly remove gain and offset errors, in which subtracting two measured voltages removes any offset errors in the measurement system:

$$R_T = R_{REF} \times \left(\frac{V_1 - V_2}{V_0 - V_1} \right).$$

The ratio of these two difference values removes any measurement-path gain error, leaving the reference resistance to determine the measurement error. This result is valid as long as the measured signal is never outside the range of the A/D converter. To guarantee this condition, set the sense buffer gain to slightly less than unity.

You can also measure multiple resistors, in which all the sense paths multiplex to a single buffer and A/D converter, and the eight analog pins let you measure as many as six transducers (**Figure 3**). Alternatively, you could connect each of four sense paths to its own buffer and converter.

Listing 1 at the Web version of this Design Idea at www.edn.com shows how you implement the circuit of **Figure 2** using a programmable analog system-on-chip controller. It uses the ADCINC12 user module, programmable-gain-adjustment user module, and two analog output buffers. Placing the analog block of the ADCINC12 just below the buffer and setting the clock for the ADCINC12 to 167 kHz for a sample rate of 10 samples/sec remove any 50- or 60-Hz interference from the signal. Increase the sample rate if the application requires a faster conversion. The control software is in C; the program calculates the resistance reading and leaves it in a global memory location.□

Simple nanosecond-width pulse generator provides high performance

Jim Williams, Linear Technology Corp

If you need to produce extremely fast pulses in response to an input and trigger, such as for sampling applications, the predictably programmable short-time-interval generator has broad uses. The circuit of **Figure 1**, built around a quad high-speed comparator and a high-speed gate, has settable 0- to 10-nsec output width with 520-psec, 5V transitions. Pulse width varies less than 100 psec with 5V supply variations of 65%. The minimum input-trigger width is 30 nsec, and input-output delay is 18 nsec.

Comparator IC_1 inverts the input pulse (**Figure 2**, Trace A) and isolates the 50Ω termination. IC_1's output drives fixed and variable RC networks. Programming resistor R_G primarily determines the networks' charge-time difference and, hence, delay at a scale factor of approx 80Ω/nsec.

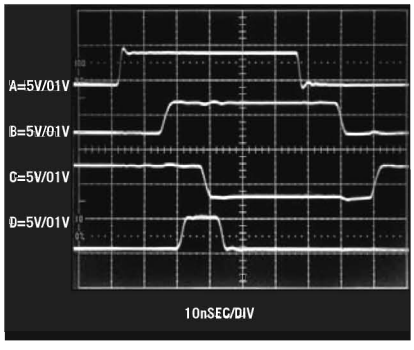


Figure 2 Pulse-generator waveforms, viewed in 400-MHz real-time bandwidth, include input (Trace A), IC_3 (Trace B) fixed and IC_2 (Trace C) variable outputs and output pulse (Trace D). RC networks differential delay manifests as IC_2-IC_3 positive overlap. G_1 extracts this interval and presents circuit output.

Comparators IC_2 and IC_3, arranged as complementary-output-level detectors, represent the networks' delay difference as edge-timing skew. Trace B is IC_3's fixed-path output, and Trace C is IC_2's variable output. Gate G_1's output (Trace D), which is high during IC_2-IC_3 positive overlap, presents the circuit output pulse. **Figure 2** shows a 5V, 5-nsec width, measured at 50% amplitude, output pulse with R=390Ω. The pulse is clean and has well-defined transitions. Post-transition aberrations, within 8%, derive from G_1's bond-wire inductance and an imperfect

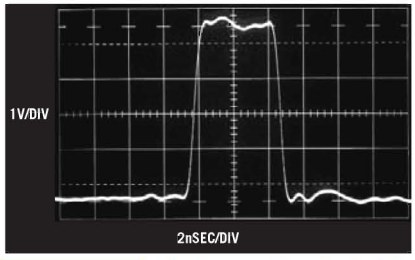


Figure 3 The 5-nsec-wide output with R=390Ω is clean with well-defined transitions. Post-transition aberrations are within 8% and derive from G_1 bond-wire inductance and an imperfect coaxial probe path.

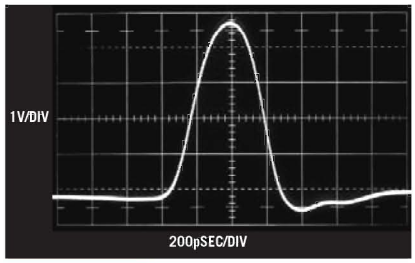
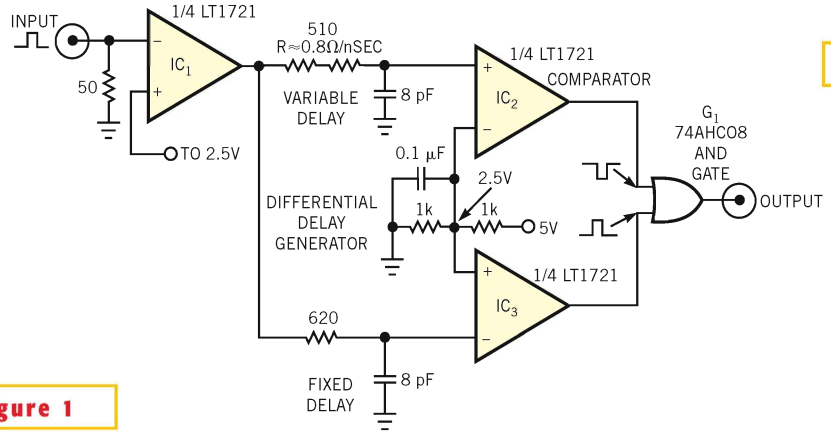


Figure 4 The narrowest amplitude pulse width is 1 nsec, and the base width measures 1.7 nsec. Measurement bandwidth is 3.9 GHz.



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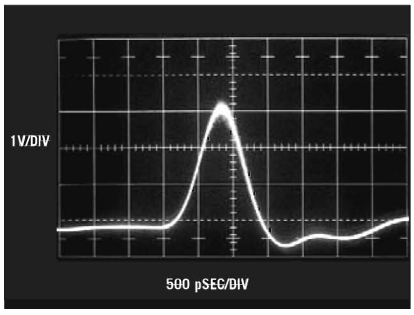

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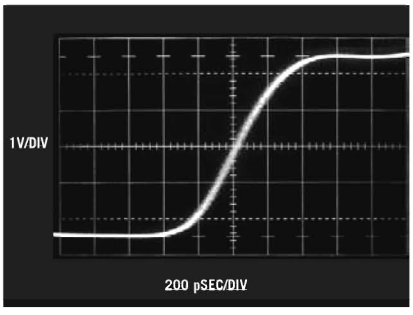

Figure 6 A transition detail in the 3.9-GHz bandpass with rise time of 90 psec shows 520-psec rise time; fall time is similar. The granularity derives from sampling-oscilloscope operation.

Edited by Brad Thompson

Power up a microcontroller with pre-power-down data

Stephan Roche, Santa Rosa, CA

It is sometimes necessary to retrieve data at power-up in the same way that they were at the last power-down, so that the product wakes up in the state it had before shutdown or to retrieve some measurement. One approach is to save critical variables into EEPROM or flash memory as soon as they change. This approach is generally not a good idea, because flash is typically limited to 100,000 write cycles, and EEPROM is typically limited to 1 million cycles. These numbers may seem large, but a product can easily reach them during their lifetimes.

Another approach is to use a battery to keep the microcontroller supplied so that it doesn't lose its RAM contents. This Design Idea presents an alternative option: detecting a power-down and triggering an interrupt routine that saves all the parameters in EEPROM or flash before the microcontroller supply falls below the operating threshold. **Figure 1** implements such an approach for a PIC18F6720 microcontroller.

One of the many features of this microcontroller is its low-voltage detection, which can trigger an interrupt when its LVD input goes below a threshold. You can set the threshold at 2.06V to 4.64V.

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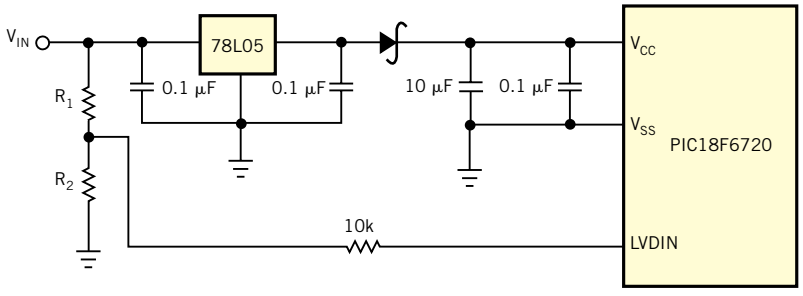


Figure 1 Use a power-down-detection scheme with a PIC18F6720 to save data before the microcontroller ceases to function.

The PIC18 microcomputer ceases functioning when its voltage supply is less than 4.2V. Because the EEPROM/flash-saving cycle is fairly time-consuming, the tactic is to monitor the voltage at the input of the 5V regulator to detect the power drop even before the microcomputer's supply starts to drop.

Select the LVD trip point inside the PIC18F6720 to be 1.22V, and calculate the required value of R_2/R_1 with the following equation:

$$\frac{R_1}{R_2} = \frac{V_{IN\_THRESHOLD}}{1.22} - 1,$$

where $V_{IN\_THRESHOLD}$ is the trip point below which a "data-save" function triggers. You should select this trip point to be as high as possible but not too high to avoid triggering on the ripples and noise on V_{IN-}.

Figure 2 shows the V_{IN} and V_{CC} waveforms when a power-down occurs. The ΔT represents the time allowed for saving data, which starts when the circuit detects the drop of V_{IN} and finishes when the voltage on the microcontroller goes below 4.2V, at which point it ceases to function. If the same 5V supply powers other devices , add a Schottky diode in series to ensure sufficient energy storage for the microcontroller to save the data. **Listing 1** in the Web version of this article at www.edn.com contains the assembly code that saves the data when a power-down occurs and retrieves the saved data at power-up.□

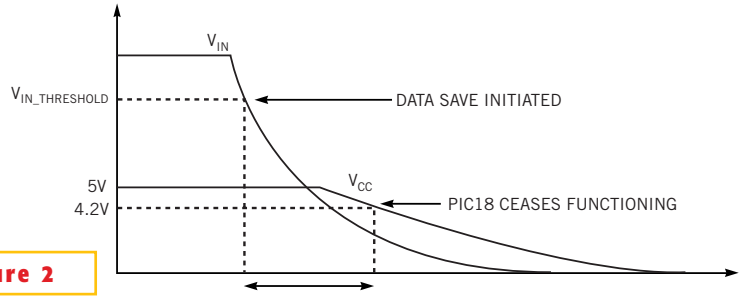


Figure 2 The V_{CC} and V_{IN} waveforms at power-down indicate the relationships in the sequence of events.

Power MOSFET is core of regulated-dc electronic load

Ausias Garrigós and José M Blanes, University Miguel Hernández, Electronic Technology Division, Elche, Spain

Designers use electronic dc loads for testing power supplies and sources, such as solar arrays or batteries, but commercial ones are often expensive. By using a power MOSFET in its linear region, you can build your own (**Figure 1**). It uses two simple feedback loops to allow the transistors to work as a current drain in current-regulation mode or as a voltage source in voltage-regulation mode. Designers use current-regulation mode when they are characterizing voltage sources, in which the power source must deliver current value that is set in the electronic load. They use voltage-regulation mode with current sources because it forces the sources to operate at a voltage that the load sets.

In current mode, R_{SHUNT} senses I_{LOAD}, and the resultant voltage feeds back to the inverting input of op amp IC_{1A}. Because the dc gain of this amplifier is high in the linear-feedback operating range, the inverting input stays equal to the

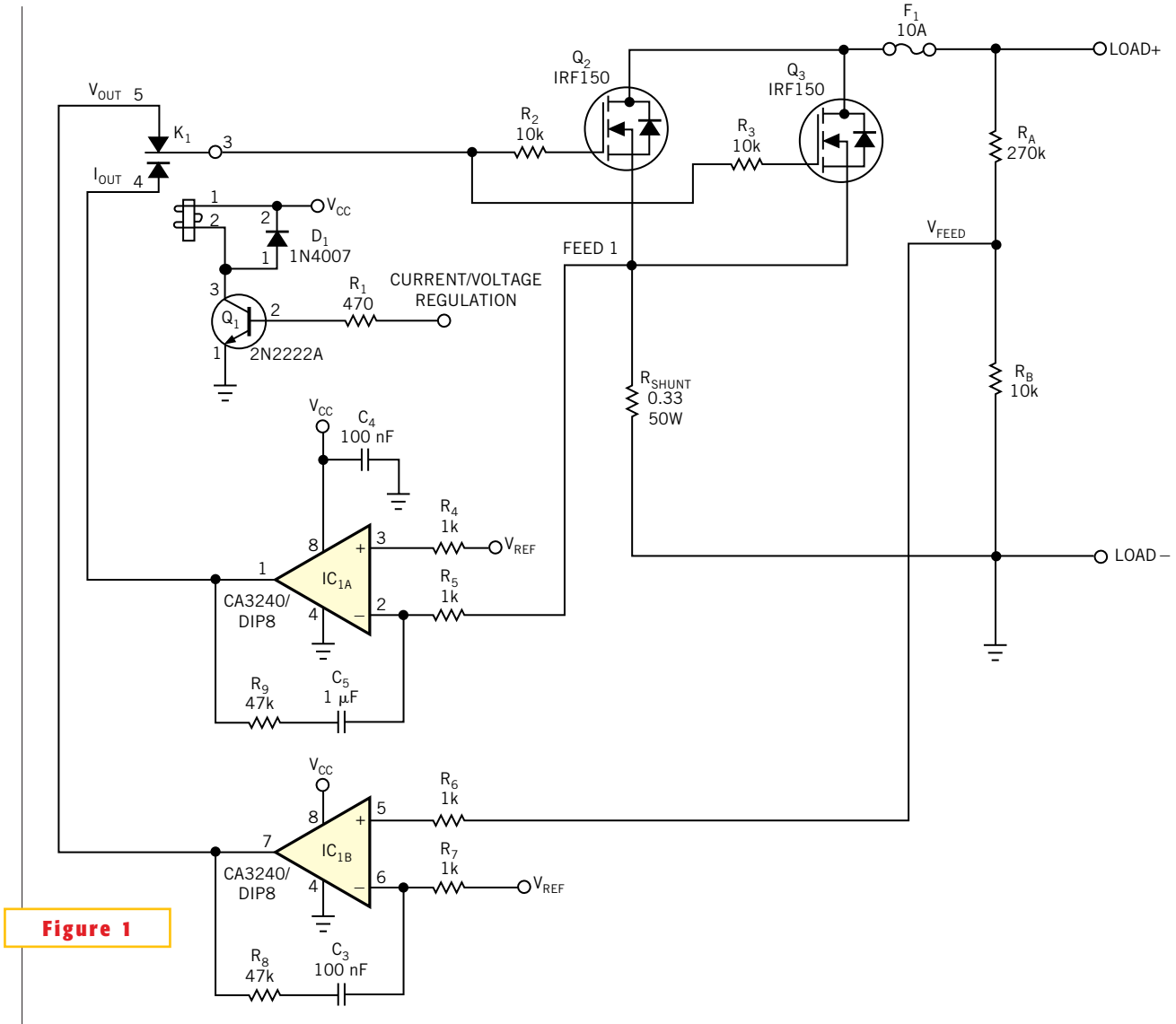


Figure 1

Using MOSFETs and a relay, this electronic load can operate in both current- and voltage-regulation modes.

noninverting input, which corresponds to V_{IREF}. The amplifier establishes its output value to operate MOSFETs Q_2 and Q_3 in a linear region and, therefore, dissipate the power from the source. The value of the source current is proportional to the current-loop reference, V_{IREF}, and is $I_{LOAD}=V_{IREF}/R_{SHUNT}$. Set V_{IREF} using a resistive voltage divider connected to a stable reference, or use the output of a D/A converter from a PC-based I/O card for flexible configuration.

Voltage-operating mode is similar, but now the sensed variable is the output voltage, which voltage divider R_A/R_B attenuates, so that the electronic load can operate at higher voltages than the op-amp supply voltage. The sensed voltage feeds back to the noninverting input of IC_{1B}, and the MOSFETs again operate in the linear region. Load voltage $V_{LOAD}=V_{VREF}\times(R_A+R_B)/R_B$.

The dual-op-amp CA3240, IC_1, can operate with an input voltage below its negative supply rail, which is useful for single-supply operation, but you can use any op amp if you have a symmetrical supply. Relay K_1 switches operating mode through a digital control line driving Q_1. The MOSFET is critical; you can add the IRF150 devices this design uses in parallel to increase the current-handling capabilities due to their positive-temperature coefficient, which equalizes the current flowing in the parallel MOSFETs. With the two MOSFETs in the circuit, the load handles 10A, and power consumption is greater than 100W, so using a heat sink and small fan is a good idea.

This circuit is useful for characterizing photovoltaic modules, which have two source modes. With this circuit and a PC-based setup, the I-V characteristic of a photovoltaic module from Helios Technology (www.heliostechnology.com) shows a region above V_{MPP} (voltage in the maximum point), at which a sharp transition corresponds to a voltage source (**Figure 2**). At voltages below V_{MPP}, the photovoltaic modules look like a current source. It is normally difficult to characterize this flat region of the curve with a simple current-mode electronic load, because the voltage output is sensitive to small variations in current, and thus a constant-voltage mode load is a better choice.□

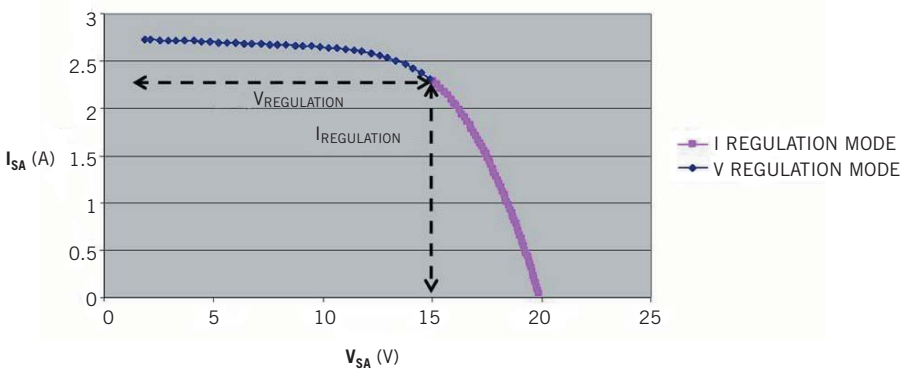


Figure 2 The I-V characteristics of a photovoltaic module, using the electronic load, show the special attributes of these power sources.

Use PSpice to model distributed-gap cores

Jeff Fries, GE Transportation Systems Global Signaling, Grain Valley, MO

PSpice software lets you create magnetic-core models that simulate nonlinear magnetic devices (**Figure 1**). These simulations are useful for observing hard-to-measure magnetic parameters such as core flux density, especially when you cannot quickly procure a sample device. The required inputs to the PSpice magnetic-core model are initial permeability of the core material, data points from the B-H magnetization curve, and the physical properties of the core, such as magnetic-path length, cross-sectional area, and air-gap length.

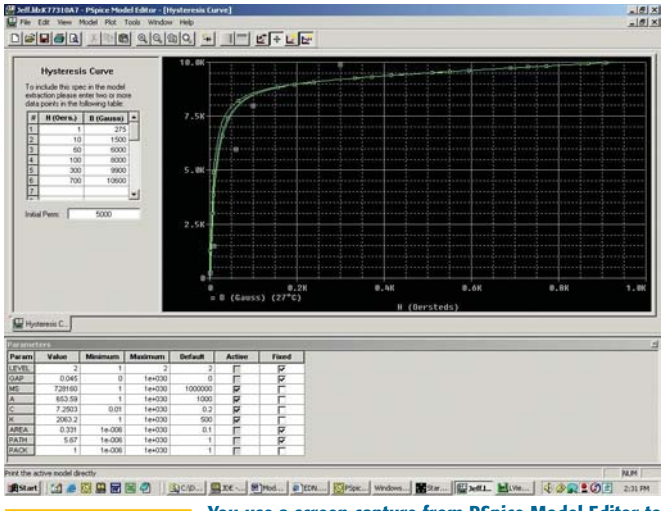


Figure 1 You use a screen capture from PSpice Model Editor to create a magnetic-core model.

All of the needed inputs for the magnetic-core model are typically available from core manufacturers' data sheets. However, in the case of a distributed gap with powder cores such as MPP or KoolMu, you need to determine the equivalent air gap to model the core using PSpice, because it relies on the air-gap length as input data to the model. Using the conservation of flux and manipulating Ampere's Law for a magnetic

circuit with an air gap result in: $1/U_E=(1/U_I)+(L_G/L_E)$, where U_E is the effective permeability of the core, U_I is the initial permeability of the core material, L_G is the length of the gap in centimeters, and L_E is the magnetic-path length of the core in centimeters. Assuming that the initial permeability, U_I, of the core is high, which is typical of distributed-gap cores, then the term $1/U_I$ drops out, and you can rearrange the equation to solve for the gap length as $L_G=L_E/U_E$. Using the magnetic-path length, L_E, and effective permeability, U_E, that the core manufacturer's data sheet specifies, calculate the equivalent air-gap length of the distributed gap-core for use in the PSpice model.

As an example, take the KoolMu 77310-A7 toroidal powder core from Magnetics Inc (www.mag-inc.com). Because the data sheet does not specify the initial permeability of the KoolMu core, arbitrarily use 5000. (This parameter is insignificant in the model due to the air gap.) Use the magnetization curve for the KoolMu material and mark the data points in **Table 1**.

Physical data for the 77310-A7 core shows a magnetic path length of 5.67 cm, cross-sectional area of 0.331 cm^2, and effective permeability of 125. From this data, you calculate the effective air-gap length of 0.045 cm. Enter this data into PSpice for the core model.

A quick and easy way to verify the accuracy of the model is to create an inductor in PSpice using your magnetic-core model. Place the inductor in a series-tuned RLC circuit (**Figure 2**). Using PSpice, run an ac sweep of the circuit, and use a probe to find the resonant frequency, f_{RES}. Using the resonant frequency, you can calculate the measured inductance of the PSpice model as $L_{MEAS}=1/(4\times\pi 2\times f_{RES}2\times C)$. If your magnetic-core model is correct, this should be close to the expected inductance calculated as $L_{EXP}=(N^2)\times A_L$, where N is the number of turns, and the core data sheet typically supplies the inductance factor, A_L.□

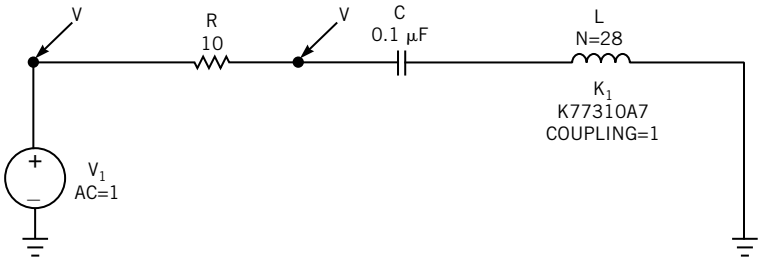


Figure 2 You can use this RLC-resonant circuit to measure the modeled inductance in PSpice, using an ac sweep analysis.

TABLE 1–DATA POINTS FOR KOOLMU CORE

B (Gauss)	H (Oersteds)
275	1
1500	10
6000	60
8000	100
9900	300
10,600	700

Precision divide-by-two analog attenuator needs no external components

Moshe Gerstanhaber and Chau Tran, Analog Devices, Wilmington, MA

Many modern A/D converters offer only a 5V input range, and using these converters with a ±5V or larger input signal gives the designer a problem: how to discard half of a good analog signal without introducing errors and distortion. To solve the problem, you can use an attenuator comprising two operational amplifiers and two resistors (**Figure 1**). However, this approach can reduce a system's performance by introducing gain errors due to amplifier offset and drift and resistor mismatch.

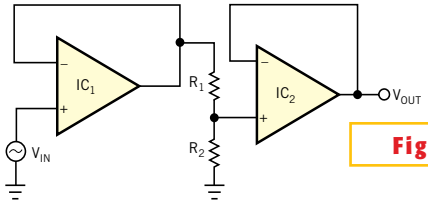


Figure 1 A conventional active voltage divider requires two op amps, IC_1 and IC_2, and two resistors, R_1 and R_2, that form a 2-to-1 voltage divider.

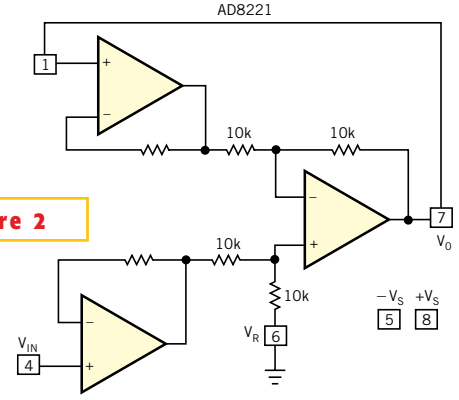


Figure 2 You can use an instrumentation amplifier to halve an analog signal's amplitude. All resistors are internal to the IC.

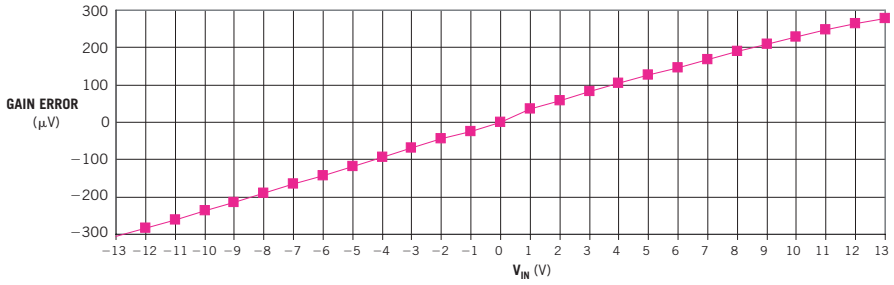
Figure 2 shows an alternative circuit that provides a precision gain of one-half with low offset, low drift, and low input-bias currents and that uses an AD8221 instrumentation amplifier.

The amplifier's output, V_O, equals the difference between the two inputs, V_{IN+} and V_{IN-}: $V_O=(V_{IN+})-(V_{IN-})$. Connecting the amplifier's output to its inverting input and substituting V_O for V_{IN-} yields: $V_O=(V_{IN+})-(V_O)$, or $V_O=(V_{IN+})$.

Thus, the circuit provides a precision gain of one-half with no external components and, in this configuration, is unconditionally stable. The performance plots of **figures 3** and **4**, respectively, show a gain error of less than 300 µV and a maximum nonlinearity error of about 1 ppm over a 26V input-voltage range.

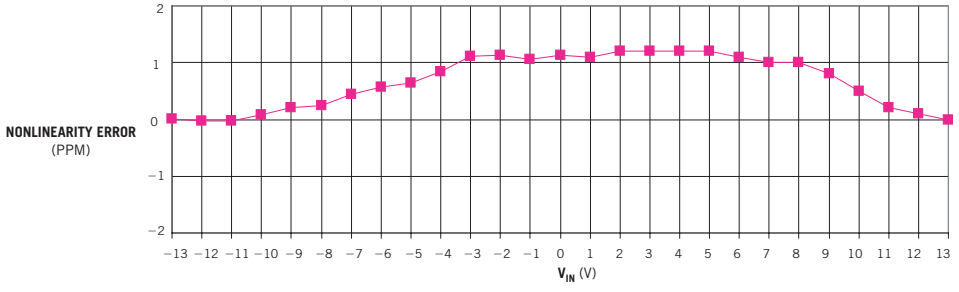
To introduce an offset voltage, V_{OS}, that equals half of a reference voltage ($V_{OS}=V_R/2$), connect the AD8221's reference input (Pin 6) to voltage V_R. To bias the attenuator's output at half of the positive- or negative-power-supply voltage, connect the reference pin to the appropriate power supply.□

Figure 3



The circuit in Figure 2 introduces a full-scale gain error of less than 300 µV over a 26V input-voltage range.

Figure 4



The circuit in Figure 2 introduces a maximum nonlinearity error of about 1 ppm over a 26V input-voltage range.

Quartz crystal-based remote thermometer features direct Celsius readout

Jim Williams and Mark Thoren, Linear Technology Corp

Although quartz crystals have served as temperature sensors, designers haven't taken advantage of the technology because few manufacturers offer the sensors as standard products (**references 1** and **2**). In contrast to conventional resistance- or semiconductor-based sensors, a quartz-based sensor provides inherently digital-signal conditioning, good stability, and a direct digital output that's immune to noise and thus ideally suited to remote-sensor placement (**Figure 1**, pg 100).

An economical and commercially available quartz temperature sensor, Y_1 and IC_1, an LTC-485 RS485 transceiver in transmitter mode, form a Pierce crystal oscillator. The sensor, an Epson HTS-206, presents a nominal frequency of 40 kHz at 25°C and a temperature coefficient of −29.6/ppm/°C (**Reference 3**). The transceiver's differential-line-driver outputs deliver a frequency-coded temperature signal over a twisted-pair cable at distances as far as 1000 ft.

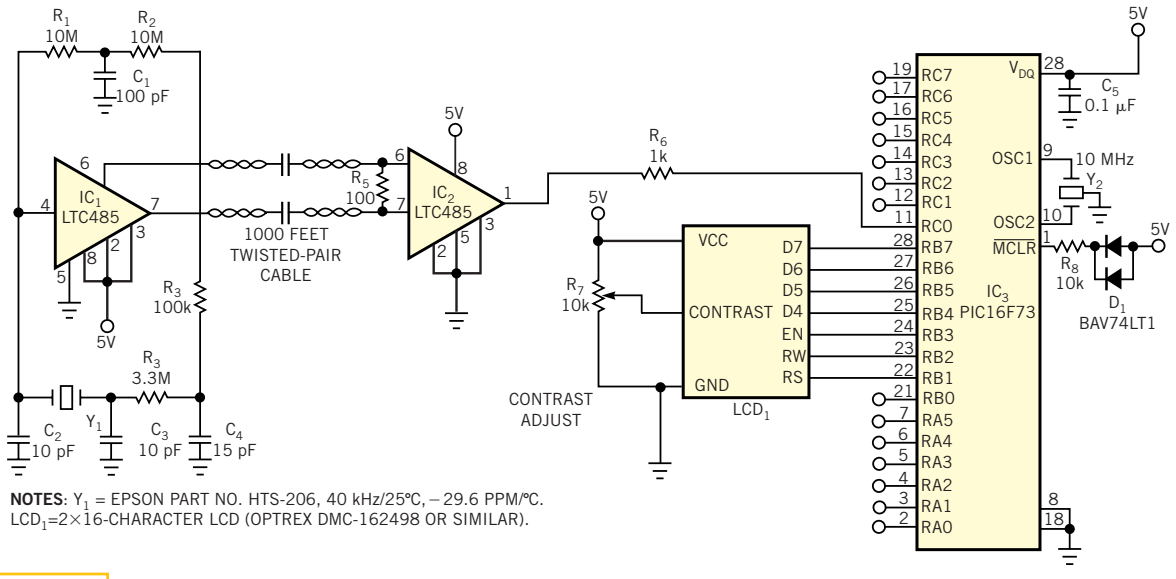
A second LTC-485, IC_2, in receiving mode, accepts the differential data and presents a single-ended output to IC_3, a PIC-16F73 processor that converts the frequency-coded temperature data and presents the temperature in Celsius format on LCD_1. You can view and download the conversion program's source code in the Web version of this Design Idea at www.edn.com.□

References

1. Benjamin, Albert, "The Linear Quartz Thermometer—A New Tool for Measuring Absolute and Differential Temperature," *Hewlett-Packard Journal*, March 1965.

2. Williams, Jim, "Practical Circuitry for Measurement and Control Problems," Application Note 61, August 1994, Linear Technology Corp.

3. HTS-206 specifications, Epson Corp, www.eea.epson.com.



NOTES: Y_1 = EPSON PART NO. HTS-206, 40 kHz/25°C, –29.6 PPM/°C.
LCD_1=2×16-CHARACTER LCD (OPTREX DMC-162498 OR SIMILAR).

Figure 1 A quartz-crystal temperature sensor provides Celsius-temperature readouts accurate to 2% over a −40 to +85°C range.

Quartz crystal-based remote thermometer features direct Celsius readout

Jim Williams and Mark Thoren, Linear Technology Corp

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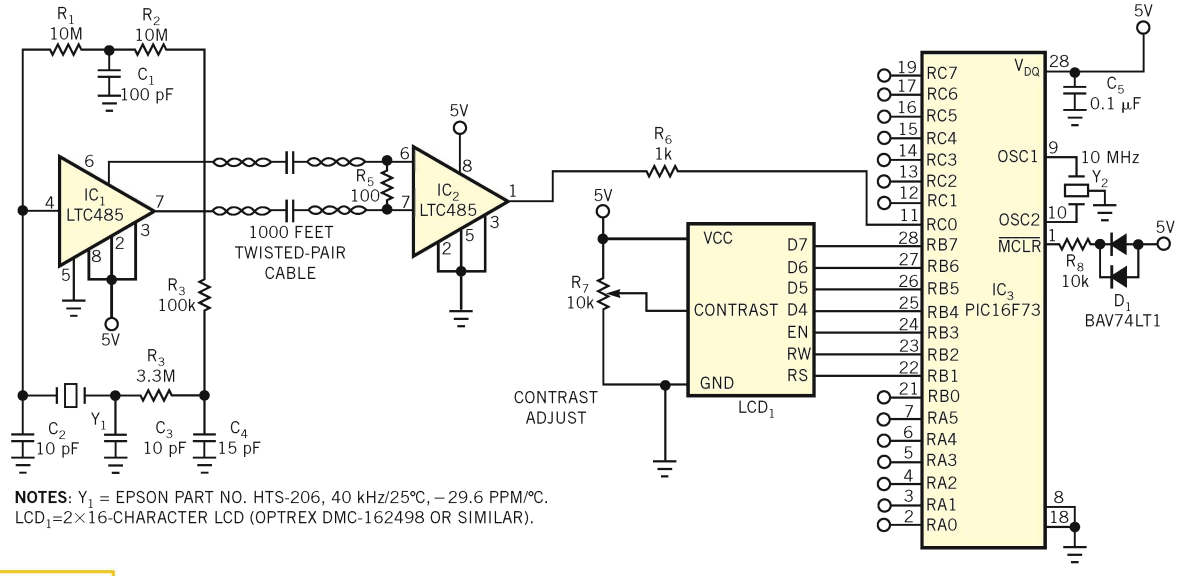

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Figure 1 A quartz-crystal temperature sensor provides Celsius-temperature readouts accurate to 2% over a −40 to +85°C range.

design ideas

Edited by Brad Thompson

Single-wire keypad interface frees microcontroller-I/O pins

Israel Schleicher, Prescott Valley, AZ

In most keypads, pressing a key closes a contact that bridges two lines in an xy matrix. If you use a microcontroller to detect a key closure, checking the states of (x+y) lines requires an equal number of I/O pins. Occupying only one free I/O pin, the circuit **Figure 1** communicates with a microcontroller by generating a single pulse each time someone presses a key. The pulse's width is proportional to the number of the pressed key, and the microcontroller identifies the pressed key by measuring the pulse's width.

IC_2, a CMOS LMC555 version of the popular 555 timer, operates as a monostable one-shot multivibrator. In the circuit's resting state, a transistor internal to IC_2 at Pin 7 shunts C_6, and IC_2's output at Pin 3 remains at logic low. Pressing any key on the keypad connects two resistors from two groups—R_1 and R_2 in one

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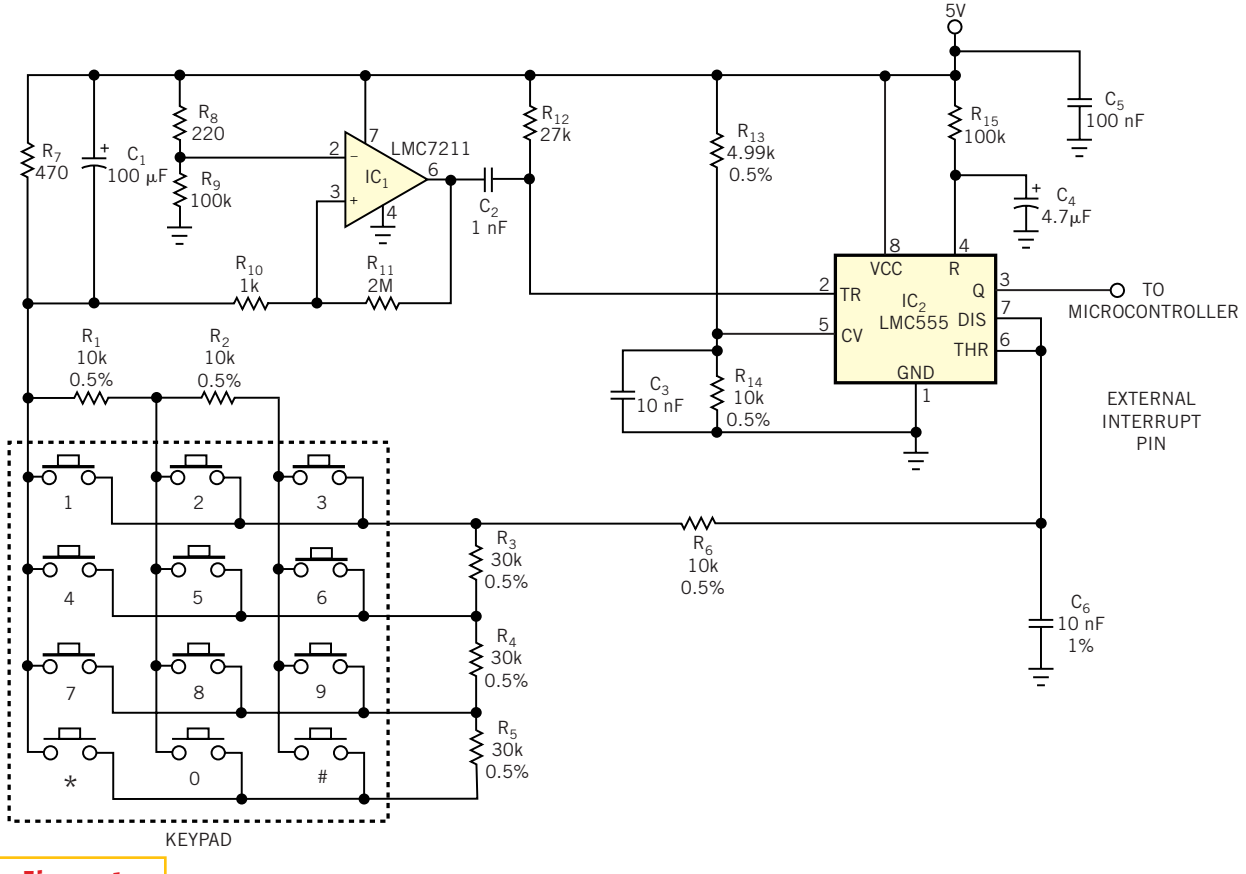

Figure 1 Two ICs form a pulse-width-modulated keypad interface that uses only one microcontroller-input pin.

group and R_3, R_4, and R_5 in the other—in series with R_6. The sum of the two resistors varies in 10-kΩ increments, and the total resistance is proportional to the number of the pressed key.

Pressing any key draws current through R_6, R_7, and the selected keypad resistors and raises the voltage at IC_2's Pin 7. After C_1 charges, introducing a short delay that's sufficient to eliminate keypad-switch contact-closure bounce, CMOS comparator IC_1 detects the small voltage drop established across R_7. The output of IC_1 (Pin 6) goes from 5 to 0V, which in turn triggers Pin 2 of IC_2. Timer IC_2's output (Pin 3) goes high and begins to charge capacitor C_6 at a time constant that depends on the selected key. When the voltage across C_6 reaches two-thirds of V_{CC}, or 3.333V, Pin 3 goes low and discharges C_6. The following equation calculates IC_2's output pulse width, T: $T = 1.1 \times R_S \times C_6$, where R_S equals the sum of the selected keypad resistors and ranges from 10 to 120 kΩ. The pulse width spans a range of 110 to 1320 μsec in increments of 110 μsec.

The smallest relative change in pulse width occurs at the longest pulse ratio, 110/1320, or 8.33%. This ratio provides sufficient margin to allow use of standard ±1% tolerance or better components for those in **Figure 1** that are ±0.5 and ±1%. Resistors R_{13} and R_{14} compensate for variations in IC_2's internal voltage dividers by forcing the voltage at Pin 5 to two-thirds of power-supply voltage V_{CC}.

The keypad circuit's output pulse drives the external interrupt input, RA_2, of a Microchip 16F630 microcontroller. **Listing 1**, available at the online version of this Design Idea at www.edn.com, presents an interrupt routine for the 16F630 that measures the pulse width, verifies that its tolerance is within ±40 μsec, and returns a numerical value of 1 to 12 that corresponds to the pressed key. As a safeguard against erroneous data, the routine returns an error code if the pulse width falls outside certain limits.□

Calculator program evaluates elliptic filters

Fernando Salazar-Martínez, Alan Altamirano-Cruz, and David Báez-López, Department of Engineering Electronics, University of the Americas, Puebla, Mexico

Many designers consider the elliptic-transfer function to be the most useful of all analog-filtering functions, because of its steep roll-off at the band edges. You can use a Texas Instruments model V200 Voyage programmable calculator and the program in **Listing 1** at the Web version of this Design Idea at www.edn.com to evaluate a lowpass elliptic filter by finding its characteristic's poles and zeros. To do so, this program implements Darlington's algorithm (**Reference 1**). The program accepts as input the filter's maximum passband-attenuation ripple in decibels, its stopband and passband frequencies in radians per second, and its order, or number of poles (**Figure 1**).

As an example, calculate the zeros, poles, and stopband attenuation of an elliptic, fifth-order, analog lowpass filter with maximum gain of 0.1 dB and stopband frequency of 1.05 radians/sec. **Figure 2** illustrates the calculator's display screens during program execution.□

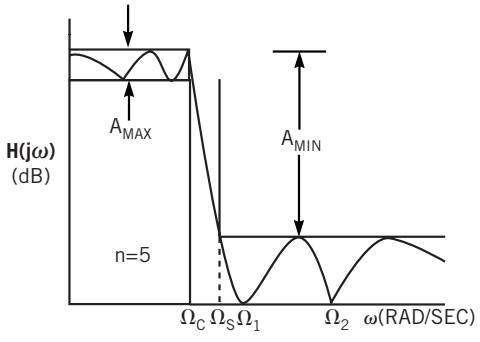

Figure 1 The characteristics of an elliptic filter's amplitude response include in-band ripple, passband-attenuation and stopband frequencies, and stopband attenuation.

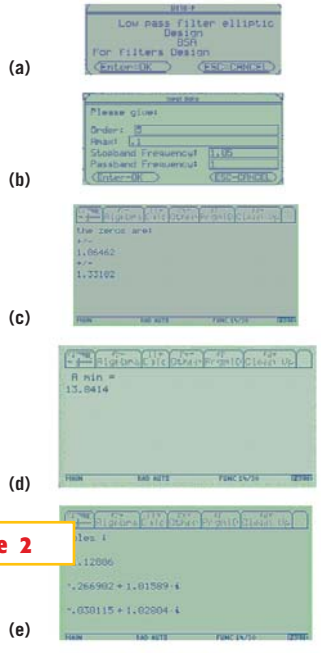

Figure 2 These screens show the calculator's display from the introductory menu (a), entering filter parameters (b), calculating values for filter-response zeros (c), calculating value for out-of-band attenuation (d), and calculating values for filter-response poles (e).

Reference

1. Darlington, Sidney, "Simple Algorithms for Elliptic filters and Generalizations Thereof," *IEEE Transactions on Circuits and Systems*, Volume CAS-25, No. 12, December 1978, pg 975.

Dynamic-load circuit determines a battery's internal resistance

Jim Williams, Linear Technology Corp, Milpitas, CA

THE SIMPLEST MODEL of a battery comprises an ideal voltage source that connects in series with a resistance whose value—often a few milliohms—depends on the battery's electrochemical condition and construction. If you attempt to use an ordinary ac milliohmmeter containing a kilohertz-range ac excitation source to measure a battery's internal resistance, you get erroneous results due to capacitive effects, which introduce losses. A more realistic battery model includes a resistive divider that a capacitor partially shunts (**Figure 1**). In addition, a battery's no-load internal resistances may differ significantly from their values under a full load. Thus, for greatest accuracy, you must measure internal resistance under full load at or near dc.

The circuit in **Figure 2** meets these requirements and accurately measures internal resistance over a range of 0.001 to 1Ω at battery voltages as high as 13V. One section of an LTC6943 analog switch, IC_{2A}, alternately applies 0.110 and 0.010V derived from 2.5V voltage reference IC_3 and resistive divider R_2, R_3, and R_4 to IC_1's input.

Amplifier IC_1, power MOSFET Q_1, and associated components form a closed-loop current sink that provides an active load for the battery under test via Q_1's drain. Diode D_1 provides reversed-bat-

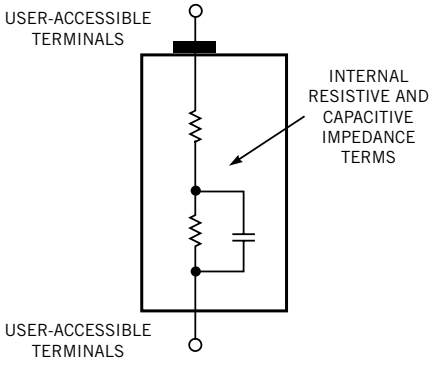

Figure 1 An elementary model of a battery's internal impedance includes resistive and capacitive elements, but the capacitive elements introduce errors in ac-based impedance measurements. For improved accuracy, analyze the battery's voltage drop at a frequency near dc.

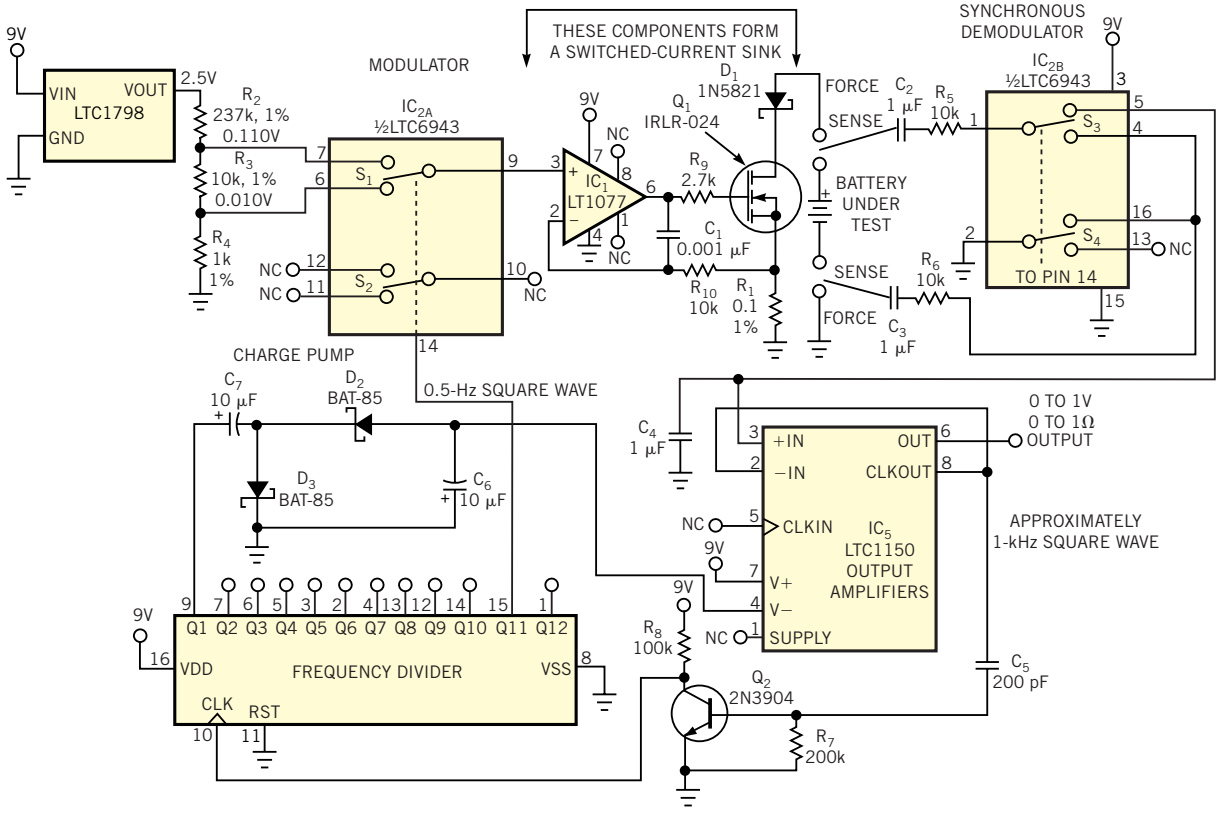

Figure 2 This circuit determines a battery's internal resistance by repetitively applying a calibrated discharge current and measuring the resultant voltage drop across the battery's terminals.

tery protection. The voltage at amplifier IC_1's positive input and the voltage drop across R_1 determine the load applied to the battery. In operation, the circuit applies a constant-current load comprising a 1A, 0.5-Hz square wave biased at 100 mA to the battery.

The battery's internal resistance develops a 0.5-Hz amplitude-modulated square-wave signal at the Kelvin connections attached to the battery. A synchronous demodulator comprising analog switches S_2 and S_3 in IC_{2B} and chopper-stabilized amplifier IC_5 processes the sensed signal and delivers a 0 to 1V analog output that corresponds to a battery-resistance range of 0 to 1Ω.

Via transistor Q_2, amplifier IC_5's internal approximately 1-kHz clock drives CMOS binary divider CD4040, IC_4, which supplies a 0.5-Hz square-wave clock drive for the switches in IC_2. In addition, a 500-Hz output from IC_4 powers a charge-pump circuit that delivers approximately −7V to IC_5's negative power-supply input and thus enables IC_5's output to swing to 0V.

The complete circuit consumes approximately 230 µA, allowing nearly 3000 hours of operation from a 9V alkaline-battery power supply. The circuit operates at a supply voltage as low as 4V with less than 1-mV output variation and provides an output accuracy of 3%. The circuit accommodates a battery-under-test voltage range of 0.9 to 13V, but you can easily alter discharge current and repetition rate to observe battery resistance under a variety of conditions.□

Battery automatic power-off has simpler design

Yongping Xia, Navcom Technology, Torrance, CA

A previous Design Idea describes a simple way to automatically turn off a battery after a preset on period to save battery life (**Reference 1**). This Design Idea presents a simpler way to perform the same function (**Figure 1**). Two gates of IC_1, a quad two-input NAND Schmitt trigger, form a modified flip-flop. When you apply a 9V battery to the circuitry, the output of IC_{1A} goes high because the initial voltage on C_1 is zero. The output of IC_{1B} is low, which feeds back to IC_{1A} through R_2. C_3 charges up through R_3. The output of IC_{1C} goes high because R_6 is connects to ground. A P-channel MOSFET switch, Q_1, is off, and the output IC_{1D} goes high, which in turn charges C_4 through R_2.

When you push momentary switch S_1, IC_{1A}'s output goes low because both of its inputs are high, and this output forces IC_{1B}'s output high. The value of R_2 is much smaller than R_3, so that C_3 holds a logic-level high when S_1 stays on. When S_1 goes off, C_3 discharges through R_3.

You can turn off the MOSFET switch in one of two ways. When tantalum capacitor C_2 is charged up such that the voltage on IC_{1C}'s input becomes lower than its threshold V−, IC_{1C}'s output changes from low to high; this action turns off the MOSFET switch. C_2 and R_6 determine the duration of this automat-

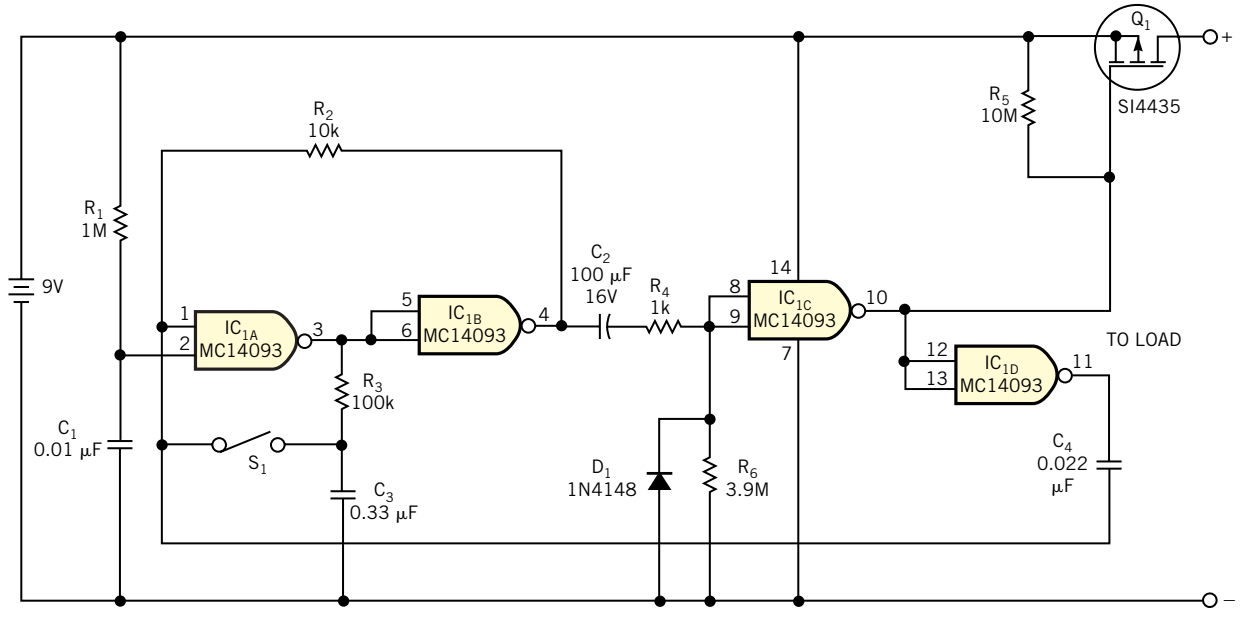

Figure 1 An improved power-off circuit automatically disconnects the battery after a preset on period.

ic turn-off. With the values shown, the turn-off takes approximately six minutes. Meanwhile, the high-to-low transition on IC_{1D}'s output forces IC_{1A} and IC_{1B} back to standby status through C_4.

Alternatively, you can manually turn off the MOSFET switch by pushing S_1. Because the voltage on C_3 is low, closing S_1 forces IC_{1A}'s outputs high and IC_{1B}'s outputs low. The high-to-low transition on IC_{1B}'s output forces IC_{1C}'s output to be high, which turns off the MOSFET. Because the value of C_2 is fairly large, D_1 provides a quick discharge route, and R_4 limits the discharge current.

This circuitry consumes less than 0.2 µA of power during standby operation. Because the MOSFET switch has a low on-resistance, it has only a 2-mV loss when the load current is 100 mA. Add an LED with a current-limiting resistor in series to the load side if you need a power-on indicator.□

Reference

1. Gimenez, Miguel, "Scheme provides automatic power-off for batteries," *EDN*, May 13, 2004, pg 92.

Control a processor's power supply in real time

Yogesh Sharma, Analog Devices, San Jose, CA

In battery-powered applications in which power management is key, a microprocessor may adjust its core voltage corresponding to an increase or a decrease in clock speed, allowing full processing power when necessary but not wasting excess power when idle. The circuit of **Figure 1** shows how an embedded processor can control its own supply voltage via a simple step-down converter and inexpensive digital potentiometer.

In this application, an embedded ADSP-BF531 Blackfin processor adjusts the wiper setting of IC_2, an AD5258 digital potentiometer, via its I^2C interface. In turn, IC_2 controls the output of IC_1, an ADP3051 current-mode, PWM step-down converter that supplies as much as 500 mA at output voltages as low as 0.8V. When its output is in regulation, IC_1's feedback input rests at 0.8V, and IC_2 and R_2 form a voltage divider.

The ADSP-BF531 imposes several design requirements: Its core power-supply voltage must maintain its accuracy to within 25 mV and offer an adjustment resolution of 50 mV per step from 0.8 to 1.2V. Also, the processor requires 1.2V at start-up to initialize its clocks. Finally, the power controller must prevent its output

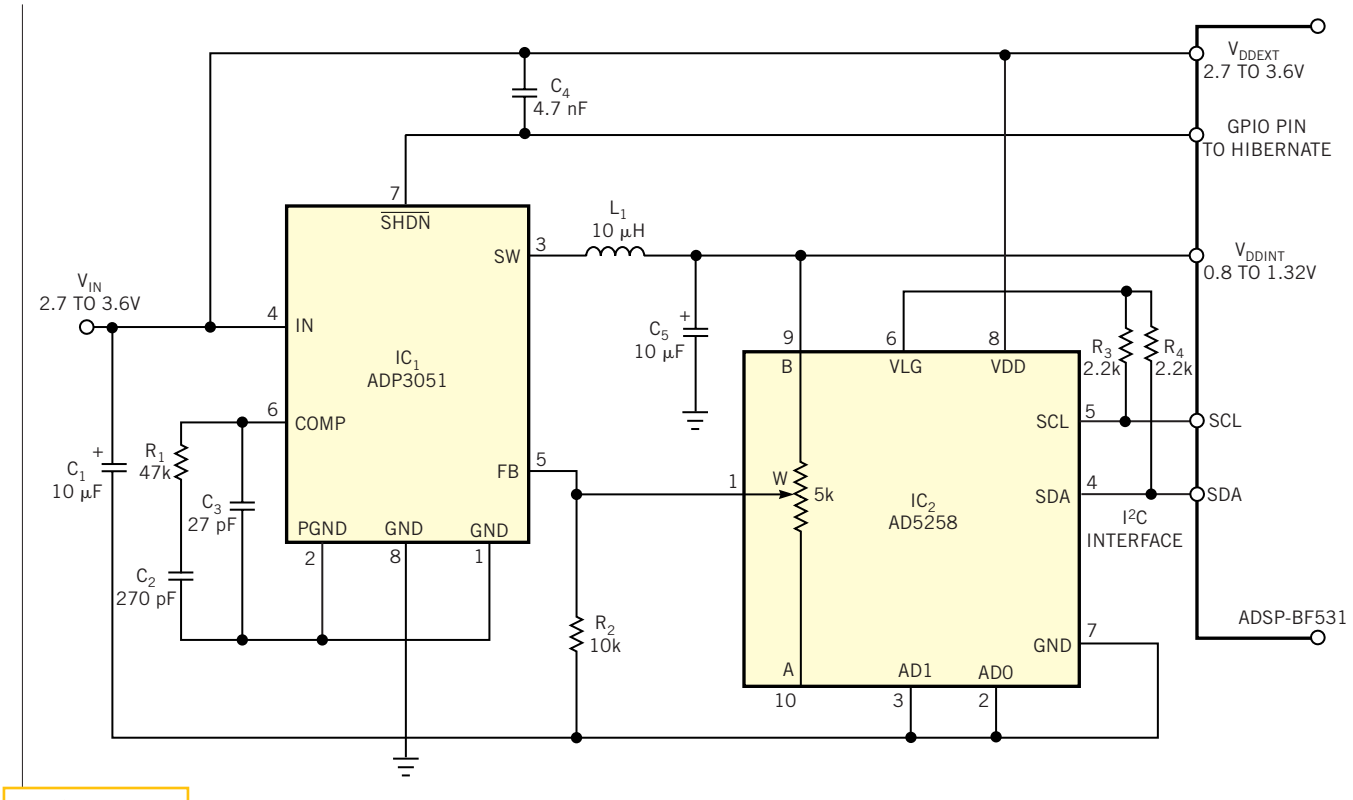

Figure 1 Under control of its host processor, digital potentiometer IC_2 adjusts the processor's core power-supply voltage.

voltage from exceeding 1.2V if a software glitch occurs.

A digital potentiometer typically presents a highly variable absolute resistance value but can accurately set its internal resistance ratio. In this design, the AD5258's internal resistor forms a voltage divider with an external resistor to set the output voltage. To improve the ADP3051's output-voltage accuracy, the ADSP-BF531 uses a simple algorithm to compute and store an appropriate maximum resistance for a given operating voltage in the AD5258's nonvolatile memory via its I^2C port.

Using the AD5258 with an external resistor provides hardware protection to prevent the output voltage from going above 1.2V. If the AD5258 is set to zero resistance, the resulting output voltage is $0.8V\times(0\Omega+10\ k\Omega)/10\ k\Omega=0.8V$. If you set it to its maximum resistance of 5 kΩ, the resulting output voltage is $0.8V\times(5\ k\Omega+10\ k\Omega)/10\ k\Omega=1.2V$. When the embedded processor directs the AD5258 via its I^2C port to ramp the core voltage from 0.8 to 1.2V, IC_1's output voltage monotonically increases within 40 µsec (**Figure 2**).□

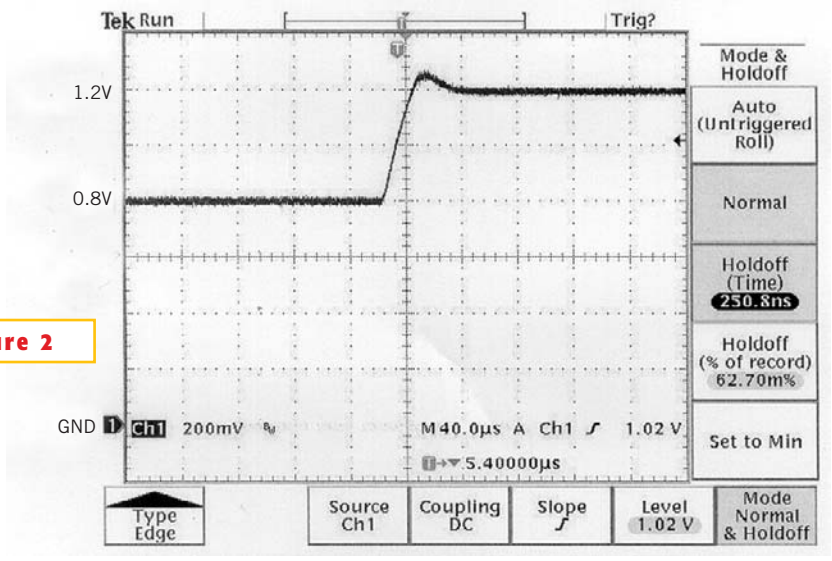

Figure 2

Applying power-supply voltage to the host processor ramps voltage from 0.8 to 1.2V with only 60-mV overshoot.

Dynamic-load circuit determines a battery's internal resistance

Jim Williams, Linear Technology Corp, Milpitas, CA

THE SIMPLEST MODEL of a battery comprises an ideal voltage source that connects in series with a resistance whose value—often a few milliohms—depends on the battery's electrochemical condition and construction. If you attempt to use an ordinary ac milliohmmeter containing a kilohertz-range ac excitation source to measure a battery's internal resistance, you get erroneous results due to capacitive effects, which introduce losses. A more realistic battery model includes a resistive divider that a capacitor partially shunts (**Figure 1**). In addition, a battery's no-load internal resistances may differ significantly from their values under a full load. Thus, for greatest accuracy, you must measure internal resistance under full load at or near dc.

The circuit in **Figure 2** meets these requirements and accurately measures internal resistance over a range of 0.001 to 1Ω at battery voltages as high as 13V. One section of an LTC6943 analog switch, IC_{2A}, alternately applies 0.110 and 0.010V derived from 2.5V voltage reference IC_3 and resistive divider R_2, R_3, and R_4 to IC_1's input.

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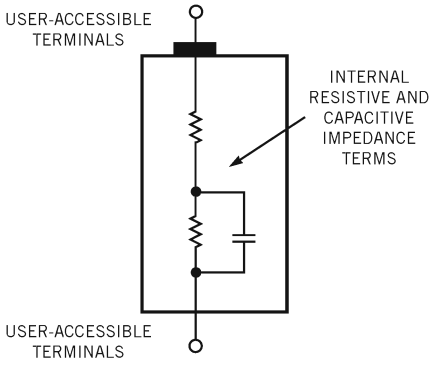

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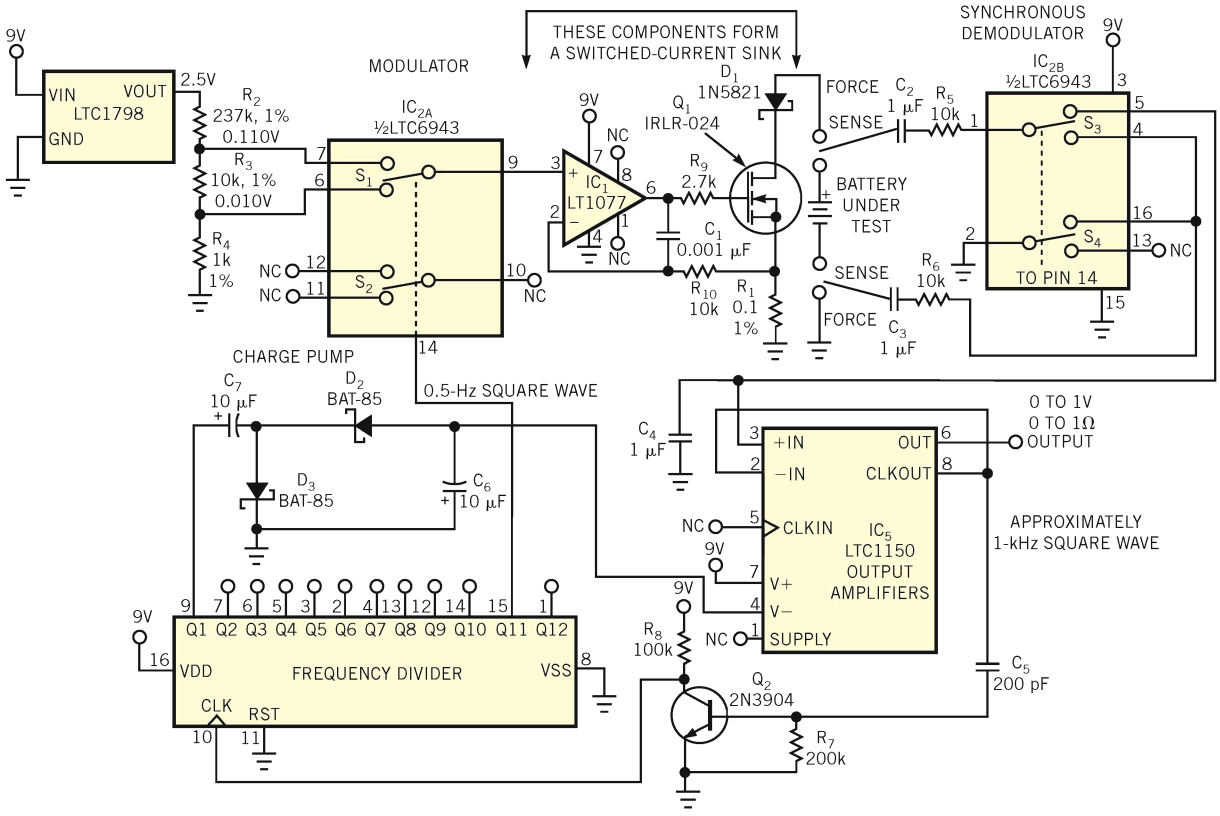

Figure 2 This circuit determines a battery's internal resistance by repetitively applying a calibrated discharge current and measuring the resultant voltage drop across the battery's terminals.

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The battery's internal resistance develops a 0.5-Hz amplitude-modulated square-wave signal at the Kelvin connections attached to the battery. A synchronous demodulator comprising analog switches S_2 and S_3 in IC_{2B} and chopper-stabilized amplifier IC_5 processes the sensed signal and delivers a 0 to 1V analog output that corresponds to a battery-resistance range of 0 to 1Ω.

Via transistor Q_2, amplifier IC_5's internal approximately 1-kHz clock drives CMOS binary divider CD4040, IC_4, which supplies a 0.5-Hz square-wave clock drive for the switches in IC_2. In addition, a 500-Hz output from IC_4 powers a charge-pump circuit that delivers approximately −7V to IC_5's negative power-supply input and thus enables IC_5's output to swing to 0V.

The complete circuit consumes approximately 230 µA, allowing nearly 3000 hours of operation from a 9V alkaline-battery power supply. The circuit operates at a supply voltage as low as 4V with less than 1-mV output variation and provides an output accuracy of 3%. The circuit accommodates a battery-under-test voltage range of 0.9 to 13V, but you can easily alter discharge current and repetition rate to observe battery resistance under a variety of conditions.□

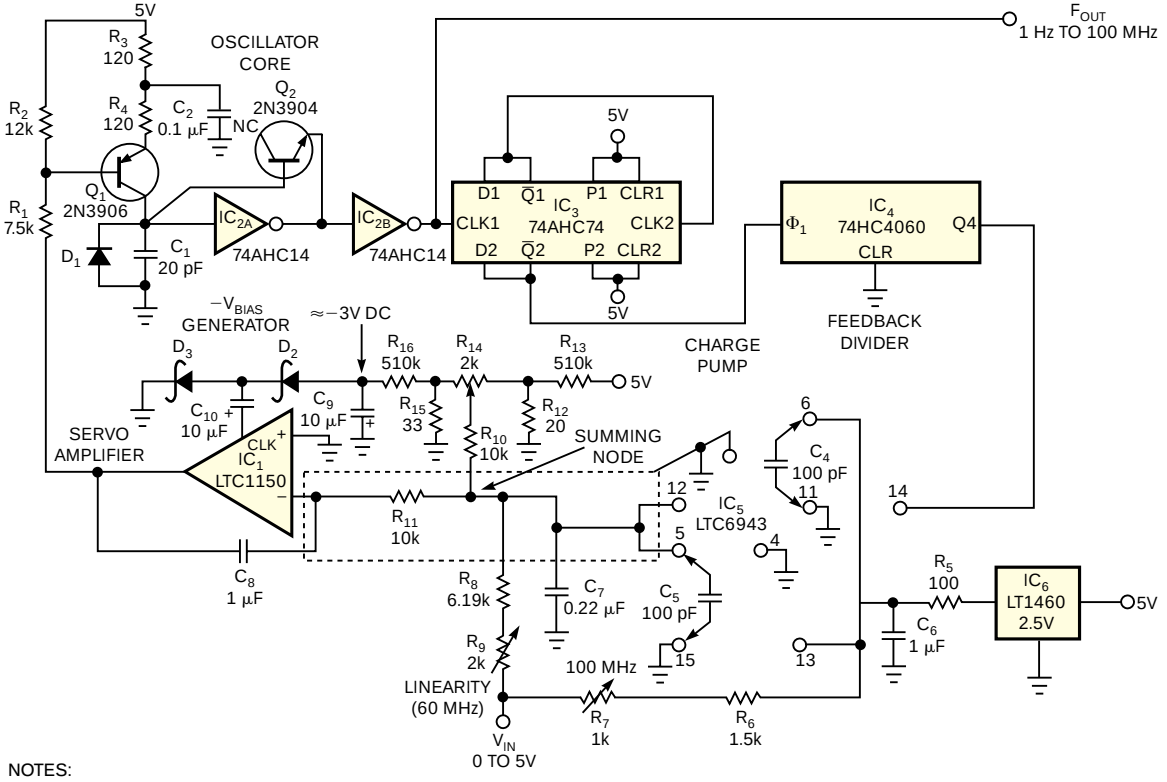
1-Hz to 100-MHz VFC features 160-dB dynamic range

Jim Williams, Linear Technology Corp

The VFC (voltage-to-frequency-converter) circuit in Figure 1 achieves a wider dynamic range and a higher full-scale output frequency—100 MHz with 10% overrange to 110 MHz—by a factor of 10 over any commercially available converter. The circuit's 160-dB dynamic range spans eight decades for a 0 to 5V input range and allows continuous operation down to 1 Hz. Additional specifications include 0.1% linearity, a 250-ppm/°C gain/temperature coefficient, a 1-Hz/°C zero-point shift, and a 0.1% frequency shift for a 10% power-supply-voltage variation. A single 5V supply powers the circuit.

Chopper-stabilized amplifier IC_1, an LTC-1150, controls a crude but wide-range oscillator core comprising bipolar transistors Q_1 and Q_2 and inverters IC_{2A} and IC_{2B}. In addition to delivering a logic-level output, the oscillator core clocks divide-by-four counter IC_3, which in turn drives IC_4, a 74HC4060 configured as a divide-by-16 counter.

After undergoing a total division by 64 in IC_3 and IC_4, the oscillator core's output drives a charge pump comprising IC_5, an LTC6943, and its associated components. The averaged difference between the charge pump's output and the applied input voltage appears at the summing node and biases IC_1, thereby closing the control loop around the wide-range oscillator core.



NOTES:
1. D_1: JPAD-500, D_2, D_3: BAT-85, R_5, R_6, R_8: TRW-IRC TYPE MAR-6, 1% METAL-FILM, C_4, C_5: WIMA TYPE FKP-2 CAPACITORS, AND C_7, C_8: WIMA TYPE MKS-2 CAPACITORS.
2. CONNECT ALL COMPONENTS AT Q_1'S COLLECTOR WITH A MINIMUM-AREA AIR-INSULATED "FLOATING" JUNCTION OVER A RELIEVED AREA OF GROUND TO MINIMIZE STRAY CAPACITANCE.
3. ENCLOSE R_{11} AND ITS CONNECTIONS TO R_9, R_{10}, IC_1'S INVERTING INPUT, C_7, AND PINS 5 AND 12 OF IC_5 WITHIN SOLDER- AND COMPONENT-SIDE GUARD TRACES TO INTERCEPT ANY BOARD-SURFACE LEAKAGE CURRENTS. (NOTE THAT THE DASHED LINE DEFINES THE GUARD TRACE.)
4. CONNECT IC_2'S UNUSED INPUTS TO GROUND. THE SCHEMATIC OMITS POWER-SUPPLY CONNECTIONS TO MOST ICS FOR CLARITY

Figure 1 Featuring a 160-dB dynamic range corresponding to a 1-Hz- to 100-MHz-frequency span, this voltage-to-frequency converter operates from a single 5V power supply.

The circuit's extraordinary dynamic range and high speed derive from the oscillator core's characteristics, the divider/charge-pump-based feedback loop, and IC_1's low dc input errors. Both IC_1 and IC_5 help stabilize the circuit's operating point by contributing to overall linearity and stability. In addition, IC_1's low offset drift ensures the circuit's 50-nV/Hz gain-versus-frequency characteristic slope and permits operation as low as 1 Hz at 25°C.

Applying a positive input voltage causes IC_1's output to go negative and alter Q_1's bias. In turn, Q_1's collector current produces a voltage ramp on C_1 (upper trace in Figure 2). The ramp's amplitude increases until Schmitt trigger inverter IC_{2A}'s output (lower trace in Figure 2) goes low, discharging C_1 through Q_2 (connected as a low-leakage diode). Discharging C_1 resets IC_{1A}'s output to its high state, and the ramp-and-reset action continues.

The leakage current of diode D_1, a Linear Systems JPAD-500, dominates all other parasitic currents in the oscillator core, but its 500-pA maximum leakage ensures operation as low as 1 Hz. The two sections of charge pump IC_5 operate out of phase and transfer charge at each clock transition. Components critical to the charge pump's stability include a 2.5V LT-1460 voltage reference, IC_6; two Wima FKP-2 polypropylene film/foils; 100-pF capacitors, C_4 and C_5; and the low charge-injection characteristics of IC_5's internal switches.

The 0.22-µF capacitor, C_7, averages the difference signal between the input-derived current and the charge pump's output and applies the smoothed dc signal to amplifier IC_1, which in turn controls the bias applied to Q_1 and thus the circuit's operating point. As noted, the circuit's closed-loop-servo action reduces the oscillator's drift and enhances its high linearity. A 1-µF Wima MKS-2 metallized-film-construction capacitor, C_8, compensates the servo loop's frequency response and ensures stability. Figure 3 illustrates the loop's well-behaved response (lower trace) to an input-voltage step (upper trace).

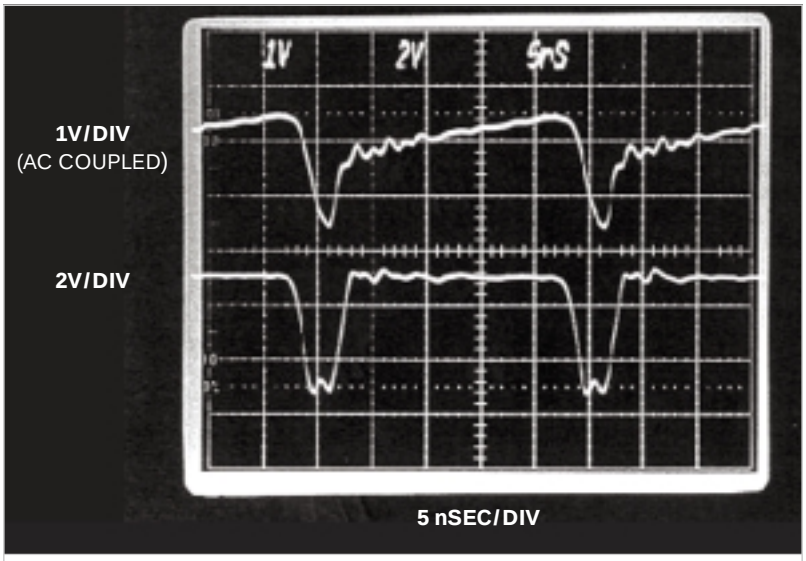


Figure 2 On a 700-MHz real-time oscilloscope, the oscillator-core waveforms at a 40-MHz operating frequency show the ramp-and-reset waveform at Q_1's collector (upper trace) and Q_2's emitter (lower trace).

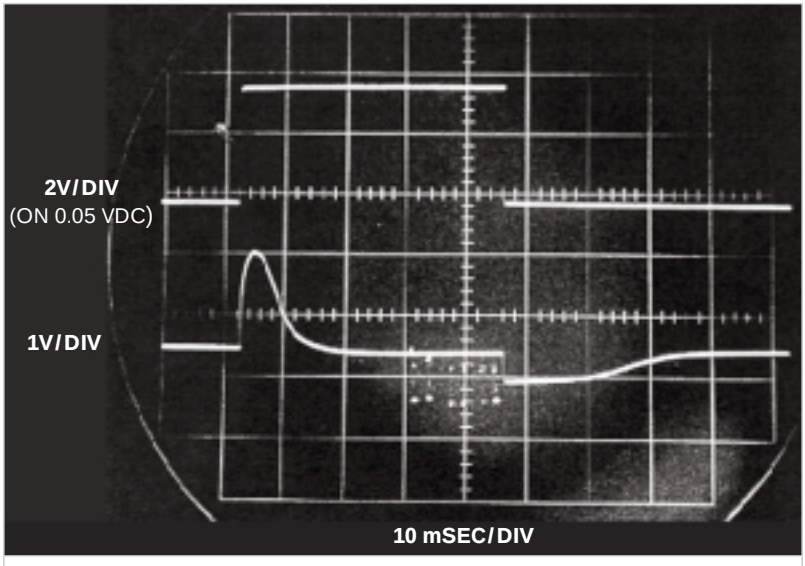


Figure 3 In response to an input-voltage step (upper trace), the voltage at the circuit's summing junction shows a 30-msec settling time.

For the circuit to achieve its design goals, certain special techniques and considerations apply. Diode D_1's leakage current dominates all other parasitic leakage currents at IC_{2A}'s input, and thus Q_1 must always supply sufficient source current to sustain oscillation and ensure operation as low as 1 Hz.

The circuit's 100-MHz full-scale upper frequency limit forces stringent restrictions on the oscillator core's cycle time, and only 10 nsec is available for a complete ramp-and-reset sequence. The reset interval imposes an ultimate speed limit on the circuit, but the upper trace in Figure 2 shows a 6-nsec reset interval that falls comfortably within the 10-nsec limit. A path from the cir-

cuit's input to the charge pump's output allows for correction of small nonlinearities due to residual charge injection. This input-derived correction is effective because the charge injection's effects vary directly with the oscillation frequency, which the input voltage determines.

Although you can use the component values given in **Figure 1** to assemble prototypes and small production quantities of the circuit, you need to consider component selection for optimum manufacturability and high-volume production. **Table 1** lists certain components' target values and estimated selection yields. The notes in **Figure 1** list the key components that the design uses.

To calibrate the circuit, apply 5V to the input and adjust the 100-MHz trimmer, R_7 for a 100-MHz output. Next, connect the input to ground and adjust trimmer R_{13} for a 1-Hz output. Allow for an extended settling interval because, at this frequency, the charge-pump update occurs once every 32 sec. Note that R_{13}'s adjustment range accommodates either a positive or a negative offset voltage because IC_1's clock output generates a negative bias voltage for R_{13}. Next, apply 3V to the input and adjust R_9 for a 60-MHz output. A certain amount of interaction occurs among the adjustments, so repeat the process until you arrive at optimum values for the three calibration frequencies. EDN

TABLE 1 SELECTION CRITERIA FOR COMPONENTS

Component	Selection parameter at 25°C	Typical yield (%)
Q_1	I_{CER}<20 pA at 3V	90
Q_2	I_{EBO}<20 pA at 3V	90
D_1	75 pA at 3V; I_{REV}<500 pA	80
IC_{2A}	I_{IN}<25 pA	80
IC_1	I_B<5 pA at V_{CC}=5V	90
IC_{2A}, IC_{2B}	Must toggle with 3.6-nsec-wide (at-50%-level) input pulse	80

Something from nothing

In the early 1980s, as Linear Technology was just beginning, we had a fundamental problem: products in development but none to sell. But, we wanted prospective customers to know our name and what we were up to. Our public-relations company glibly urged "controlling the press" and "getting our message out" but offered little real substance.

This approach seemed arrogant folly, and I felt a restless, uneasy malaise. We couldn't and shouldn't control the press; we should feed it what it wants. Editors aren't fools. They value what interests their readers. Going to them with puffery and hype would be self-defeating. The real issue was finding a way to productively use the seeming dead time before product availability. What *EDN*'s editors and their readers wanted was a series of credible, full-length technical articles in the language of relevant, working circuits.

I moped for weeks over this problem before a possible solution became apparent. Instead of waiting for products, I'd simply go into the lab, develop the applications, and then write the articles. The key to this approach was to synthesize the expected products using available ICs and discretes to build rough equivalents on small plug-in boards. We could develop functional applications and write most of the text. We'd then shelve the manuscript and breadboards. Later, when products became available, we could put them into the breadboards and implement the attendant final changes. Once we had done these tasks, we could drop scope photos and specifications into the waiting text, tweak the manuscript, and ship it off to *EDN*. This approach would speed publication by perhaps a year and synchronize the article's appearance with product introduction.

Initially, the whole scheme appeared absurd and eminently unworkable, with uncountable technical and editorial sinkholes. Getting started was much more difficult than I had imagined. Synthesizing the hardware for our unborn ICs proved tricky; my methods, clumsy and stumbling. Breadboarding the applications was laborious and slow, primarily because I wasn't sure how accurately I was mimicking the forthcoming IC's performance. Writing was equally painful. Text flow was staccato and disjointed because of the gaps that occurred while I waited for results with actual products. I had to keep separate notes directing me to unfinished text when we finally dropped the products into the breadboards.

The first article took almost two months, but things slowly became easier. Tricks to move along the lab work evolved, and I found ways to write more efficiently, making the manuscripts inherently adaptable to the planned additions and changes. Soon, I was producing an almost-finished article every two weeks or so, roaring along, powered by adrenaline, solder, pencils, paper, and pizza.

During the next year, life was a dizzy seven-day-a-week blur of breadboards and manuscripts shuttling between work and my home lab. My diet was a cardiologist's nightmare. I don't recall having a meal at home. The refrigerator was devoid of food but well-provisioned with Polaroid film to feed the oscilloscope camera. All this frenetic bustle boiled off any semblance of a normal social life. At dinner in San Francisco, while nominally listening to my date describe her job intricacies, I silently calculated the optimum chopper-channel crossover frequency in a composite amplifier. This regimen of madness continued for about a year, resulting in 35 full-length feature articles appearing in *EDN* between June 1983 and November 1987.

I still write for *EDN*, although at a significantly less frenetic pace. Now, when the kids in our lab complain to me about writing technical material, I try not to sound like the curmudgeon I am not so slowly becoming. I think that mad tear almost 25 years ago contributes to my current lack of empathy. These kids today, with a catalog full of products, they don't know what they've got.

Long-time EDN *contributor Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), has more than 20 years' experience in analog-circuit and instrumentation design. Like Jim, you can share your tale. E-mail mgwright@edn.com.*

DANIEL VASCONCELLOS

BY JIM WILLIAMS • LINEAR TECHNOLOGY CORP

Minimizing switching-regulator residue in linear-regulator outputs

BANISHING THOSE ACCURSED SPIKES TAKES ATTENTION TO DETAIL AND UNDERSTANDING THE SUBTLETIES.

Designers frequently use linear regulators to postregulate switching-regulator outputs. The benefits of this approach include improved stability, accuracy, and transient response, along with lower output impedance. Ideally, markedly reduced switching-regulator-generated ripple and spikes would accompany these performance gains. In practice, all linear regulators encounter some difficulty with ripple and spikes, particularly as frequency rises. The regulator's small input to output differential voltages magnify these effects; this situation is unfortunate, because such small differentials are desirable for maintaining efficiency.

Input-filter capacitors smooth the ripple and spikes before they reach the regulator (**Figure 1**). The output capacitor maintains low output impedance at higher frequencies, improves load transient response, and supplies frequency compensation for some regulators. Ancillary purposes include minimizing both noise and the appearance of residual-input-derived artifacts at the regulator's output. These artifacts are of concern because these high-frequency components, even though of small amplitude, can cause problems in noise-sensitive video, communication, and other types of circuitry. Designers expend large numbers of capacitors and aspirin in attempts to eliminate these undesired signals and their resultant effects. Although these signals are stubborn and sometimes seemingly immune to any treatment, understanding their origin and nature is the key to containing them.

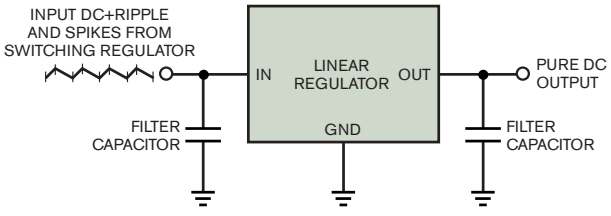


Figure 1 A conceptual linear regulator and its filter capacitors theoretically reject switching-regulator ripple and spikes.

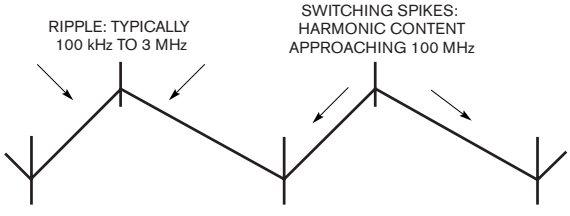


Figure 2 A switching-regulator output contains relatively low-frequency ripple and high-frequency "spikes," derived from regulators' pulsed-energy delivery and fast transition times.

SWITCHING-REGULATOR AC-OUTPUT CONTENT

Figure 2 details a switching regulator's dynamic ac-output content. It comprises relatively low-frequency ripple at the switching regulator's clock frequency—typically, 100 kHz to 3 MHz—and high-frequency content "spikes" associated with power-switch transition times. The switching regulator's pulsed

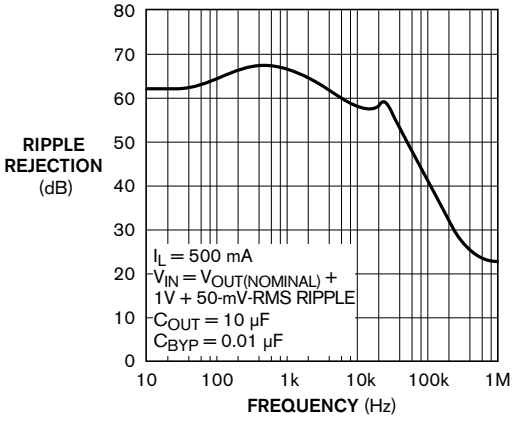


Figure 3 Ripple-rejection characteristics for an LT1763 low-dropout linear regulator show 40-dB attenuation at 100 kHz, rolling off toward 1 MHz. Switching-spike harmonic content approaches 100 MHz and passes directly from input to output.

energy delivery creates the ripple. Filter capacitors smooth—but do not eliminate—the ac content. The spikes, which often have harmonic content approaching 100 MHz, result from high-energy, rapidly switching power elements within the switching regulator. Slowing the regulator's repetition rate and transition times can greatly reduce ripple and spike amplitude, but the size of the magnetic elements increases, and their efficiency falls. Circuitry employing this approach has significantly reduced harmonic content but sacrificed the magnetics' size and efficiency (**Reference 1**). The same rapid clocking and switching that allows the use of small, highly efficient passives results in the presentation of high-frequency ripple and spikes to the linear regulator.

The regulator is better at rejecting the ripple than the wideband spikes. In a typical example, the rejection performance for an LT1763 low-dropout linear regulator, 40 dB of attenuation at 100 kHz rolls off to about 25 dB at 1 MHz (**Figure 3**). The more wideband spikes pass directly through the regulator. The output-filter capacitor, which absorbs the spikes, also has high-frequency performance limitations. The imperfect response of the regulator and filter capacitors, due to high-frequency parasitics, reveals **Figure 1** to be too simplistic. Including parasitic terms and some new components shows the regulation path with emphasis on high-frequency parasitic terms (**Figure 4**). It is important to identify these terms because they allow ripple and spikes to propagate into the nominally regulated output.

Additionally, understanding the parasitic elements permits a measurement strategy, facilitating reduction of high-frequency output content. The regulator includes high-frequency parasitic paths, primarily capacitive, across its pass transistor and into its

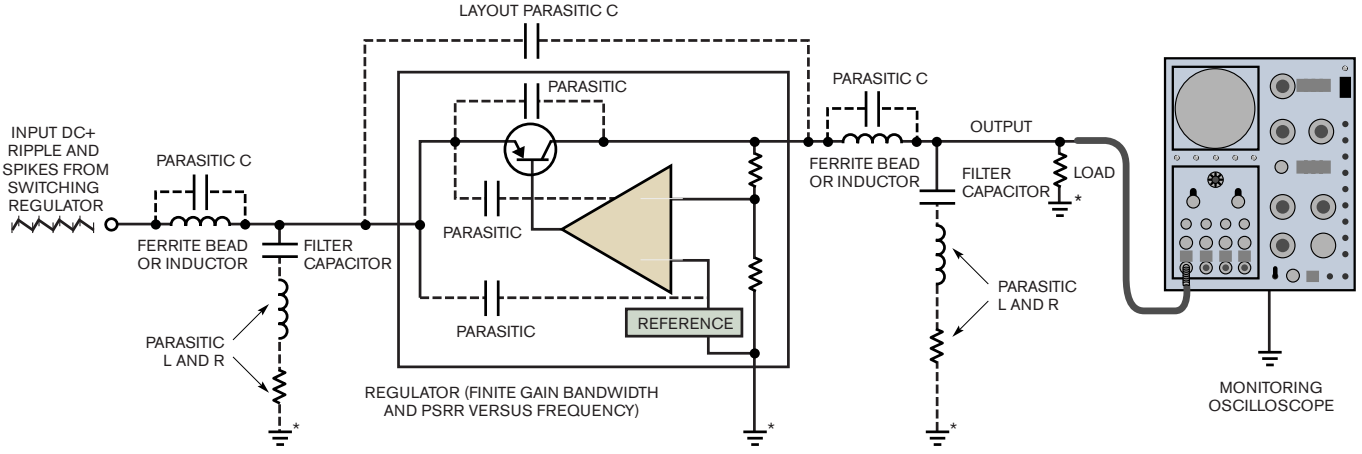


Figure 4 A conceptual linear regulator shows high-frequency-rejection parasitics. The finite-gain-bandwidth product and power-supply-rejection-ratio versus frequency limit the regulator's high-frequency rejection. Passive components attenuate ripple and spikes, but parasitics degrade effectiveness. The layout capacitance and ground-potential differences add errors and complicate measurement.

THE TRUTH ABOUT FERRITE BEADS

A ferrite bead enclosing a conductor provides the highly desirable property of increasing impedance as frequency rises. This effect suits high-frequency noise filtering of conductors carrying dc and low-frequency signals. The bead is essentially lossless within a linear regulator's passband. At higher frequencies, the bead's ferrite material interacts with the conductor's magnetic field, creating the loss characteristic. Various ferrite materials and geometries result in different loss factors versus frequency and power level (Figure A).

Impedance rises from 0.01Ω at dc to 50Ω at 100 MHz. As dc current and, hence, constant magnetic-field bias rise, the ferrite becomes less effective in offering loss. Note that you can stack beads in series along a conductor, proportionally increasing their loss contribution. A variety of bead materials and physical configurations are available to suit requirements in standard and custom products.

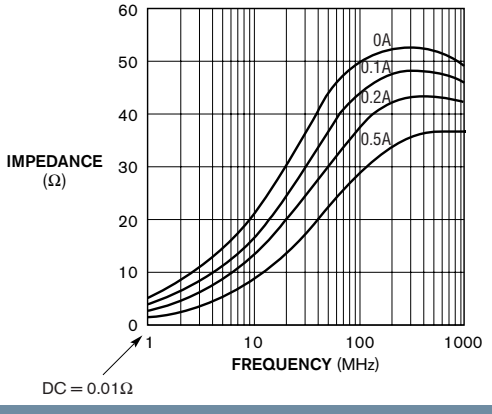


Figure A Impedance versus frequency at various dc-bias currents for a surface-mounted ferrite bead shows essentially zero impedance at dc and low frequency, rising above 50Ω depending on frequency and dc current (courtesy Fair-Rite).

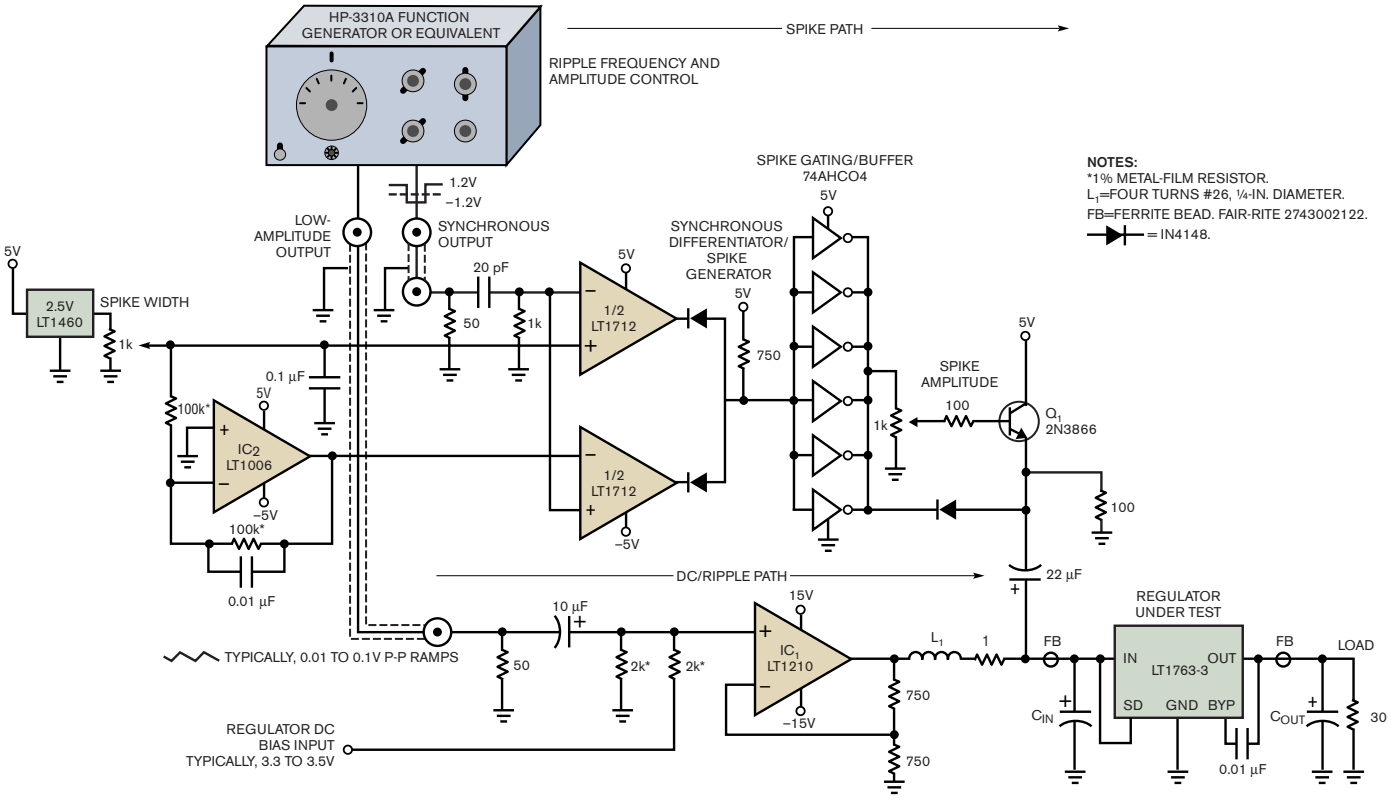


Figure 5 This circuit simulates switching-regulator output. You can independently set ripple amplitude, dc, frequency, and spike duration and height. A split-path scheme sums wideband spikes with dc and ripple, presenting the linear regulator with simulated switching-regulator output. A function generator sources waveforms to both paths.

USING INDUCTORS AS HIGH-FREQUENCY FILTERS

You can sometimes use inductors instead of beads for high-frequency filtering. Typically, values of 2 to 10 µH are appropriate. Advantages include wide availability and better effectiveness at frequencies of less than 100 kHz. Figure A shows that the disadvantages are increased dc resistance in the regulator path due to copper losses, addition of parasitic shunt capacitance, and potential susceptibility to stray switching-regulator radiation. The copper loss appears at dc, reducing efficiency, and parasitic shunt capacitance allows unwanted high-frequency feedthrough. The position and orientation of the inductors on the pc board may allow stray magnetic fields to impinge its winding, effectively turning the winding into a secondary transformer. The resulting observed spike- and ripple-related artifacts masquerade as conducted components, degrading performance.

Figure B shows a form of inductance-based filter constructed from a pc-board trace. Such extended-length traces, formed in spiral or serpentine patterns, look inductive at high frequencies. They can be surprisingly effective in some circumstances, although they introduce less loss per unit area than ferrite beads.

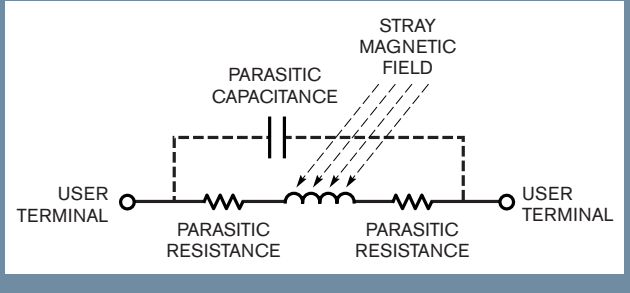


Figure A Some parasitic terms of an inductor show that parasitic resistance decreases voltage, degrading efficiency, and unwanted capacitance permits high-frequency feedthrough. The stray magnetic field induces erroneous inductor current.

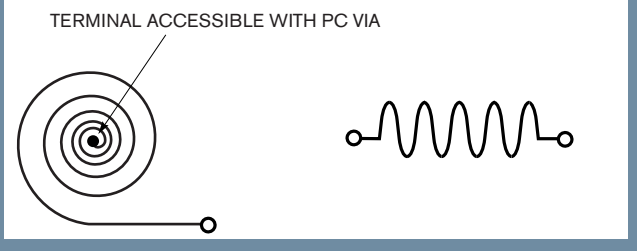


Figure B Spiral and serpentine pc-board patterns sometimes act as high-frequency filters, although they are less effective than ferrite beads.

reference and regulation amplifier. These terms combine with finite regulator gain bandwidth to limit high-frequency rejection. The input- and output-filter capacitors include parasitic inductance and resistance, degrading their effectiveness as frequency rises. Stray layout capacitance provides additional unwanted feedthrough paths. Ground-path resistance and inductance promote ground-potential differences, which add error and also complicate measurement.

Some new components, not normally associated with linear regulators, also appear. These additions include ferrite beads or inductors in the regulator input and output lines. These components have their own high-frequency parasitic paths but can considerably improve overall regulator high-frequency rejection (see **sidebar** "The truth about ferrite beads").

BUILD A RIPPLE/SPIKE SIMULATOR

Understanding the problem requires observing regulator response to ripple and spikes under a variety of conditions. You should independently vary ripple and spike parameters, including their frequency, harmonic content, amplitude, duration, and dc level. This capability is versatile, permitting real-time optimization and sensitivity analysis to various circuit variations.

PROBING TECHNIQUE FOR SUBMILLIVOLT-WIDEBAND-SIGNAL INTEGRITY

Obtaining reliable, wideband, submillivolt measurements requires attention to critical issues before measuring anything. It is essential that you design the pc-board layout for low noise. Consider current flow and interactions in power distribution, ground lines, and ground planes. Examine the effects of component choice and placement. Plan radiation management and disposition of load-return currents. The circuit must be sound, the board layout must be proper, and the circuit must use the appropriate components before you can begin meaningful measurements.

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurately extracting information. Low-level, wideband measurements demand care in routing signals to test instrumentation. Issues to consider include ground loops between pieces of test equipment, including the power supply connected to the breadboard, and noise pickup due to excessive test-lead or trace length.

Minimize the number of connections to the pc board and keep leads short. Route wideband signals to or from the breadboard in a coaxial environment with attention to where the coaxial shields tie into the ground system. A strictly maintained coaxial environment is critical for reliable measurements.

Figure A shows a believable presentation of a typical switching-regulator spike measured within a continuous coaxial signal path. The spike's main body is reasonably well-defined, and disturbances after it are contained. Figure B depicts the same event with a 3-in. ground lead connecting the coaxial shield to the pc-board ground plane. Pronounced signal distortion and ringing occur. The photographs were taken at 0.01V/division sensitivity. More sensitive measurement requires proportionately more care.

Figure C details the use of a wideband, 40-dB gain preamplifier permitting a 200-μV/division measurement in Figure 12 of the main text (pg 90). Note the purely coaxial path, including the ac-coupling capacitor, from the regulator, through the preamplifier, and to the oscilloscope. The coaxial-coupling capacitor's shield directly connects to the regulator board's ground plane with the capacitor's center conductor going to the regulator output. There are no noncoaxial-measurement connections. Figure D, repeating Figure 12, shows a cleanly detailed rendition of the 900-mV output spikes. In Figure E, 2 in. of ground lead is present at the measurement site, violating the coaxial regime. The result is corruption of the waveform presentation. As a final test to verify measurement integrity, it is useful to repeat Figure D's measurement with the signal-

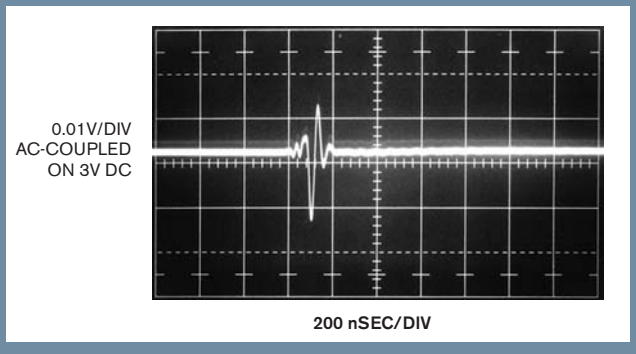


Figure A Spike measured within a continuous coaxial-signal path displays moderate disturbance and ringing after the main event.

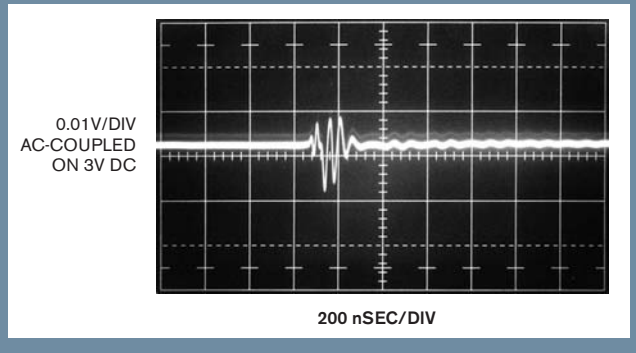


Figure B Introducing a 3-in., noncoaxial ground connection causes pronounced signal distortion and postevent ringing.

Although no substitute exists for observing linear-regulator performance under actual switching-regulator-driven conditions, a hardware simulator reduces the likelihood of surprises (**Figure 5**). It simulates a switching regulator's output with independently settable dc, ripple, and spike parameters.

The design combines a commercially available function generator with two parallel signal paths to form the circuit. It transmits dc and ripple on a relatively slow path and processes wideband spike information through a fast path. The two paths combine at the linear-regulator input. The function generator's settable ramp output (**Figure 6**, Trace A) feeds the dc/rip-

ALTHOUGH NO SUBSTITUTE EXISTS FOR OBSERVING LINEAR-REGULATOR PERFORMANCE UNDER ACTUAL SWITCHING-REGULATOR-DRIVEN CONDITIONS, A HARDWARE SIMULATOR REDUCES THE LIKELIHOOD OF SURPRISES.

path input–for example, the coaxial-coupling capacitor's center conductor–grounded near the measurement point, as in Figure 13 of the main text. Ideally, no signal should appear. Practically, some small residue, primarily due to common-mode effects, is permissible.

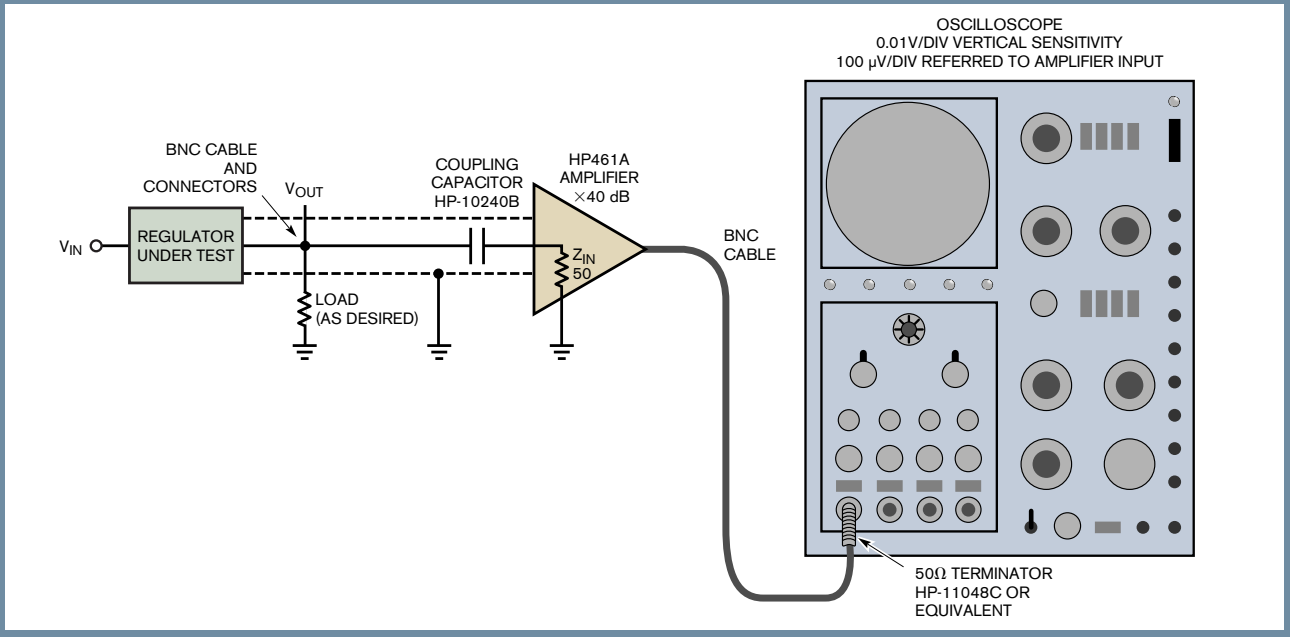


Figure C A wideband, low-noise preamplifier permits submillivolt-spike observation. The coaxial connections must remain to preserve measurement integrity.

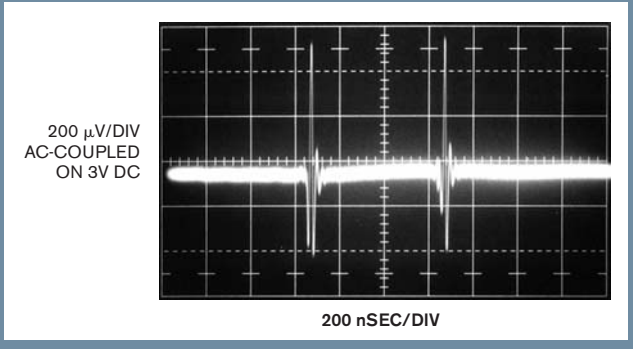


Figure D A low-noise preamplifier and strictly enforced coaxial signal path yield Figure 12's 900-mV p-p presentation. The trace's baseline thickening represents the preamplifier's noise floor.

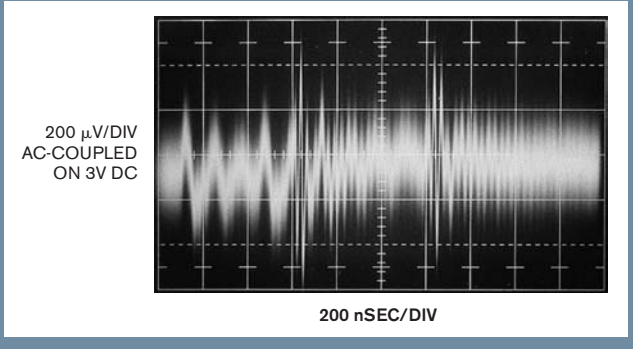
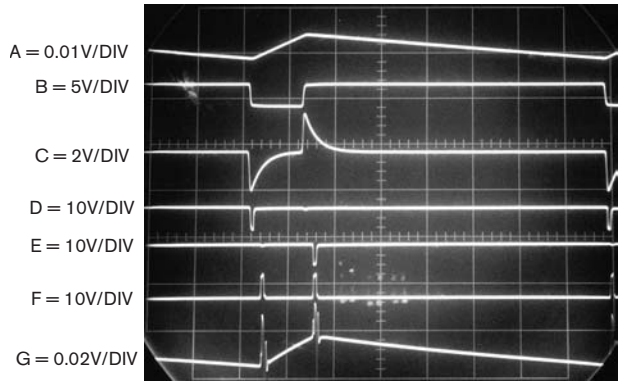


Figure E A 2-in. noncoaxial ground connection at the measurement site violates the coaxial regime, resulting in complete corruption of the waveform presentation.



NOTE: AC-COUPLED ON 3.3V DC.

Figure 6 A switching regulator outputs simulator waveforms, in which the function generator supplies ripple-path (Trace A) and spike-path (Trace B) information. C_1 and C_2 compare the differentiated spike information's bipolar excursion (Trace C), resulting in Traces D and E's synchronized spikes. Diode-gating inverters present Trace F to spike-amplitude control. G_1 sums spikes with dc-ripple path from power amplifier IC_1, forming linear-regulator input (Trace G). (Spike width is abnormally wide for photographic clarity.)

ple path, which is made up of power amplifier IC_1 and associated components. IC_1 receives the ramp input and dc-bias information and drives the regulator under test. L_1 and the 1Ω resistor allow IC_1 to drive the regulator at ripple frequencies without instability.

The function generator's pulsed synchronous output (Trace B) sources the wideband spike. Amplifier IC_2 differentiates the output's edges (Trace C) and feeds bipolar comparator IC_{3A} and

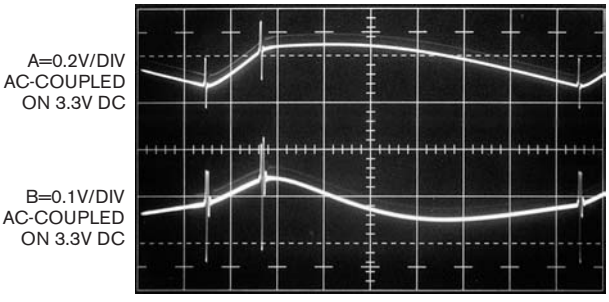


Figure 7 C_{IN} of 1 µF and C_{OUT} of 10 µF result in linear-regulator input (Trace A), output ripple (Trace B), and switching-spike content. Output spikes, driving 10 µF, have lower amplitude, but rise time remains fast.

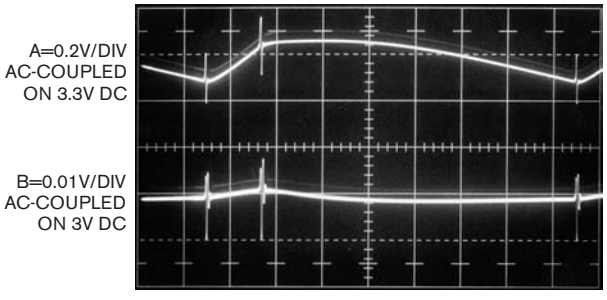


Figure 8 C_{IN} of 1 µF and C_{OUT} of 33 µF result in the same trace assignments as Figure 7. Output ripple decreases fivefold, but spikes remain. Spike rise time appears unchanged.

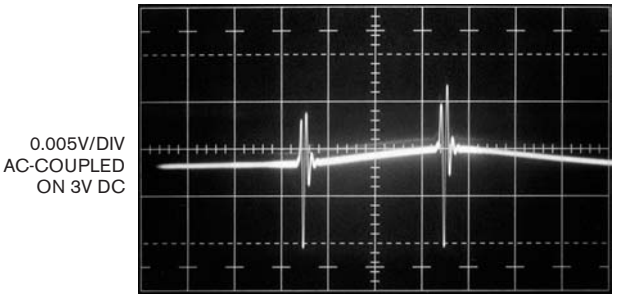


Figure 9 A time and amplitude expansion of Figure 8's output trace permits higher resolution study of spike characteristics. (The trace center-screen area is intensified for photographic clarity.)

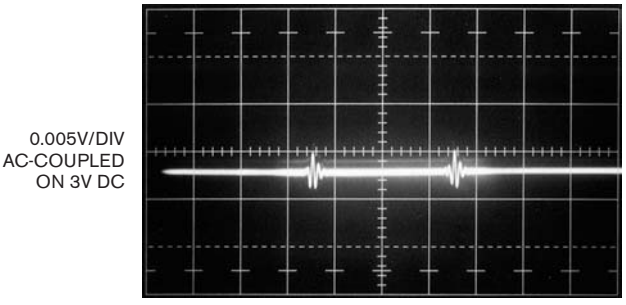


Figure 10 Adding a ferrite bead to the regulator input increases high-frequency losses, dramatically attenuating spikes. (The trace center-screen area is intensified for photographic clarity.)

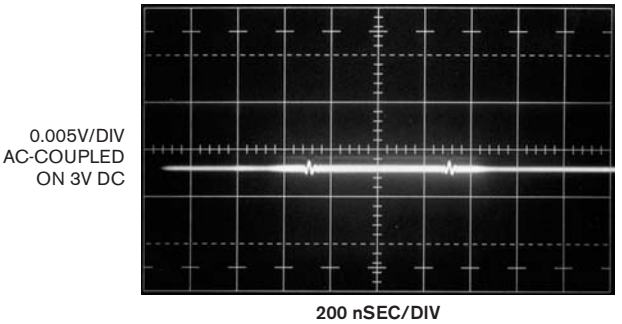


Figure 11 A ferrite bead in the regulator output further reduces spike amplitude. (The trace center-screen area is intensified for photographic clarity.)

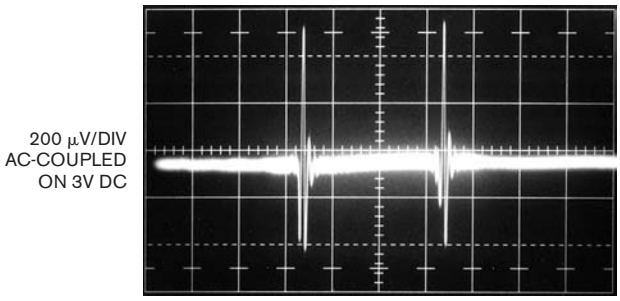


Figure 12 In this higher gain version of Figure 11, spike amplitude measures 900 μV—almost 20 times lower than without ferrite beads, whereas the instrumentation noise floor causes trace baseline thickening. (The trace center-screen area is intensified for photographic clarity.)

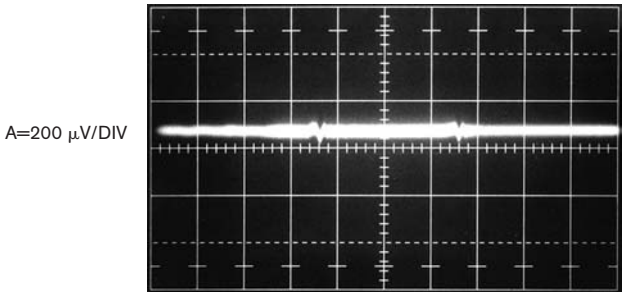


Figure 13 Grounding the oscilloscope input near the measurement point verifies that Figure 12's results are nearly free of common-mode corruption. (The trace center-screen area is intensified for photographic clarity.)

IC_{3B}. The comparator-output spikes (traces D and E) are synchronized to the ramp's inflection points. Complementary dc-threshold potentials applied to IC_{3A} and IC_{3B} with the 1-kΩ potentiometer and IC_2 control the spike width. Diode gating and the paralleled logic inverters present Trace F to the spike-amplitude control. Follower Q_1 sums the spikes with IC_1's dc/ripple path, forming the linear regulator's input (Trace G).

LINEAR-REGULATOR REJECTION EVALUATION

The circuit in **Figure 5** facilitates evaluation of linear-regulator high-frequency rejection. The waveform in **Figure 7** shows **Figure 5**'s LT1763 3V regulator response to a 3.3V-dc input with Trace A's ripple/spike contents, C_{IN}=1 μF, and C_{OUT}=10 μF. Regulator output (Trace B) shows ripple attenuated by a factor of approximately 20. Output spikes see somewhat less reduction, and their harmonic content remains high. The regulator offers no rejection at the spike's rise time. The capacitors must do the job. Unfortunately, inherent high-frequency loss terms prevent the capacitors from filtering the wideband spikes; Trace B's remaining spike shows no rise-time reduction. Increasing the capacitor value has no benefit at these rise times. **Figure 8**, with the same trace assignments as **Figure 7** but with a value of 33 μF for C_{OUT}, shows a fivefold ripple reduction but little spike-amplitude attenuation.

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Figure 9's time and amplitude expansion of **Figure 8**'s Trace B permits high-resolution study of spike characteristics, allowing the following evaluation and optimization. **Figure 10** shows dramatic results when a ferrite bead immediately precedes C_{IN}. Spike amplitude drops about fivefold. The bead presents loss at high frequency, severely limiting spike passage. The dc and low-frequency components pass unattenuated to the regulator. Placing a second ferrite bead at the regulator output before C_{OUT} produces **Figure 11**'s trace. The bead's high-frequency loss characteristic further reduces spike amplitude below 1 mV without introducing dc resistance into the regulator's output path. You can sometimes use inductors in place of beads, but make sure that you understand inductors' limitations (see **sidebar** "Using inductors as high-frequency filters").

Figure 12, which shows a higher gain version of **Figure 11**, measures 900-μV spike amplitude—almost 20 times lower than without the ferrite beads. Complete the measurement by verifying that common-mode components or ground loops do not corrupt the indicated results. You achieve this goal by grounding the oscilloscope input near the measurement point. Ideally, no signal should appear. **Figure 13** shows almost no signal, indicating that **Figure 12**'s display is realistic. Faithful wideband measurement at submillivolt levels requires special considerations (see **sidebar** "Probing technique for submillivolt-wideband-signal integrity"). The articles, application notes, and books in **references 2** through **9** are also helpful to serious designers. EDN

AUTHOR'S BIOGRAPHY

Long-time EDN *contributor Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), has more than 20 years' experience in analog-circuit and instrumentation design.*

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Load-transient-response testing for voltage regulators

VARIATIONS OCCUR IN VOLTAGE REGULATORS' TRANSIENT LOADS; THUS, THE DEVICES REQUIRE CAREFUL EVALUATION AND TESTING.

Semiconductor memory, card readers, microprocessors, disk drives, piezoelectric devices, and digital systems create transient loads that voltage regulators must service. Ideally, regulator output would be invariant during a load transient. In practice, however, some variation occurs, and this variation becomes problematic if a system exceeds its allowable operating-voltage tolerances. This problem mandates testing the regulator and its associated support components to verify desired performance under transient-loading conditions. You can use various methods to generate transient loads and allow observation of regulator response.

Figure 1 shows a conceptual load-transient generator. The regulator under test drives dc and switched resistive loads, which may be manually variable. The device monitors its switched current and output voltage, permitting comparison of the output voltage and the load current under static and dynamic conditions. The switched current is either on or off; there is no electronically controllable linear region.

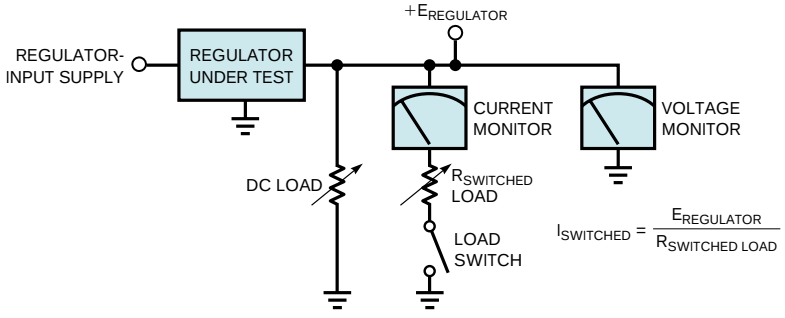

Figure 1 This conceptual regulator-load tester includes switched and dc loads and voltage and current monitors. The resistor values set dc and switched-load currents. The switched current is either on or off; there is no controllable linear region.

Figure 2 shows a practical implementation of the load-transient generator. Capacitors augment the voltage regulator under test; these capacitors provide an energy reservoir, similar to a mechanical flywheel, to aid transient response. The size, dielectric, and location of these capacitors, particularly C_{OUT}, have a pronounced effect on transient response and overall regulator stability (references 1 and 2). The input pulse triggers the LTC1693 FET driver to switch Q_1, generating a transient-load current from the regulator. An oscilloscope monitors the instantaneous load voltage and, through a "clip-on" wideband-probe, current (see sidebar "Probing considerations for load-transient-response measurements"). Figure 3 provides an evaluation of the circuit's load-transient-generating capabilities by substituting a low-impedance power source for the regulator. The combination of a high-capacity power supply, low-impedance connections, and generous bypassing maintains low impedance across frequency. Figure 4 shows the circuit in Figure 3's response to the LTC1693-1 FET driver (Trace A) by cleanly switching 1A in 15 nsec (Trace B). Such speed is useful for simulating many loads but has restricted versatility. Although fast, the circuit cannot emulate loads between the minimum and the maximum currents.

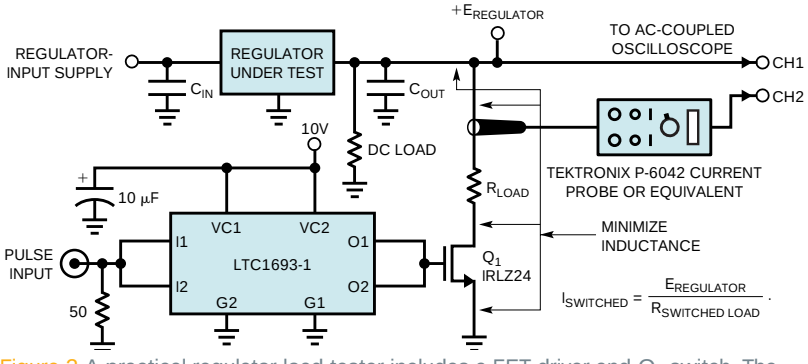

Figure 2 A practical regulator-load tester includes a FET driver and Q_1 switch. The oscilloscope monitors the current-probe output and regulator response.

CLOSED-LOOP TESTERS

Figure 5's conceptual closed-loop load-transient generator linearly controls Q_1's gate voltage to set instantaneous transient current at any desired point, allowing simulation of nearly any load profile. Feedback from Q_1's source to the A_1 control amplifier closes a loop around Q_1, stabilizing its operating point. Q_1's current assumes a value that depends on the control-input voltage and the current-sense resistor over a wide bandwidth. Once A_1 biases to Q_1's

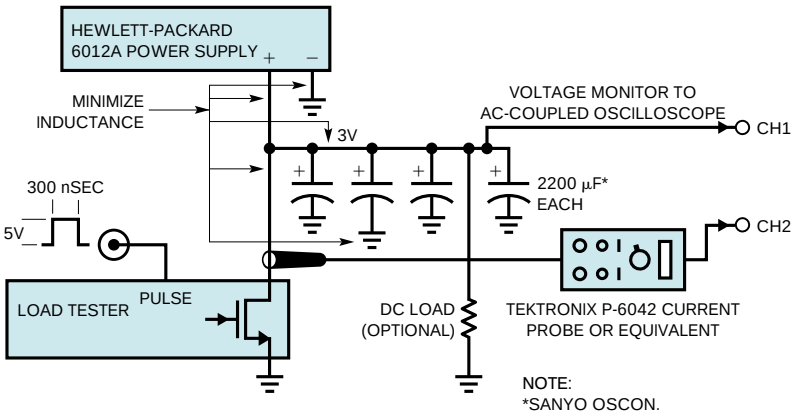

Figure 3 Substituting a well-bypassed, low-impedance power supply for the regulator lets you determine the load tester's response time.

conductance threshold, small variations in A_1's output result in large current changes in Q_1's channel. As such, A_1 need not output large excursions; its small signal bandwidth, rather than its slew rate, is the fundamental speed limitation. Within this restriction, Q_1's current waveform is the same shape as A_1's control-input voltage, allowing linear control of load current. This versatile capability permits a variety of simulated loads.

FET-BASED CIRCUIT

Figure 6 shows a practical incarnation of a FET-based closed-loop load-transient generator, including dc-bias and waveform inputs. A_1 must drive Q_1's high-capacitance gate at high frequency, necessitating high peak A_1 output currents and attention to feedback-loop compensation. A_1, a 60-MHz current-feedback amplifier, has an output-current capacity exceeding 1A. Maintaining stability and waveform fidelity at high frequency while driving Q_1's gate capacitance necessitates settable gate-drive-peaking components, a damper network, feedback trimming, and loop-peaking adjustments. You make the required dc trim first. Without applying an input, trim the 1-mV adjust for 1 mV dc at Q_1's source. You make the ac trims using Figure 7's arrangement. Similar to the circuit in Figure 3, this "brick-wall"-regulated source provides minimal ripple and sag when the load-transient generator step-loads it. Apply the inputs as the figure shows and trim the gate drive, feedback, and loop-peaking adjustments for the cleanest square-cornered response on the oscilloscope's current-probe-equipped channel.

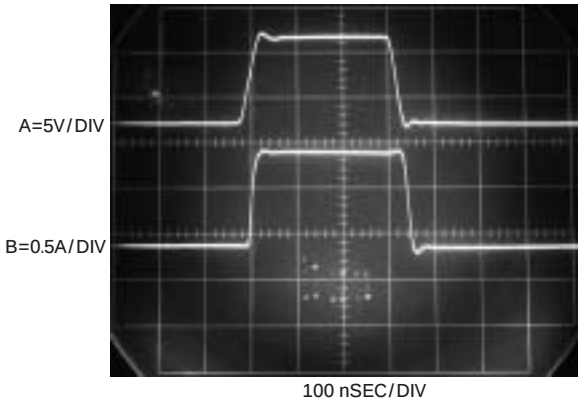

Figure 4 Figure 2's circuit responds to the FET driver's output (Trace A), switching a 1A load (Trace B) in 15 nsec.

BIPOLAR TRANSISTORS

The circuit in Figure 8 considerably simplifies the previous circuit's loop dynamics and eliminates all ac trims. The major trade-off is a halving of speed. The circuit is similar to the one in Figure 6, except that Q_1 is a bipolar transistor. The bipolar's greatly reduced input capacitance allows A_1 to drive a more benign load. This approach permits you to use an amplifier with lower output current and eliminates the dynamic trims necessary to accommodate Figure 6's FET-gate capacitance. The sole trim is the 1-mV adjustment, which you accomplish as described. You can eliminate this trim at the cost of circuit complexity (see sidebar "A trimless, closed-loop-transient-load tester"). Aside from the twofold speed decrease, the bipolar transistor also introduces a 1% output-current error due to its base current. You add Q_2 to prevent excessive Q_1 base current when the regulator supply is absent. The diode prevents reverse-base bias under any circumstances.

CLOSED-LOOP-CIRCUIT PERFORMANCE

Figures 9 and 10 show the two wideband circuits' operation. The FET-based circuit (Figure 9) requires only a 50-mV A_1 swing (Trace A) to enforce Trace B's flat-topped current pulse with 50-nsec edges through Q_1. Figure 10 details the bipolar-transistor-based circuit's performance. Trace A, taken at Q_1's

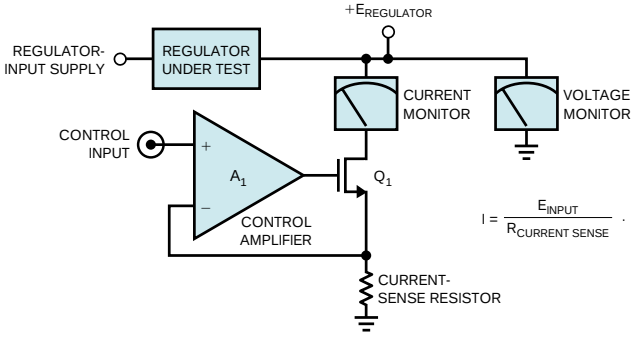

Figure 5 In this conceptual closed-loop-load tester, A_1 controls Q_1's source voltage, setting the regulator's output current. Q_1's drain-current waveshape is identical to A_1's input, allowing linear control of the load current. The voltage and current monitors match those in Figure 1.

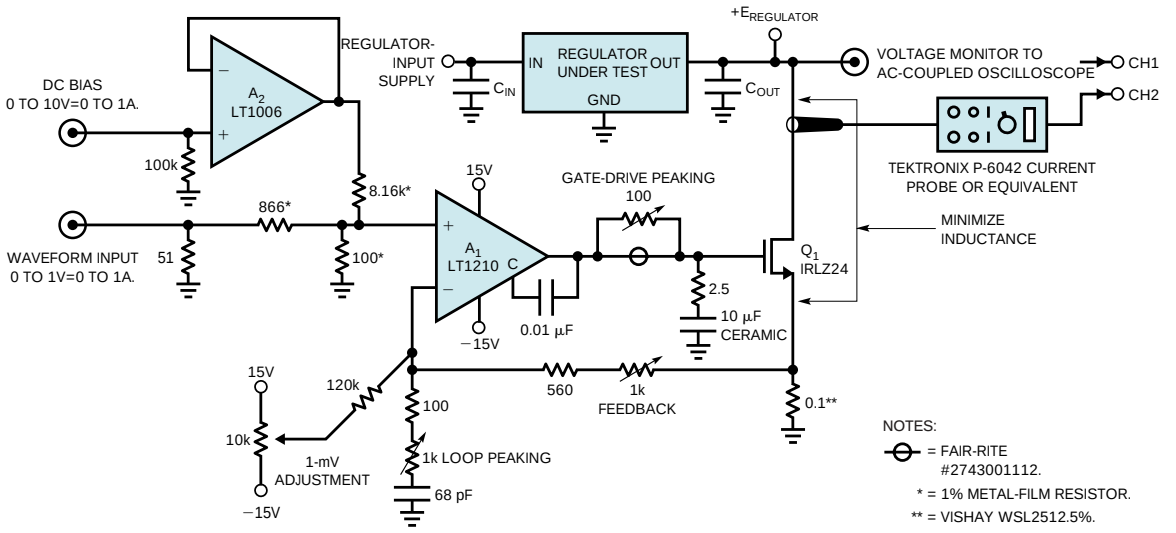

Figure 6 In a detailed closed-loop-load tester, the dc-level and pulse inputs feed A_1 to the Q_1 current-sinking-regulator load. Q_1's gain allows a small A_1 output swing, permitting wide bandwidth. The damper network, feedback, and peaking trims optimize edge response.

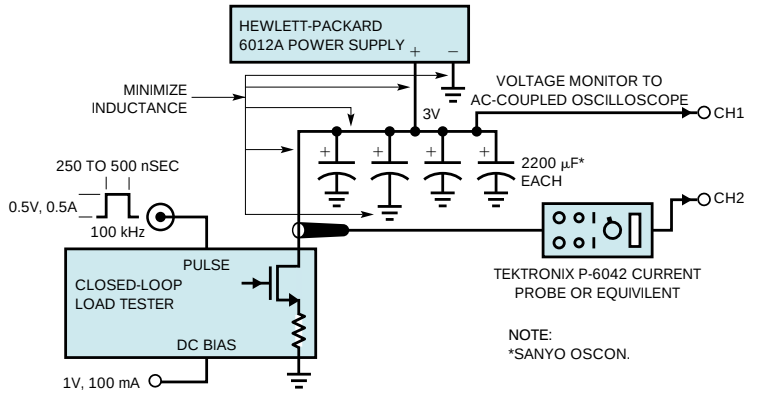

Figure 7 Determining the closed-loop-load-tester response time occurs as in Figure 3. A "brick-wall" input provides a low-impedance source.

base, rises less than 100 mV, causing Trace B's clean, 1A current conduction through Q_1. This circuit's 100-nsec edges, about two times slower than the more complex FET-based version, are still fast enough for most practical transient-load testing.

LOAD-TRANSIENT TESTING

These circuits permit rapid and thorough voltage-regulator load-transient testing. Figure 11 uses Figure 6's circuit to evaluate an LT1963A linear regulator. Figure 12 shows regulator response (Trace B) to Trace A's asymmetrically edged input pulse. The ramped leading edge, within the LT1963A's bandwidth, results in Trace B's smooth 10-mV p-p excursion. The fast trailing edge, well outside the LT1963A's passband,

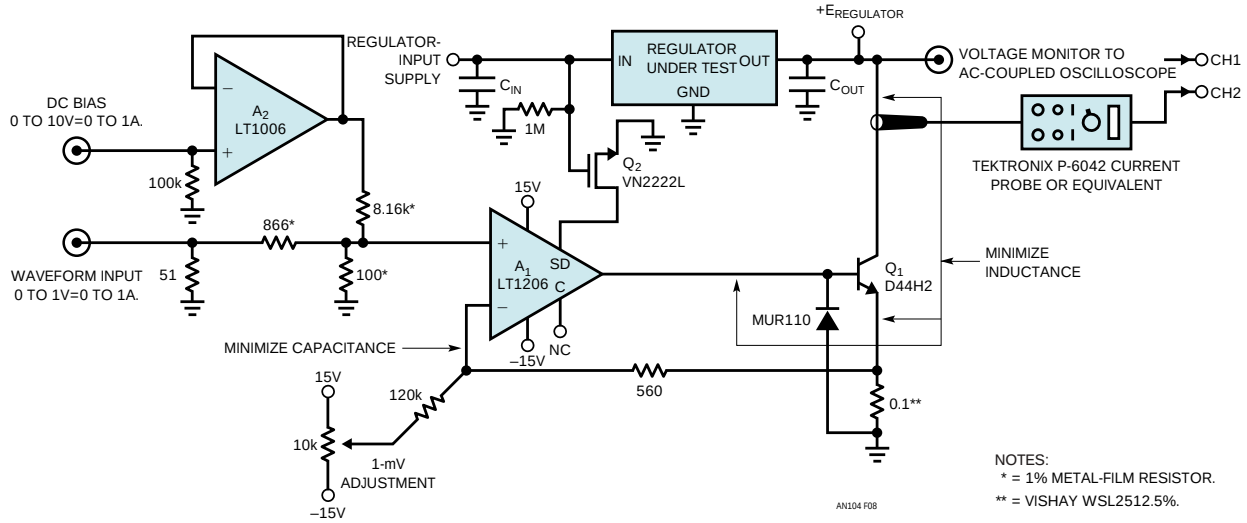

Figure 8 This circuit matches that of Figure 6 but with a bipolar transistor. Q_1's reduced input capacitance simplifies loop dynamics, eliminating compensation components and trims. The trade-off is a halving of speed and a base-current-induced 1% error.

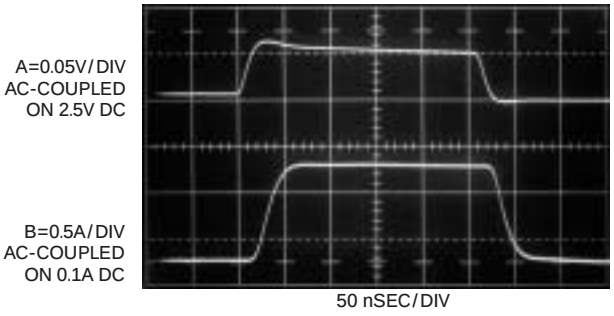

Figure 9 Figure 6's closed-loop-load-tester step response is quick and clean, showing 50-nsec edges and a flat top. (Q_1's current is Trace B.) A_1's output (Trace A) swings only 50 mV, allowing wideband operation. Trace B's presentation is slightly delayed due to voltage and current-probe time skew.

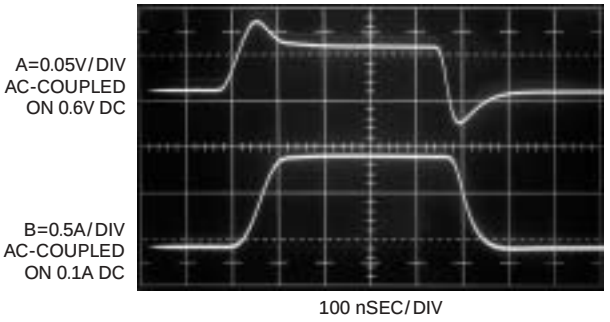

Figure 10 Figure 8's bipolar-output-load-tester response is two times slower than the FET version, but the circuit is simpler and eliminates compensation trims. Trace A is A_1's output, and Trace B is Q_1's collector current.

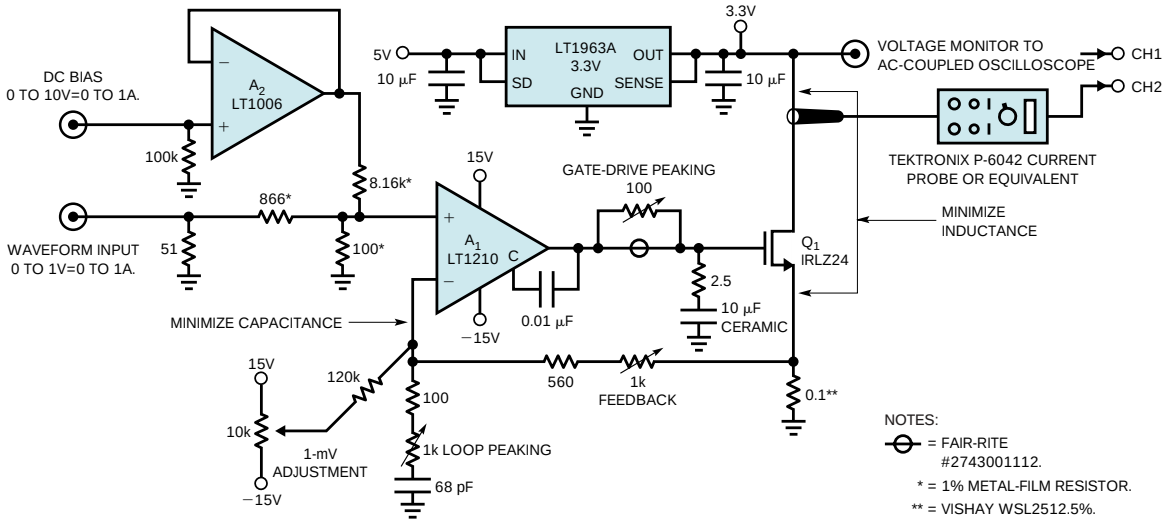

Figure 11 This closed-loop-load tester with an LT1963A regulator provides load testing for a variety of current and load waveshapes.

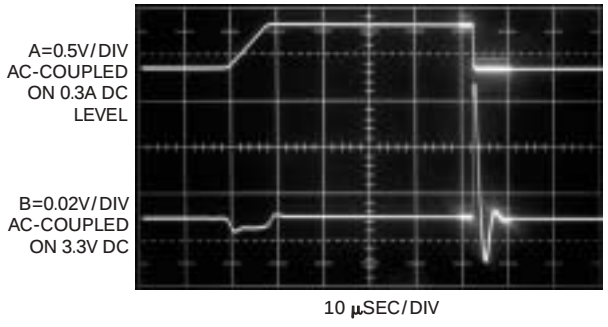

Figure 12 The circuit in Figure 11 responds (Trace B) to an asymmetrically edged pulse input (Trace A). A ramped leading edge within the LT1963A's bandwidth results in Trace B's smooth, 10-mV-p-p excursion. A fast trailing edge outside the LT1963A's bandwidth causes Trace B's abrupt 75-mV-p-p disruption. The photo intensifies the trace's latter portion for clarity.

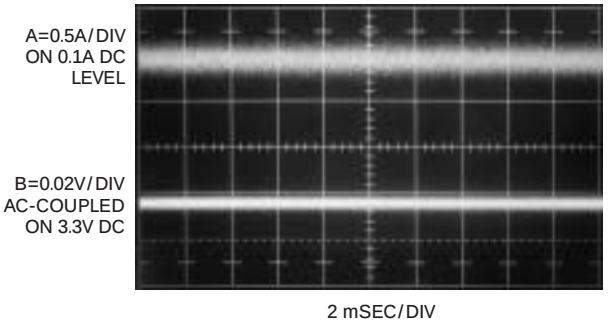

Figure 13 A 500-mA-p-p, 500-kHz noise load (Trace A) within the regulator's bandpass produces only 6-mV artifacts at Trace B's regulator output.

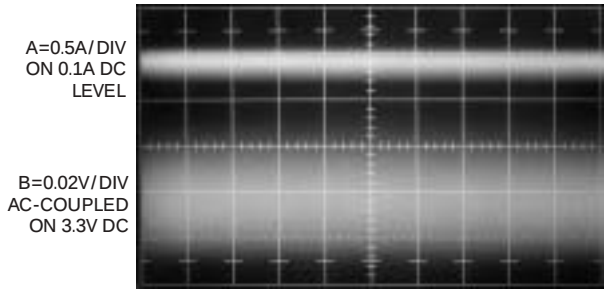

Figure 14 This waveform has the same conditions as Figure 13, except with increased noise bandwidth of 5 MHz, exceeding the regulator's bandwidth and resulting in 50-mV-p-p output error.

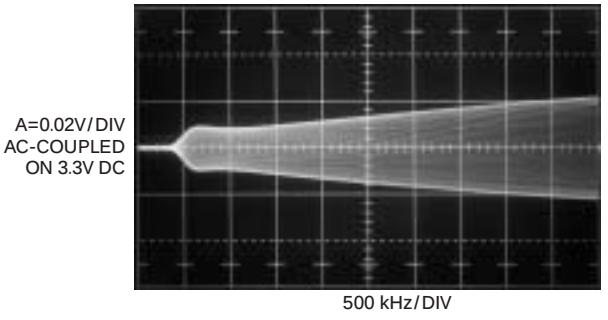

Figure 15 A swept, dc to 5-MHz, 0.35A load on 0.2A dc causes the regulator's output impedance to rise with frequency and correspondingly increases output error.

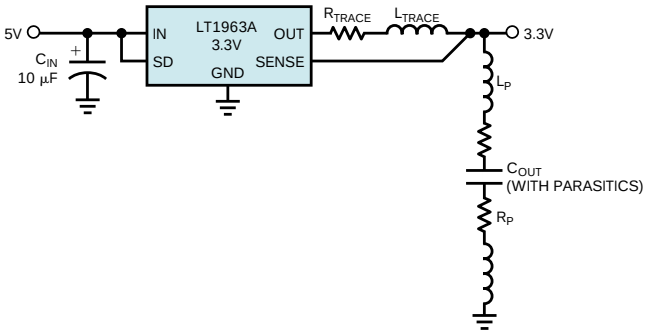

Figure 16 C_{OUT} dominates the regulator's dynamic response; C_{IN} is much less critical. Parasitic inductance and resistance limit the capacitor's effectiveness at frequency. The capacitor's value and dielectric significantly influence the load-step response. Excessive trace impedance is also a factor.

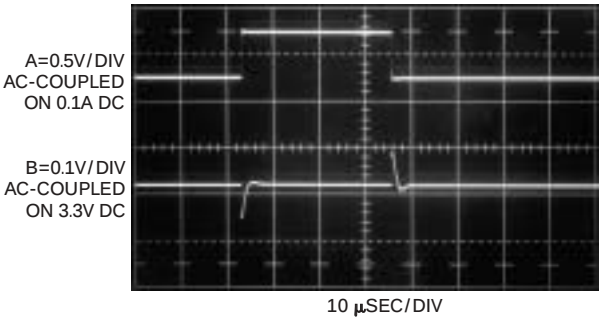

Figure 17 A stepped 0.5A load to Figure 16's circuit (Trace A) with $C_{IN}=C_{OUT}=10$ µF results in Trace B's regulator output. The use of low-loss capacitors promotes controlled output excursions.

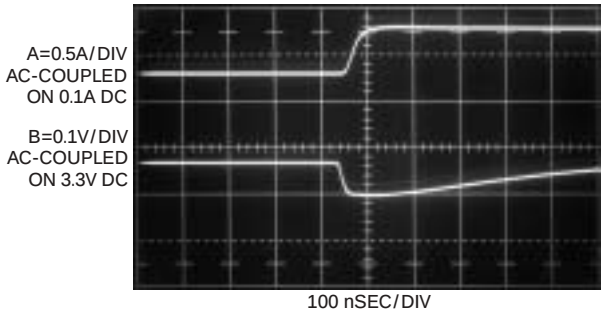

Figure 18 The expanding horizontal scale shows Trace B's smooth regulator-output response. Mismatched current- and voltage-probe delays account for slight time skewing.

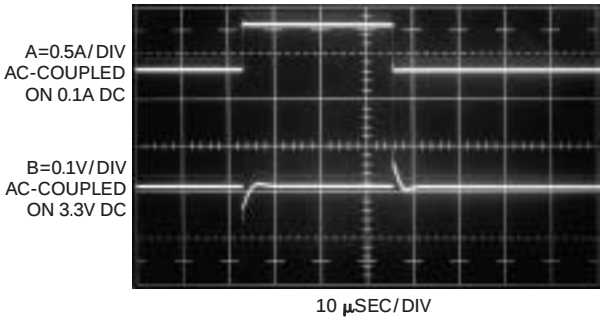

Figure 19 An "equivalent" 10-µF C_{OUT} capacitor to the one in Figure 17 shows performance that appears similar at 10 µsec/division.

causes Trace B's abrupt disruption. C_{OUT} supplies too little current to maintain output level, and a 75-mV-p-p spike results before the regulator resumes control. In Figure 13, a 500-mA p-p, 500-kHz noise load, emulating a multitude of incoherent loads, feeds the regulator in Trace A. This frequency is within the regulator's bandwidth, and only 6 mV p-p of disturbance appears in Trace B, the regulator output. Figure 14 maintains the same conditions, except that noise bandwidth increases to 5 MHz. This increase exceeds regulation bandwidth, resulting in more than 50-mV p-p error, an eightfold increase.

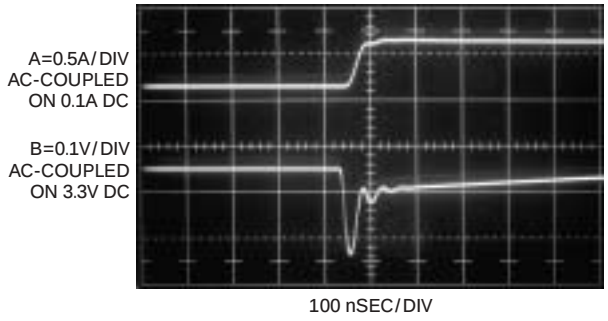

Figure 20 The horizontal-scale expansion reveals that the "equivalent" capacitor produces two times more amplitude error than the one in Figure 18. Mismatched probe delays cause time skewing between traces.

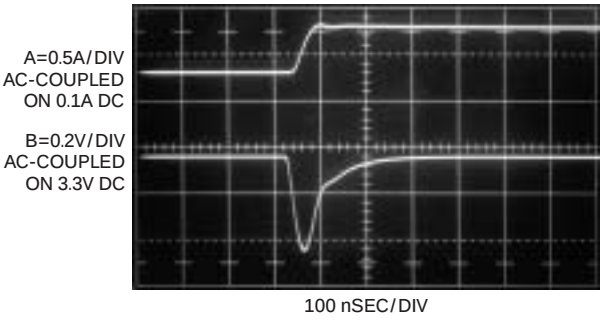

Figure 21 An excessively lossy 10-μF C_{OUT} allows a 400-mV excursion—four times Figure 18's amount. The time skewing between the traces derives from probe mismatch.

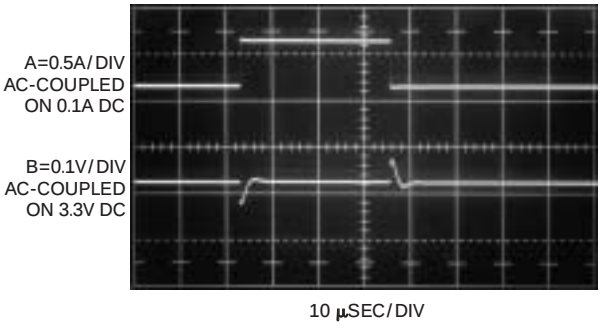

Figure 22 Replacing C_{OUT} with a low-loss, 33-μF unit yields a 40% smaller output-response transient than that of Figure 17.

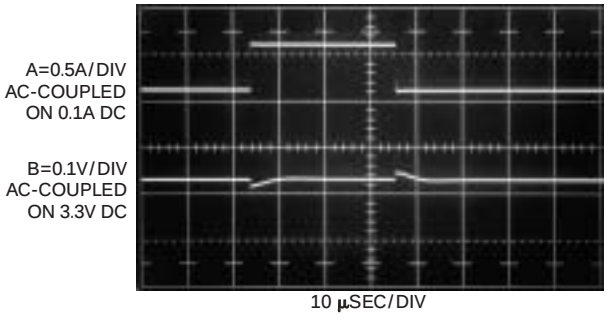

Figure 23 A low-loss, 330-μF capacitor keeps output-response transients to less than 20 mV—four times lower than Figure 17's 10-μF capacitor.

Figure 15 shows what happens when you present a 0.2A, dc-biased, swept, dc to 5-MHz, 0.35A load to the regulator. The regulator's rising output impedance versus frequency results in ascending error as frequency scales. This information allows determination of regulator output impedance versus frequency.

CAPACITOR'S ROLE IN REGULATOR RESPONSE

The regulator employs capacitors at its input (C_{IN}) and output (C_{OUT}) to augment its high-frequency response. You should carefully consider the capacitor's dielectric, value, and location because they greatly influence regulator characteristics (references 1, 2, and 3). C_{OUT} dominates the regulator's dynamic response; C_{IN} is much less critical, as long as it does not discharge below the regulator's dropout point. Figure 16 shows a typical regulator circuit and emphasizes C_{OUT} and its parasitics. Parasitic inductance and resistance limit capacitor effectiveness at frequency. The capacitor's dielectric and value significantly influence load-step response. A "hidden" parasitic, impedance buildup in regulator-output-trace runs, also influences regulation characteristics, although you can minimize the parasitic's effects by remote sensing and distributed capacitive bypassing.

Figure 17 shows Figure 16's circuit responding (Trace B) to a 0.5A load step biased on 0.1A dc (Trace A) with $C_{IN}=C_{OUT}=10$ μF. The circuit employs low-loss capacitors, resulting in Trace B's well-controlled output. Figure 18 greatly expands the horizontal time scale to investigate high-frequency behavior. Regulator-output deviation (Trace B) is smooth with no abrupt discontinuities. Figure 19 runs the same test as Figure 17 using an output capacitor claimed as "equivalent" to the one that Figure 17 employs. At 10 μsec/division, the scope photos seem similar, but Figure 20 indicates problems. This photo, taken at the same higher sweep speed as the one in Figure 18, reveals the "equivalent" capacitor to have twice as much amplitude error, higher frequency content, and higher resonances than the one in Figure 18. (Always specify components according to observed performance, rather than salesmen's claims.) Figure 21 substitutes a lossy 10-μF unit for C_{OUT}. This capacitor allows a 400-mV excursion (note Trace B's vertical-scale change), greater than four times Figure 18's amount. Conversely, Figure 22 increases C_{OUT} to a low-loss, 33-μF type, decreasing Trace B's output-response transient by 40% versus Figure 18. Figure 23's further increase, to a low-loss, 330-μF capacitor, keeps transients inside 20 mV: four times lower than Figure 18's 10-μF value.

The lesson is clear: Capacitor value and dielectric quality have a pronounced effect on transient-load response. Try before specifying!

RISE TIME VERSUS REGULATOR RESPONSE

The closed-loop-load-transient generator also allows investigating load-transient rise time on regulation at high speed. Figure 24 shows Figure 16's circuit ($C_{IN}=C_{OUT}=10$ μF), respond-

PROBING CONSIDERATIONS FOR LOAD-TRANSIENT-RESPONSE MEASUREMENTS

Signals of interest in load-transient-response studies occur within a bandwidth of approximately 25 MHz and a rise time of 14 nsec. This modest speed range eases probing techniques, but high-fidelity measurement requires some care. You measure load current with a dc-stabilized, Hall-effect, clip-on current probe such as the Tektronix (www.tektronix.com) P-6042 or A6302/AM503. The conductor loop in the probe jaws should encompass the smallest possible area to minimize introduced parasitic inductance, which can degrade measurement. At higher speeds, grounding the probe case may slightly decrease measurement aberrations, but this effect is usually small.

You perform voltage measurement, typically ac-coupled and ranging from 10 to 250 mV, using the arrangement in Figure A.

This arrangement feeds the measured voltage to a BNC 50Ω, back-terminated cable, which drives the oscilloscope through a dc-blocking capacitor and a 50Ω termination. The back termination is strict practice, enforcing a true 50Ω signal path. You can eliminate the unit's 6-dB attenuation if it presents problems with only minor signal degradation in the 25-MHz measurement passband. The termination at the oscilloscope end is not negotiable. Figure B shows a typical observed load transient with no back termination but 50Ω at the oscilloscope. The presentation is clean and well-defined. Figure C removes the cable's 50Ω termination, causing a distorted leading edge, ill-defined peaking, and pronounced postevent ringing. Even at relatively modest frequencies, the cable displays unterminated-transmission-line characteristics, resulting in signal distortion.

In theory, a 1× scope probe using a probe-tip coaxial connection could replace the described circuit, but such probes usually have bandwidth limitations of 10 to 20 MHz. Conversely, a 10× probe is wideband, but the oscilloscope's vertical sensitivity must accommodate the introduced attenuation.

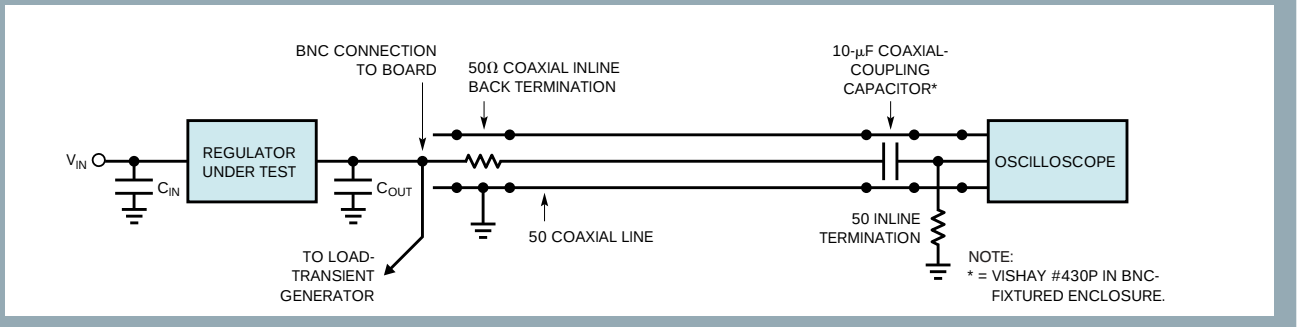

Figure A A coaxial-load-transient voltage-measurement path promotes observed signal fidelity. You can remove the 50Ω back termination with minimal impact on the 25-MHz signal path's integrity.

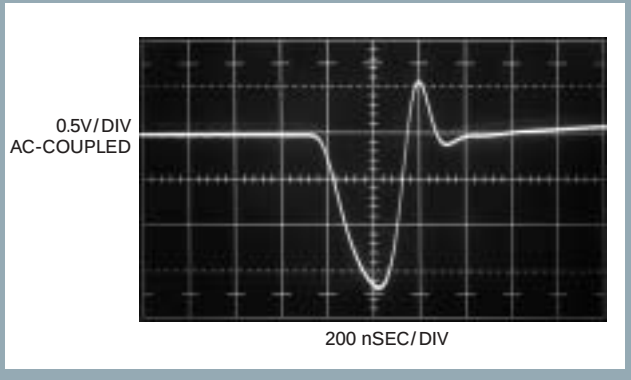

Figure B Observing a typical high-speed transient through Figure A's measurement path presents a clean and well-defined signal.

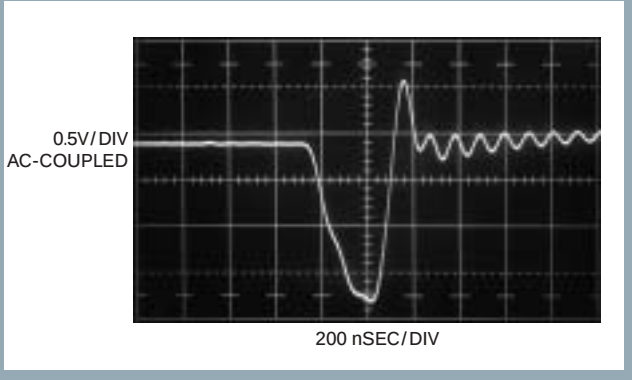

Figure C Measuring Figure B's transient without the 50Ω oscilloscope's termination shows results in waveform distortion and postevent ringing.

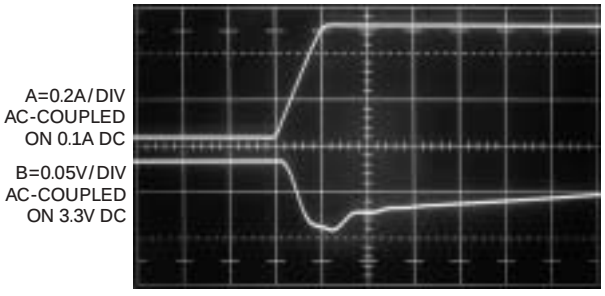

Figure 24 The regulator's output response (Trace B) to a 100-nsec rise-time current step (Trace A) for C_{OUT} is 10 µF. The response decay peaks at 75 mV.

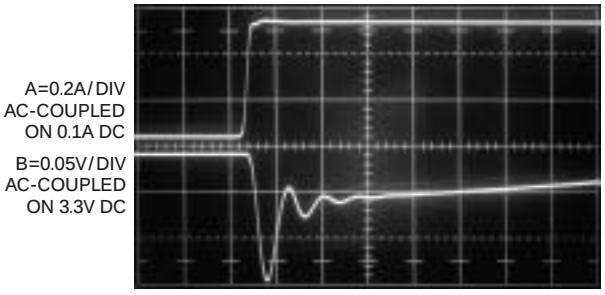

Figure 25 Faster rise-time current step (Trace A) increases response-decay peak (Trace B) to 140 mV, indicating increased regulation loss versus frequency.

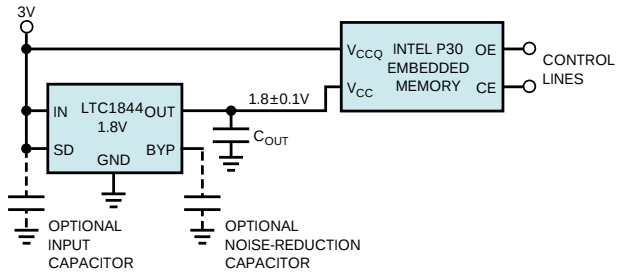

Figure 26 The P30 embedded-memory voltage regulator must maintain a ±0.1V error band. Control-line movement causes 50-mA load steps, necessitating attention to C_{OUT} selection.

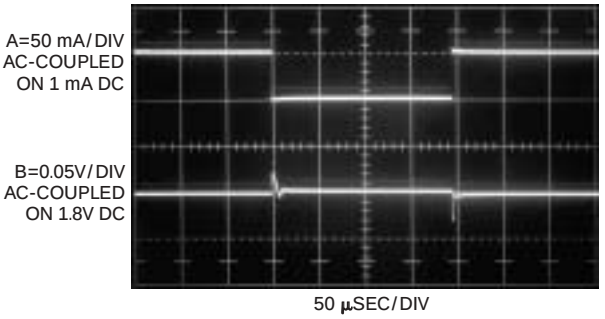

Figure 27 A 50-mA load step (Trace A) results in 30-mV regulator-response peaks, two times better than error-budget requirements. C_{OUT} is a low-loss, 1-µF capacitor.

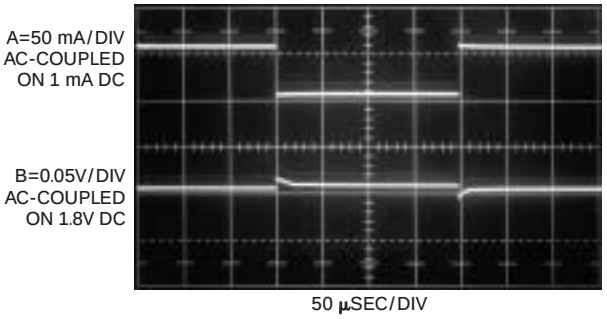

Figure 28 Increasing the value of C_{OUT} to 10 µF decreases regulator-output peaks to 12 mV, almost six times better than required.

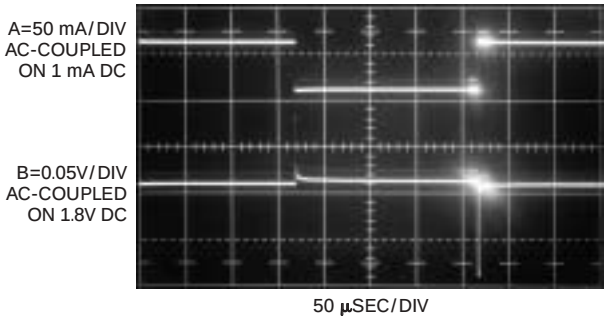

Figure 29 A low-grade, 10-µF C_{OUT} causes 100-mV regulator-output peaks (Trace B), violating the P30 regulator's memory limits. The scope photo intensifies the trace's latter portion for clarity.

ing to a 0.5A, 100-nsec rise-time step on a 0.1A dc load (Trace A). Response decay (Trace B) peaks at 75 mV with some following aberrations. Decreasing Trace A's load-step rise time (Figure 25) almost doubles Trace B's response error, with attendant enlarged following aberrations. This scenario indicates increased regulator error at higher frequency.

All regulators present increasing error with frequency—some more than others. A slow load transient can unfairly make a poor

TABLE 1 INTEL P30 EMBEDDED-MEMORY VOLTAGE-REGULATOR ERROR BUDGET

Parameter	Limits
Intel-specified supply limits	1.8V±0.1V
LTC1844-regulator initial accuracy	±1.75% (±31.5 mV)
Dynamic-error allowance	±68.5 mV

A TRIMLESS, CLOSED-LOOP-TRANSIENT-LOAD TESTER

Eliminating a FET-based design's ac trims is an attractive option; however, eliminating the dc trim is also important. The circuit in Figure A trades circuit complexity to achieve this goal. The circuit includes two amplifiers, A_1 and A_2. A_2 replaces the dc trim by measuring the circuit's dc input and comparing it with Q_1's emitter dc level and controlling A_1's positive input to stabilize the circuit. The system filters high-frequency signals at A_2's inputs, and these signals do not corrupt A_2's stabilizing action. A useful way to consider circuit operation is that A_2 balances its inputs and, hence, the circuit's input and output, regardless of A_1's dc-input errors. You can set the dc-current bias to any desired point by directing a variable reference source to A_2's positive input. The arrangement of the network's resistors yields a minimum load current of 10 mA, avoiding loop disruption for currents near zero.

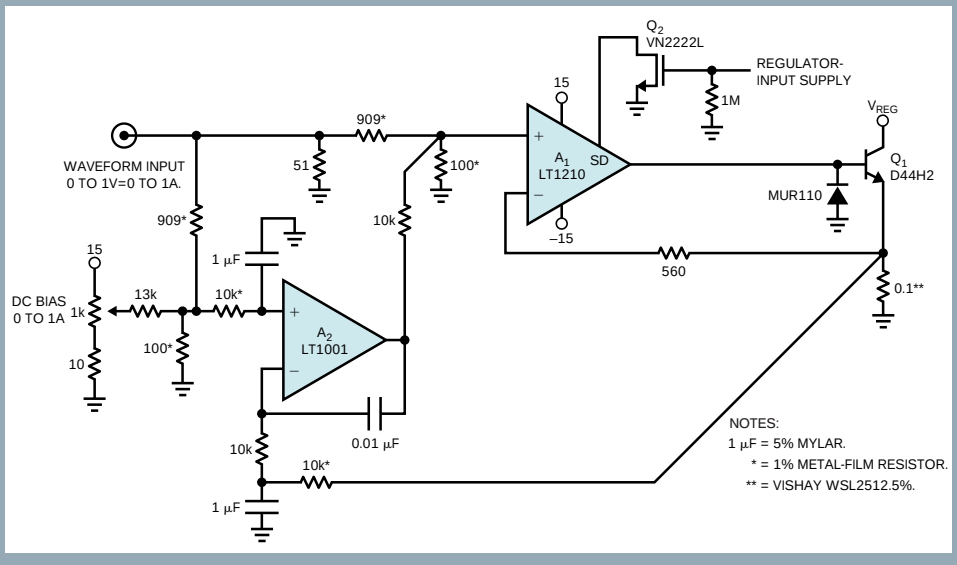

Figure A A_2's feedback controls A_1's dc errors, eliminating trim. Filtering restricts A_2's response to dc and low frequency.

regulator look good. Transient-load testing that does not indicate some response outside regulator bandwidth is suspect.

The Intel (www.intel.com) embedded-memory voltage regulator furnishes a good, practical example of the importance of voltage-regulator-load-step performance. The memory requires a 1.8V supply, typically regulated down from 3V. Although current requirements are relatively modest, supply tolerances are tight. Table 1 shows only 0.1V allowable excursion from 1.8V, including all dc and dynamic errors. The LTC1844-1.8 regulator has a 1.75% initial tolerance at 31.5 mV, leaving only a 68.5-mV dynamic-error allowance. Figure 26 shows the test circuit. Memory-control-line movement causes 50-mA load transients, necessitating attention to capacitor selection. (The LTC1844-1.8's noise-bypass pin works with an optional external capacitor to achieve low output noise. This application, however, does not require it, and remains unconnected.) If the regulator is close to the power source, C_{IN} is optional. If not, use a high-grade, 1-µF capacitor for C_{IN}. C_{OUT} is a low-loss, 1-µF type. In all other respects, the circuit appears deceptively routine. A load-transient generator provides Figure 27's output-load test step (Trace A). This test uses Figure 8's circuit and changes Q_1's emitter-current shunt to 1Ω. Trace B's regulator response shows just 30-mV peaks, more than two times better than necessary. Increasing C_{OUT} to 10 µF (Figure 28) reduces peak output error to 12 mV, almost six times better than specification. However, a low-grade 10-µF—or 1-µF, for that matter—capacitor produces Figure 29's unwelcome surprise. Severe peaking error on both edges occurs with 100 mV observable on the negative-going edge. (The photograph shows an intensified version of Trace B's latter portion to aid clarity.) This figure is well outside the error budget and would cause unreliable memory operation (references 4, 5, and 6). EDN

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AUTHOR BIOGRAPHY

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BY JIM WILLIAMS • LINEAR TECHNOLOGY CORP

Designing instrumentation circuitry with rms/dc converters

RMS CONVERTERS RECTIFY AVERAGE RESULTS.

Using rms to measure waveforms furnishes the most accurate amplitude information (**Reference 1**). Rectify-and-average schemes, which you usually calibrate to a sine wave, are accurate for only one waveshape, however. Departures from this waveshape result in pronounced errors. Although accurate, rms conversion often entails limited bandwidth, restricted range, complexity, and difficult-to-characterize dynamic and static errors. Recent developments address these issues and also improve accuracy. **Table 1** at the Web version of this article at www.edn.com/ms4228 shows Linear Technology's (www.linear.com) LTC1966/LTC1967/LTC1968 device family. The devices feature low-frequency accuracy, including linearity and gain error, of 0.5% and 1% error at bandwidths extending to 500 kHz. These converters employ a sigma-delta-based computational scheme to achieve their performance.

Figure 1's pinout descriptions and basic circuits reveal an easily applied device. An output filter capacitor is all that is necessary to form a functional rms/dc converter. The **figure** shows split- and single-supply-powered variants. Such ease of implementation invites a broad range of application; examples begin with **Figure 2**.

ISOLATED POWER-LINE MONITOR

Figure 2's ac-power-line monitor has 0.5% accuracy over a sensed 90 to 130V-ac input and provides a safe, fully isolated output. Conversion of rms provides accurate reporting of ac-line voltage, regardless of waveform distortion, which is common. T_1's ratio divides down the ac-line voltage. An isolated and reduced potential appears across T_1's secondary, B, at which it resistively scales and presents itself to IC_1's input. Power for IC_1 comes from T_1's secondary, A, which you rectify, filter, and zener-regulate to dc. IC_2 provides a numerically convenient output from gain. You can increase accuracy by biasing T_1 to an optimal loading point, which the relatively low-resistance-divider values facilitate. Similarly, although IC_1 and IC_2 can operate from one supply, split supplies maintain symmetrical T_1 loading. You calibrate the circuit by adjusting the 1-kΩ trim for 1.20V output with the ac line at 120V ac. You make this adjustment using a variable-ac-line transformer and a floating rms voltmeter (see **sidebar** "AC-measurement and signal-handling practice" at the Web version of this article at www.edn.com/ms4228 for recommendations on rms voltmeters and other ac-measurement-related gossip).

Figure 3's error plot shows 0.5% accuracy from 90 to 130V ac, degrading to 1.4% at 140V ac. The beneficial effect of trimming at 120V ac is evident; trimming at full-scale would result in larger overall error, primarily due to nonideal-transformer behavior. Note that the data is specific to the transformer. Substitution for T_1 necessitates circuit-value changes and recharacterization.

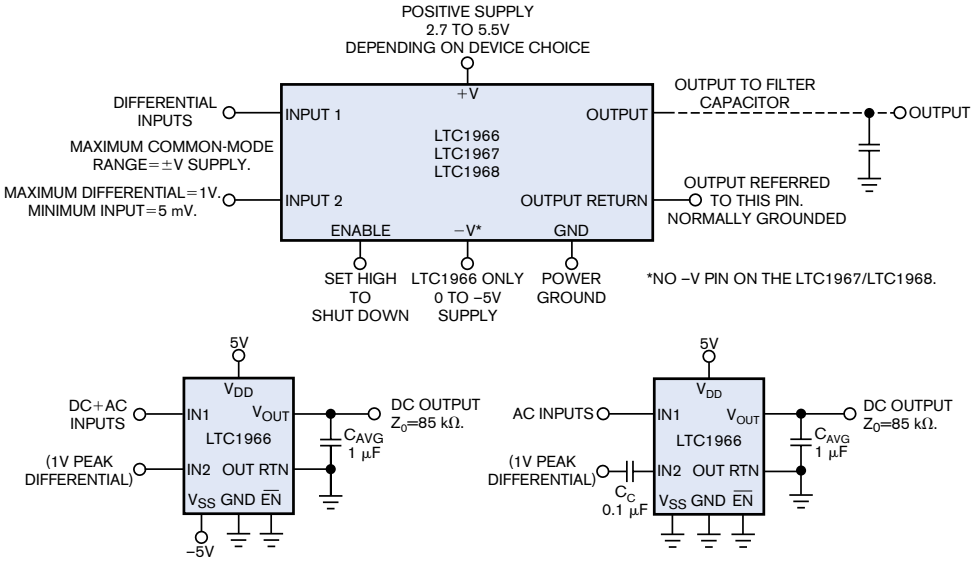


Figure 1 The pinout descriptions (top) and basic circuits (bottom) include the rms converter's pin functions and application circuits. The pins' descriptions are equivalent in all the devices, with only minor differences.

FULLY ISOLATED

RMS/dc converters commonly require accurate rms-amplitude measurement of an SCR's (silicon-controlled rectifier's) chopped ac-line waveforms. The

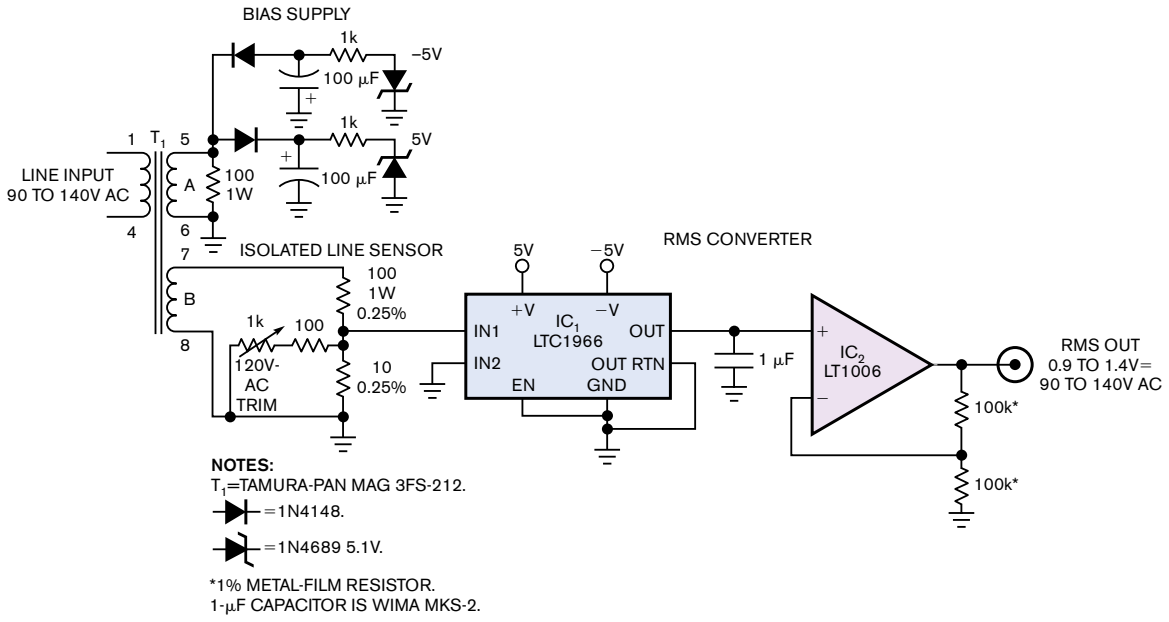


Figure 2 This isolated power-line monitor senses with a transformer and provides 0.5% accuracy from 90 to 130V-ac input. Loading the transformer secondary optimizes the voltage conversion's linearity.

SCR's fast sine-wave switching complicates this measurement because this speed introduces odd waveshapes with high-frequency harmonic content. **Figure 4**'s conceptual SCR-based ac/dc converter is typical. The SCRs alternatively chop the 220V-ac line, responding to a loop-enforced, phase-modulated trigger to maintain a dc output. **Figure 5**'s waveforms show typical operation. Trace A represents one ac-line phase, and Trace B represents the SCR cathodes. The SCR's irregularly shaped waveform contains dc and high-frequency harmonics, requiring wideband rms conversion for measurement. Additionally, for safety and system-interface considerations, you must fully isolate the measurement.

Figure 6 provides isolated power and data-output paths to an rms/dc converter, permitting safe, wideband, digital output-rms

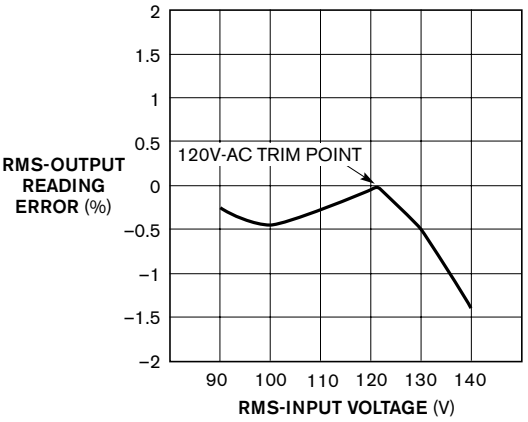


Figure 3 The line monitor has 0.5% accuracy from 90 to 130V ac, degrading to 1.4% accuracy at 140V ac. Almost all the error is due to transformer parasitic losses.

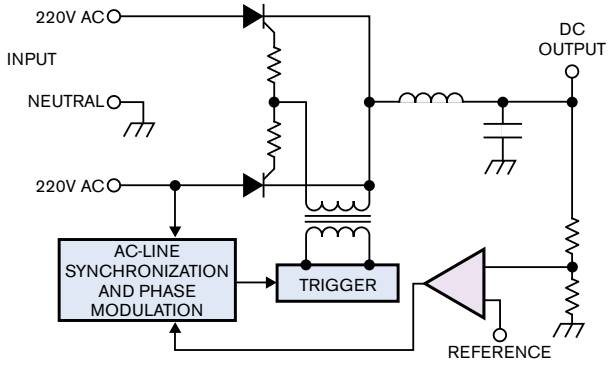


Figure 4 This ac/dc converter is typical of SCR-based designs. Feedback directs the SCR, which synchronizes with the ac line. The SCR's trigger-phase modulation controls the dc output.

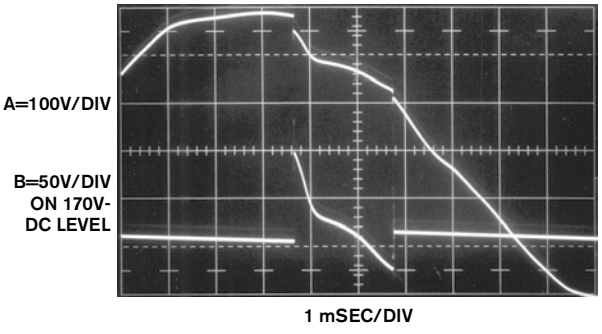


Figure 5 Trace A is the ac line of the SCR-based ac/dc converter. Trace B is the waveform at the SCR cathode. It contains dc and high-frequency harmonics that require wideband rms measurement to ensure accurate regulation.

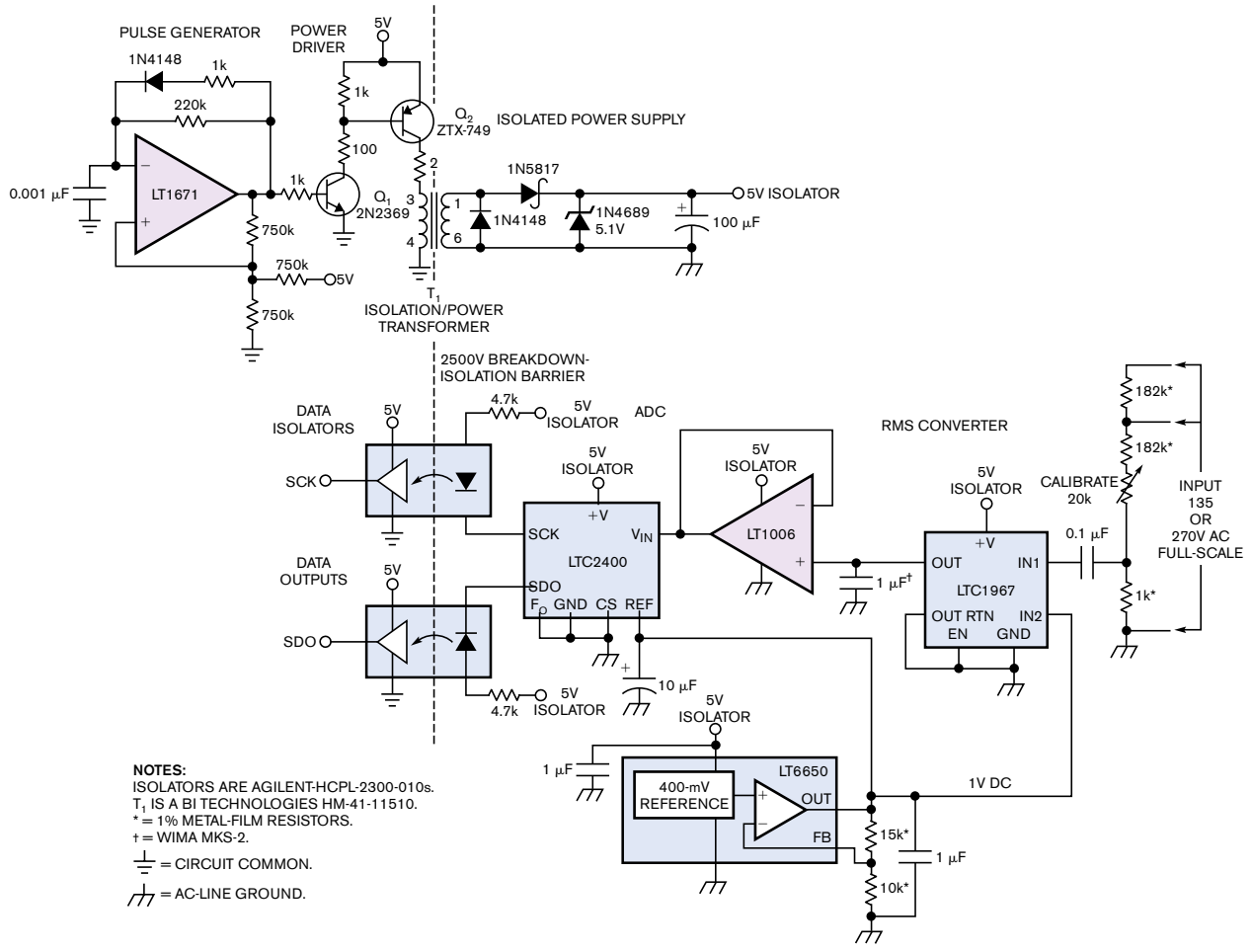


Figure 6 Optoisolators provide a safe, low-voltage digital output for this wideband-rms-measurement circuit. T_1 and associated circuitry provide isolated power for the rms converter, and a resistive divider performs high-voltage ac sensing. An ADC provides a serial output to the optoisolators. The accuracy of this circuit is 1% over a 200-kHz bandwidth.

measurement. A pulse-generator-configured comparator combines with Q_1 and Q_2 to drive T_1, resulting in isolated 5V power at T_1's rectified, filtered, and zener-regulated output. The rms/dc converter senses either 135 or 270V-ac full-scale inputs through a resistive divider. The converter's dc output feeds a self-clocked, serially interfaced ADC; optocouplers convey output data across the isolation barrier. The LTC6650 provides a 1V reference to the ADC and biases the rms/dc converter's inputs to accommodate the voltage divider's ac swing. You accomplish calibration by adjusting the 20-kΩ trim and noting that output data agrees with the input ac voltage. Circuit accuracy is within 1% in a 200-kHz bandwidth.

LOW-DISTORTION AC-LINE RMS REGULATOR

Almost all functioning ac-line-voltage regulators rely on some form of waveform chopping, clipping, or interruption. This requirement promotes efficiency but introduces waveform distortion, which is unacceptable in some applications. **Figure 7** regulates the ac line's rms value within 0.25% over wide input swings and introduces no distortion. It accomplishes this task by continuously controlling the conductivity of a series-pass MOSFET in the ac line's path. Enclosing the MOSFET in a diode bridge permits it to operate during both ac-line polarities.

You apply the ac-line voltage to the Q_2-diode bridge. A calibrated variable-voltage divider senses this bridge and feeds IC_1. You route IC_1's output, representing the regulated line's rms value, to control amplifier IC_2 and compare it with a reference. IC_2's output biases Q_1, controlling drive to a photovoltaic optoisolator. The optoisolator's output voltage provides level-shifted bias to diode-bridge-enclosed Q_2, closing a control loop, which regulates the output's rms voltage against ac-line and -load shifts. RC components in IC_2's local feedback path stabilize the control loop. The loop operates Q_2 in its linear region, much like a common low-voltage dc linear regulator. The result is the absence of introduced distortion at the expense of lost power. Heat dissipation constrains the available output power. For example, when you set the output adjustment to regulate 10V below the normal input, Q_2 dissipates about 10W at 100W output. You can improve this figure, however. The circuit regulates for $V_{IN} \geq 2V$ above V_{OUT}, but operation in this region risks regulation dropout as V_{IN} varies.

Circuit details include JFET Q_5 and associated components. The passive components associated with Q_5's gate form a slow

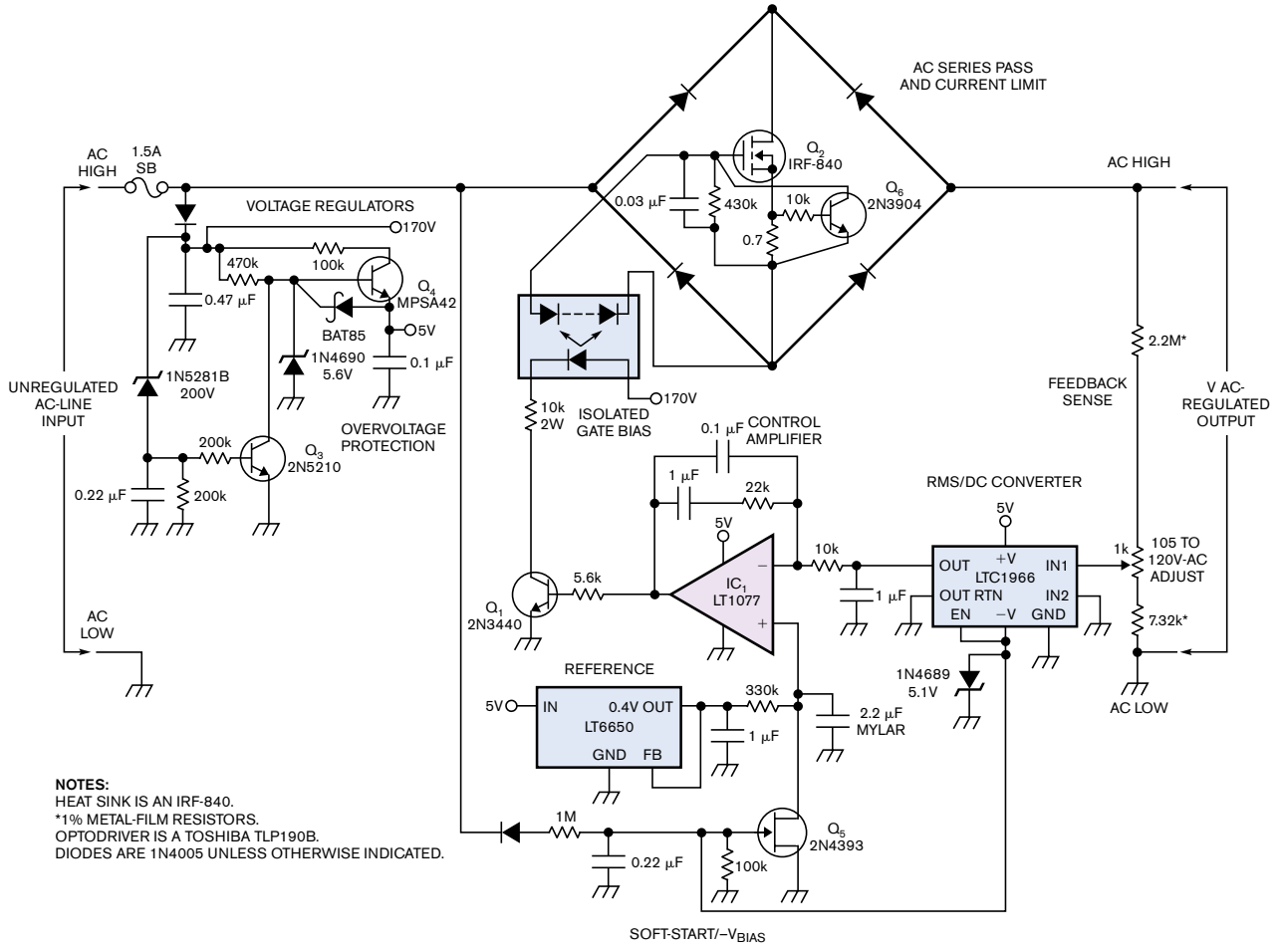


Figure 7 This ac-line-voltage regulator introduces no waveform distortion. IC_2 senses the rms value of line voltage and compares it with a reference. IC_2 then biases the photovoltaic optocoupler through Q_1. Q_2 sets the diode bridge's conductivity and closes the control loop. The input voltage must be 2V higher than the output voltage to maintain regulation.

turn-on negative supply for IC_1. They also provide gate bias for Q_5, a soft-start transistor that prevents abrupt ac power application to the output at start-up. When power is off, Q_5 conducts, holding IC_2's positive input low. When you apply power, IC_1 initially has a 0V reference, causing the control loop to set the output at zero. As the 1 MΩ, 0.22-µF combination charges, Q_5's gate moves negative, causing its channel conductivity to gradually decay. Q_5 ramps off, IC_2's positive input moves smoothly toward the LT6650's 400-mV reference, and the ac output similarly ascends toward its regulation point. Current sensor Q_6, measuring across the 0.7Ω shunt, limits output current to approximately 1A. At normal line inputs of 90 to 135V ac, Q_4 supplies 5V operating bias to the circuit. If line voltage rises beyond this point, Q_3 comes on, turning off Q_4 and shutting down the circuit.

GAIN-OF-1000 PREAMPLIFIERS

The preceding circuits furnish high-level inputs to the rms converter. Many applications lack this advantage and require some form of preamplifier. High gain preamplification for the rms converter requires more attention than you might suppose. The preamplifier must have low offset error because the rms converter (desirably) processes dc as legitimate input. More subtly, the preamplifier must have far more bandwidth than is immediately apparent. The amplifier's −3-dB bandwidth is of interest, but its closed-loop 1%-amplitude-error bandwidth must be high enough to maintain accuracy over the rms converter's 1%-error passband. This requirement is not trivial, because very high open-loop gain at the maximum frequency of interest is necessary to avoid inaccurate closed-loop gain.

Figure 8 shows a gain-of-1000 preamplifier that preserves the LTC1966's dc to 6-kHz, 1% accuracy. The amplifier may be either ac- or dc-coupled to the rms converter. The 1-mV full-scale input splits into high- and low-frequency paths. IC_1 and IC_2, which are both ac-coupled, take a cascaded, high-frequency gain of 1000. Chopper-stabilized IC_3 which is dc-coupled, also has a gain of 1000, but its RC-input filter restricts it to operate only at dc and low frequency. Assuming the switch is set to dc+ac, high- and low-frequency-path information recombine at the rms converter. The high-frequency path's 650-kHz, −3-dB response combines with the low-frequency section's microvolt-level offset to preserve the rms converter's dc to 6-kHz 1% error. If you require only ac response, set the switch to the appropriate position. The minimum processable input, which the circuit's noise floor sets, is 15 µV.

The LTC1968, with a 500-kHz, 1%-error bandwidth, poses a

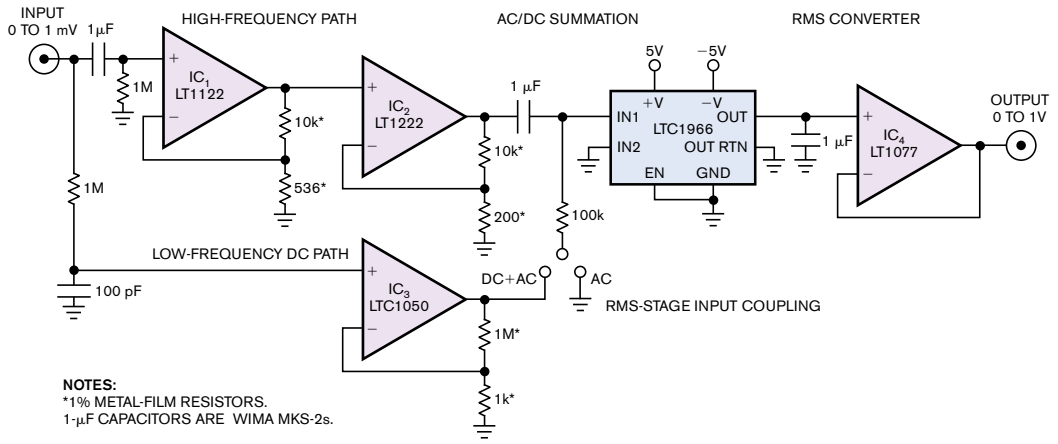
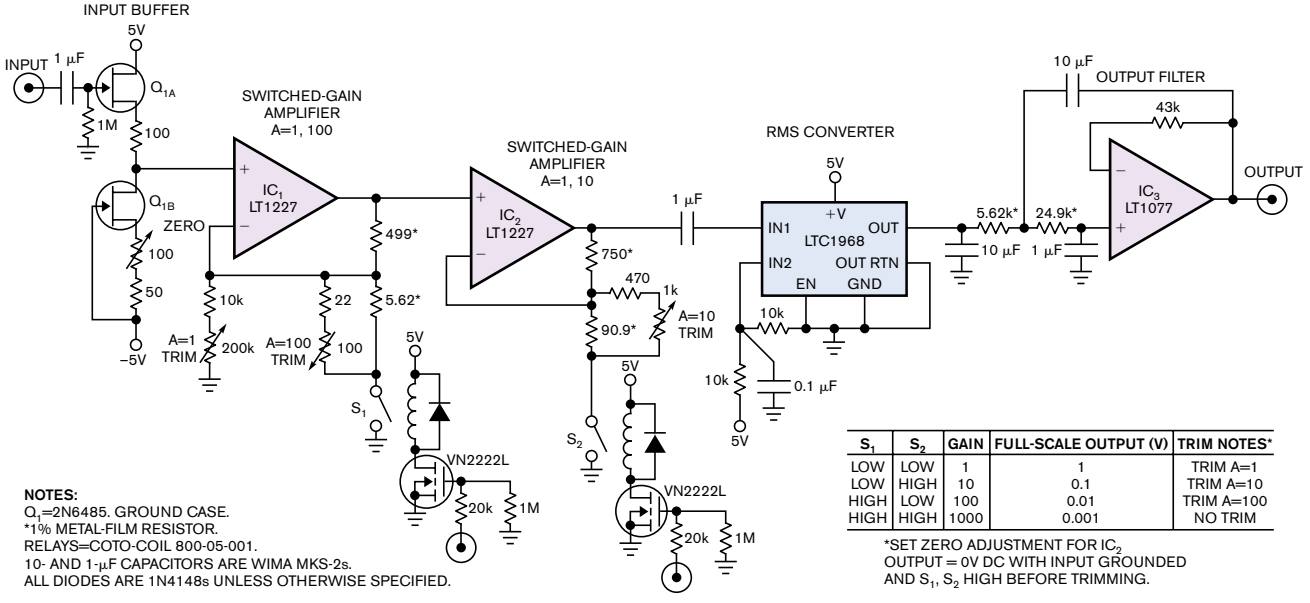


Figure 8 This gain-of-1000 preamplifier allows rms-to-dc conversion with 1-mV full-scale sensitivity. The input splits into high- and low-frequency paths that recombine at the rms converter. The amplifier's 650-kHz, −3-dB bandwidth preserves the rms converter's 6-kHz, 1%-error bandwidth. The noise floor of this circuit is 15 µV.



S_1	S_2	GAIN	FULL-SCALE OUTPUT (V)	TRIM NOTES*
LOW	LOW	1	1	TRIM A=1
LOW	HIGH	10	0.1	TRIM A=10
HIGH	LOW	100	0.01	TRIM A=100
HIGH	HIGH	1000	0.001	NO TRIM

*SET ZERO ADJUSTMENT FOR IC_2 OUTPUT = 0V DC WITH INPUT GROUNDED AND S_1, S_2 HIGH BEFORE TRIMMING.

Figure 9 This switched-gain, 10-MHz, −3-dB ac preamplifier preserves the LTC1968's 500-kHz, 1%-error bandwidth. The decade-ranged gains allow a 1-mV full-scale reading with a 20-µV noise floor. The JFET-input stage provides high input impedance. AC coupling and a third-order Sallen-Key filter maintain 1% accuracy down to 10 Hz.

significant challenge for an accurate preamplifier, but the circuit in **Figure 9** meets the requirement. This design features decade-ranged gain to 1000 with a 1%-error bandwidth beyond 500 kHz, preserving the rms converter's 1%-error bandwidth. Its 20-µV noise floor maintains wideband performance at microvolt-level inputs. Q_{1A} and Q_{1B} form a low-noise buffer, permitting high-impedance inputs. IC_1 and IC_2, which are both gain-switchable, take cascaded gain in accordance with the **figure**'s table. You set the gains using reed relays, which a 2-bit code controls. IC_2's output feeds the rms converter, and a Sallen-Key active filter smoothes the converter's output. The circuit maintains 1% error over a 10-Hz to 500-kHz bandwidth at all gains due to the preamplifier's −3-dB, 10-MHz bandwidth. You can eliminate the 10-Hz, low-frequency restriction with a dc-stabilization path similar to the one in **Figure 8**, but you would have to switch its gain in concert with the IC_1-IC_2 path.

Figure 10 shows preamplifier response to a 1-mV input step at a gain of 1000. IC_2's output is singularly clean, with trace thickening in the pulse's flat portions due to the 20-µV noise floor. The 35-nsec rise time indicates a 10-MHz bandwidth. To calibrate this circuit, first set S_1 and S_2 high, ground the input, and trim the zero adjustment for 0V dc at IC_2's output. Next, set S_1 and S_2 low, apply a 1V, 100-kHz input, and trim A=1 for unity gain, which you measure at the circuit output, in accordance with the table in **Figure 9**. Continue this procedure for the remaining three gains in the table. A good way of generating the required accurate low-level inputs is to set a 1V-ac lev-

el and divide it down with a high-grade 50Ω attenuator, such as the Hewlett-Packard (www.hp.com) 350D or the Tektronix (www.tektronix.com) 2701. It is prudent to verify the attenuator's output with a precision rms voltmeter (see **sidebar** "AC-measurement and signal-handling practice" at the Web version of this article at www.edn.com/ms4228).

MEASURING QUARTZ-CRYSTAL RMS CURRENT

Quartz-crystal rms operating current is critical to long-term stability, temperature coefficient, and reliability. You must minimize introduced parasitics, particularly capacitance, which corrupt crystal operation. This requirement complicates accurate determination of rms-crystal current. **Figure 11**, a form of **Figure 9**'s wideband amplifier, combines with a commercially available closed-core current probe to permit the measurement. An rms/dc converter supplies the rms value. The quartz-crystal test circuit in dashed lines exemplifies a typical measurement situation. The Tektronix CT-2 current probe monitors crystal current and introduces minimal parasitic loading. The probe's 50Ω termination allows direct connection to IC_1 without the FET buffer in **Figure 9**. Additionally, because quartz crystals are uncommon at frequencies lower than 4 kHz, IC_1's gain does not extend to low frequency.

Figure 12 shows the results. A crystal drive, which you take at Q_1's collector (Trace A), causes a 25-μA-rms crystal current, which appears at the rms/dc-converter input (Trace B). The trace enlargement is due to the preamplifier's 5-μA-rms equivalent-noise contribution. **Table 2** at the Web version of this article at www.edn.com/ms4228 details characteristics of two Tektronix closed-core current probes. The primary trade-off is low-frequency error versus sensitivity. The current probes contribute essentially no probe noise, and capacitive loading is notably low. You calibrate the circuit by putting 1-mA rms current through the probe and adjusting the indicated trim for a 1V circuit output. To generate the 1 mA, drive a 1-kΩ, 0.1% resistor with 1V rms.

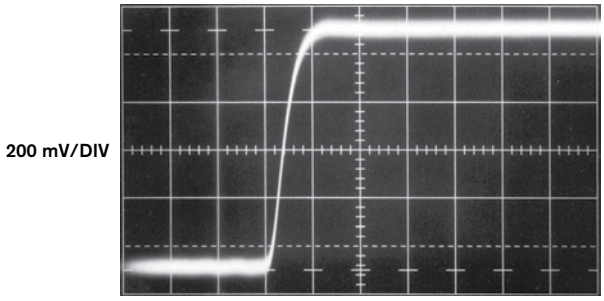


Figure 10 IC_2 in Figure 9 responds to a 1-mV input step with a gain of 1000. The 35-nsec rise time indicates the 10-MHz bandwidth. The thickened trace at the flat portions of the pulse represents the noise floor.

STABLE AC-VOLTAGE STANDARD

Figure 13 uses the rms/dc converter's stability in an ac-voltage standard. Initial circuit accuracy is 0.1%, and six months of drift at 20 to 30°C remains within that figure. Additionally, the 4-kHz operating frequency is within 0.01%, and distortion is less than 30 ppm. IC_1 and its power buffer, IC_3, sense across a bridge comprising a 4-kHz quartz crystal and an RC impedance in one arm; resistors and an LED-driven photocell comprise the other arm. IC_1 sees positive feedback at the crystal's 4-kHz resonance, promoting oscillation. Negative feedback, stabilizing oscillation amplitude, occurs through a control path, which includes an rms/dc converter and an amplitude-control amplifier, IC_5. IC_5 acts on the difference between IC_3's rms-converted output and the LT1009 voltage reference. Its output controls the LED-driven photocell to set IC_1's negative feedback. RC components in IC_5's feedback path stabilize the control loop. The 50-kΩ trim sets the optically driven resistor's value to the point at which IC_3's lowest output distortion occurs and maintains adequate loop stability.

Normally, you would ground the bridge's "bottom." Although this connection works, it subjects IC_1 to common-mode swings, increasing distortion due to IC_1's finite common-mode rejection versus frequency. IC_2 eliminates this concern

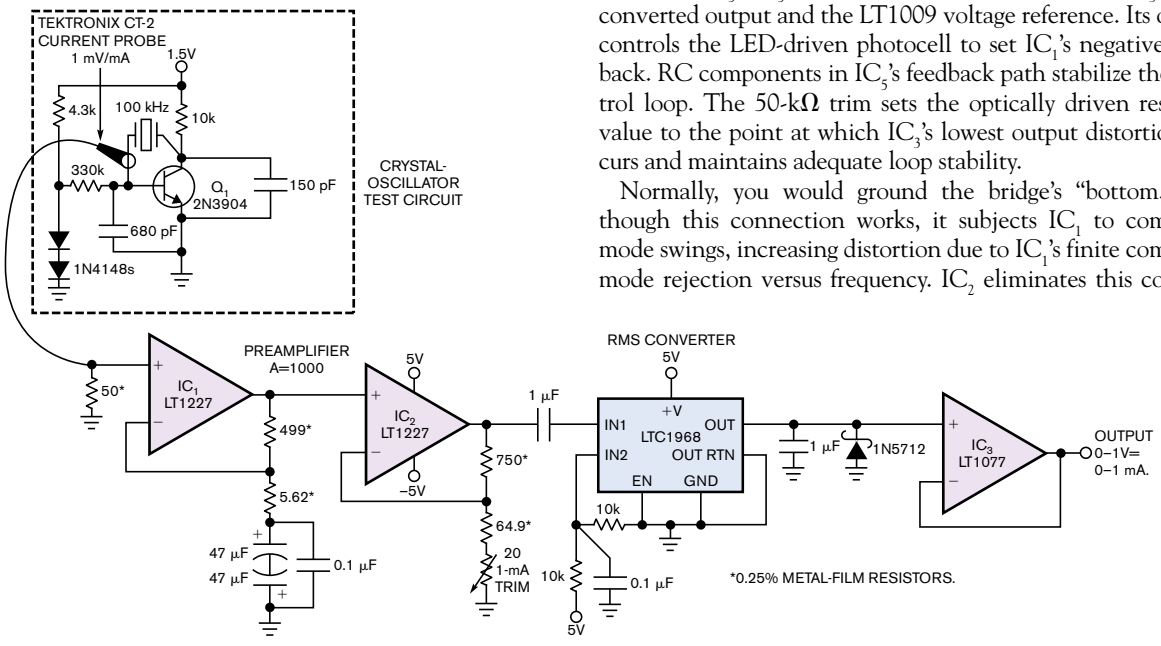


Figure 11 The circuit of Figure 9 adapts to the isolated true-rms measurement of the current in a quartz crystal. The current probe's 50Ω impedance allows the elimination of the FET-input buffer and direct connection to IC_1. The current probe does not appreciably load the crystal in this oscillator test circuit.

by forcing the bridge's midpoints and, hence, common-mode voltage to 0V but not influencing desired circuit operation. It accomplishes this task by driving the bridge bottom to force its input differential to zero. IC_2's output swing is 180° out of phase with IC_3's circuit output. This action eliminates common-mode swing at IC_1, reducing circuit output distortion by more than an order of magnitude. **Figure 14** shows the circuit's 1.414V-rms (2V peak) output in Trace A, and Trace B's distortion constituents include noise, fundamental-related residue, and second-harmonic components.

The 4-kHz crystal is a relatively large structure with a high Q factor. Normally, it would require more than 30 sec to start and arrive at full, regulated amplitude. You avoid this drawback by including the Q1-LTC201-switch circuitry. At start-up, IC_5's output goes high, biasing Q_1. Q_1's collector goes low, turning on the LTC201. This action sets IC_1's gain abnormally high, increasing bridge drive and accelerating crystal start-up. When the bridge arrives at its operating point, IC_5's output drops to a lower value, Q_1 and the LTC201 switch off, and the circuit moves into normal operation. Start-up time is several seconds.

The circuit requires trimming for amplitude accuracy and lowest distortion. You perform the distortion trim first. Adjust the trim for minimal output distortion, which you measure on a distortion analyzer. Note that the absolute lowest level of distortion coincides with the point at which control-loop gain is just adequate to maintain oscillation. As such, find this point and retreat from it into the control loop's active region. This retreat necessitates giving up about 5-ppm distortion, but you can achieve 30 ppm with good control-loop stability. You trim output amplitude with the indicated adjustment for exactly 1.414V rms (2V peak) at the circuit output.

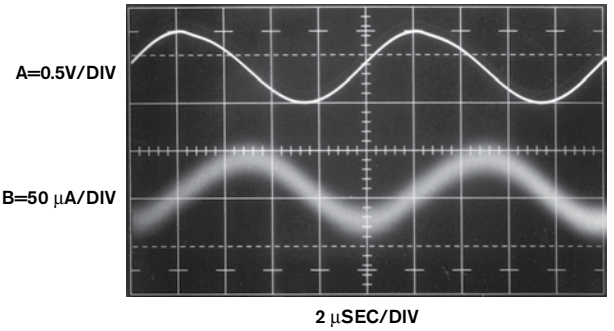


Figure 12 Trace A shows the crystal voltage, and Trace B shows the crystal current for the circuit in Figure 11. The 25-µA rms-crystal-current measurement includes the 5-µA noise-floor contribution of the preamplifier.

RANDOM-NOISE GENERATOR

Figure 15 uses the rms/dc converter in a leveled-output-random-noise generator. Noise diode D_1 ac-biases IC_1, operating at a gain of two. IC_1's output feeds a 1- to 500-kHz, switch-selectable lowpass filter. The filter output-biases the variable-gain amplifier, IC_2-IC_3. IC_2, a current-controlled transconductance amplifier, and IC_3, an output amplifier, reside on one chip. This stage takes ac gain, biases the LTC1968 rms/dc converter, and acts as the circuit's output. The rms-converter output at IC_4

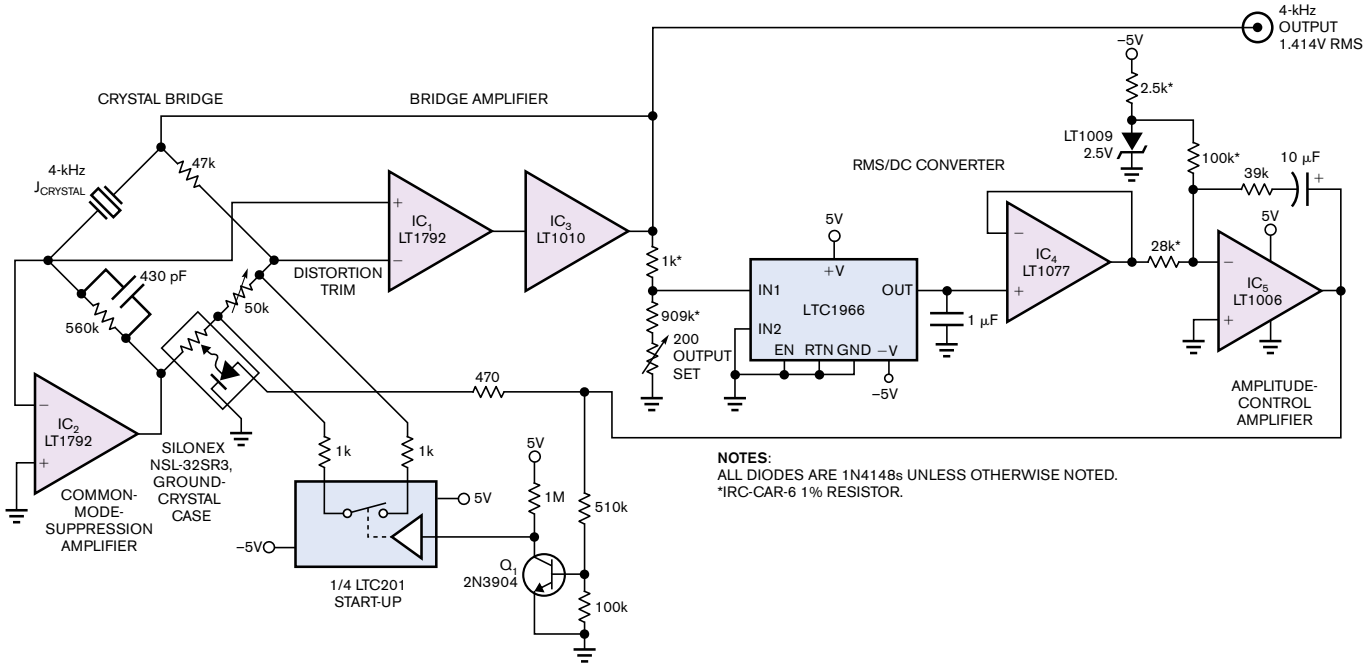


Figure 13 This quartz-stabilized sine-wave-output-ac reference has 0.1% long-term amplitude stability. The frequency accuracy is 0.01% with less-than-30-ppm distortion. The positive feedback around IC_1 causes oscillation at the crystal's resonant frequency. Amplifier IC_5 acts on the rms-amplitude output of IC_4 to supply a negative feedback to IC_1 through the bridge network that stabilizes the rms-output amplitude. The optocoupler minimizes feedback-induced distortion. Switch Q_1 closes during start-up, which ensures the rapid build up of oscillations.

feeds back to gain-control amplifier IC_5, which compares the rms value with a variable portion of the 5.1V zener potential. IC_5's output sets IC_2's gain through the 3-kΩ resistor, completing a control loop to stabilize noise-rms-output amplitude. The RC components in IC_5's local feedback path stabilize this loop. You can vary the output amplitude using the 10-kΩ potentiometer; a switch permits external voltage control. Q_1 and associated components, a soft-start circuit, prevent output overshoot at power turn-on. **Figure 16** shows circuit-output noise in the 10-kHz filter position; **Figure 17**'s spectral plot reveals essentially flat rms-noise amplitude over a 500-kHz bandwidth.

RMS-AMPLITUDE-STABILIZED LEVEL CONTROLLER

Figure 18 borrows the previous circuit's gain-control loop to stabilize the rms amplitude of an arbitrary input waveform. You apply the unregulated input to variable-gain amplifier IC_1-IC_2 which feeds IC_3. DC coupling at IC_1-IC_2 permits passage of low-frequency inputs. An rms/dc converter, comprising IC_4 and IC_6, takes IC_3's output, which feeds IC_5's gain-control amplifier. IC_5 compares the rms value with a variable reference and biases IC_1,

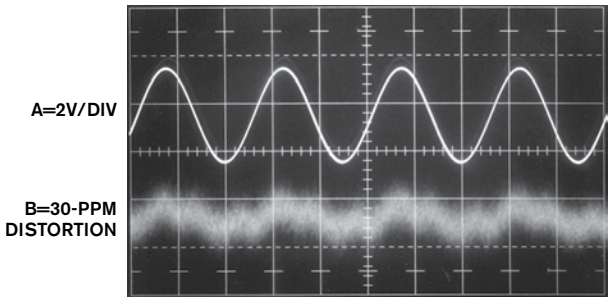


Figure 14 Trace A shows the 1.414V-rms (2V peak) reference output from IC_3. Trace B shows the 30-ppm distortion in the output. The distortion's constituents include noise, fundamental-related residue, and second-harmonic components.

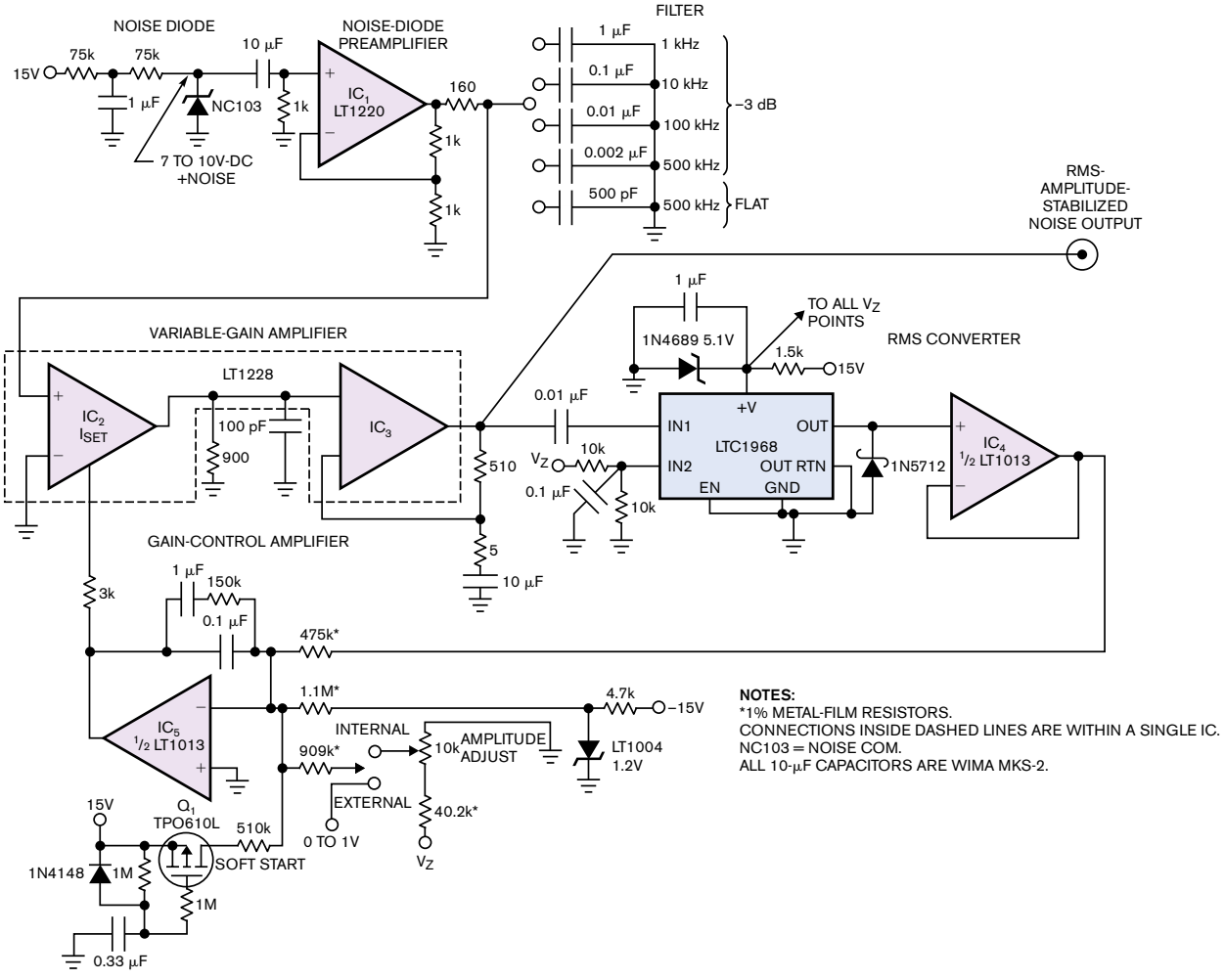


Figure 15 This circuit creates a random-noise generator with rms-leveled output. IC_1 filters and amplifies zener-diode noise. The output of the variable-gain amplifier converts to rms. The rms output feeds back to gain-control amplifier IC_5, which closes the loop to the variable-gain amplifier. A potentiometer or external input to IC_5 allows you to set the noise output to different values.

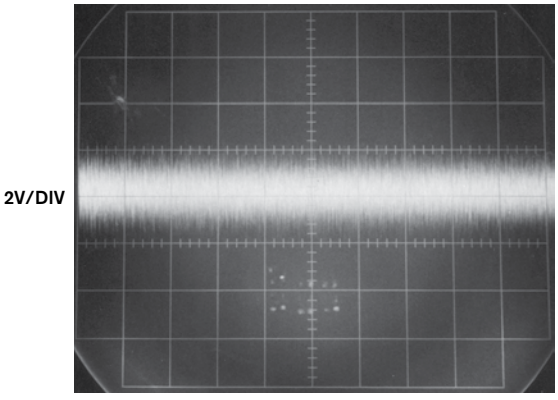


Figure 16 The output of the circuit in Figure 14 is in the 10-kHz filter position.

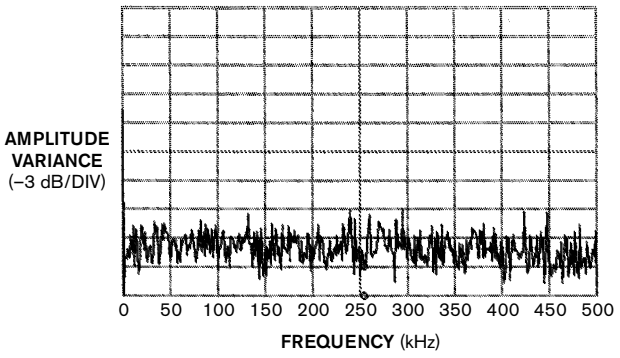


Figure 17 The amplitude over frequency for the random-noise generator is essentially flat to 500 kHz. The NC103 noise diode contributes to an even noise-spectrum distribution, and the rms converter and control loop stabilize the amplitude. The measurement sweep time is 2.8 minutes, and the resolution bandwidth is 100 Hz.

closing a gain-control loop. The 0.15-µF feedback capacitor stabilizes this loop, even for waveforms lower than 100 Hz. This feedback action maintains waveshape and stabilizes output-rms amplitude despite large variations in input amplitude. You can set the desired output level with the indicated potentiometer, or you can switch in an external control voltage.

Figure 19 shows output response (Trace B) to abrupt reference-level-setpoint changes (Trace A). The output settles within 60 msec for ascending and descending transitions. You can achieve faster response by decreasing IC_5's compensation capacitor, but the circuit would then be unable to process low-frequency waveforms. Similar considerations apply to **Figure**

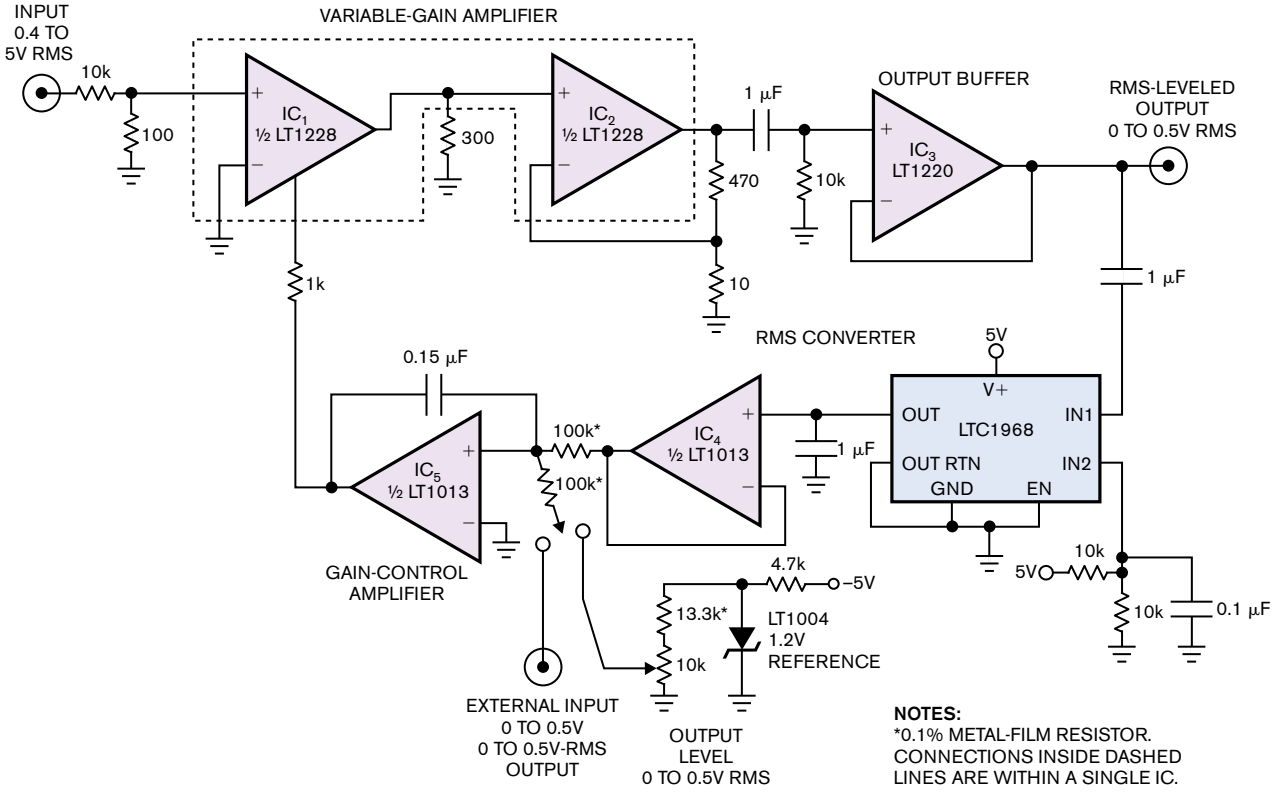


Figure 18 This rms-amplitude level-control circuit uses the gain-control loop of Figure 15. The amplifiers IC_1, IC_2, and IC_3 provide a variable-gain capability to the input section. The rms converter, IC_6, feeds back to the gain-control amplifier, IC_5, which closes the amplitude-stabilization loop. The variable-reference voltage permits a settable calibrated rms output that is amplitude-independent of the input waveshape.

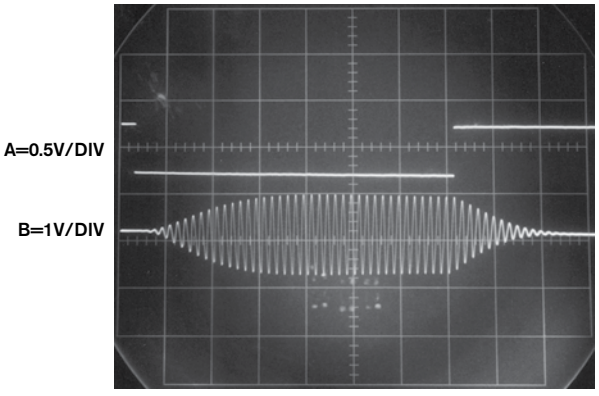


Figure 19 An abrupt change in the reference (Trace A) causes an amplitude-level-control response (Trace B). IC_5's compensation capacitor sets the settling time. This capacitor must be large enough to stabilize the loop at the lowest expected signal-input frequency.

20's response to an input-waveform step change. Trace A is the circuit's input, and Trace B is its output. The output settles in 60 msec due to IC_5's compensation. Reducing compensation value speeds response at the expense of low-frequency-waveform processing capability. Specifications include 0.1% output-amplitude stability for inputs of 0.4 to 5V rms, 1% setpoint accuracy, 0.1- to 500-kHz passband, and 0.1% stability for 20% power-supply deviation. EDN

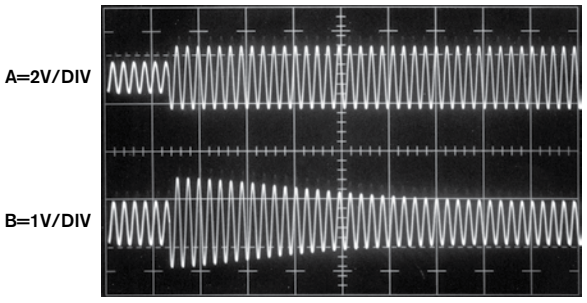


Figure 20 The amplitude-level-control output (Trace B) reacts to a step change in the input signal (Trace A). The slow loop compensation allows the overshoot, but the output settles cleanly.

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AUTHOR'S BIOGRAPHY

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BY JIM WILLIAMS AND MARK THOREN • LINEAR TECHNOLOGY

Novel measurement circuit eases battery-stack-cell design

A TRANSFORMER AND DIODE ON EACH CELL ALLOWS ISOLATED MEASUREMENT.

Automobiles, aircraft, marine vehicles, uninterruptible power supplies, and telecom hardware use series-connected battery stacks. These stacks of individual cells may contain many units, potentially reaching hundreds of volts. In such systems, it is desirable to accurately determine each individual cell's voltage. Obtaining this information in the presence of the high common-mode voltage that the battery stack generates is more difficult than you might suppose.

The "battery-stack problem" has been around for a long time. Its deceptively simple appearance masks a stubborn problem. Designers have tried various approaches to isolated-cell-voltage measurement with varying degrees of success (see **sidebar** "Some battery-cell-measurement techniques just don't work" at the Web version of this article at www.edn.com/ms4255).

Figure 1's voltmeter measures a single-cell battery. Beyond the obvious benefits, the arrangement works because no voltages other than the single cell lie in the measurement path. The ground-referred voltmeter encounters only the voltage it is measuring.

Figure 2's stack of series-connected cells is more complex. The voltmeter must switch between the cells to determine each cell's voltage. Additionally, the voltmeter, normally composed of relatively low-voltage breakdown components, must withstand input voltages relative to its ground terminal. This common-mode voltage may reach hundreds of volts in large series-connected battery stacks, such as those in an automobile. Such high-voltage operation is beyond the voltage-breakdown capabilities of most practical semiconductor components, particularly if the application requires accurate measurement. The switches present similar problems. Attempts at implementing semiconductor-based switches encounter difficulty due to voltage-breakdown and leakage limitations. A practical method is necessary that would accurately extract individual cells' voltages and reject common-mode voltages. This method should not draw any battery current and should be simple and economical.

Figure 3's concept addresses these issues. To determine battery voltage, $V_{BATTERY}$, a pulse excites a transformer, T_1, and records its primary clamp voltage after settling occurs. The diode and the battery-voltage shunt primarily set this clamp voltage and similarly clamp T_1's secondary. The diode and a small transformer term are predictable errors, and the circuit's final stage substracts them out, leaving the battery voltage as the output.

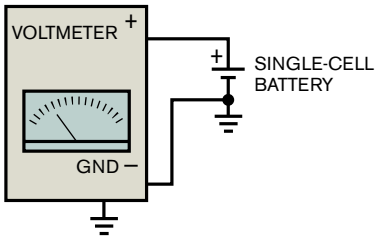

Figure 1 Common-mode voltage does not affect a voltmeter measuring a ground-referred single cell.

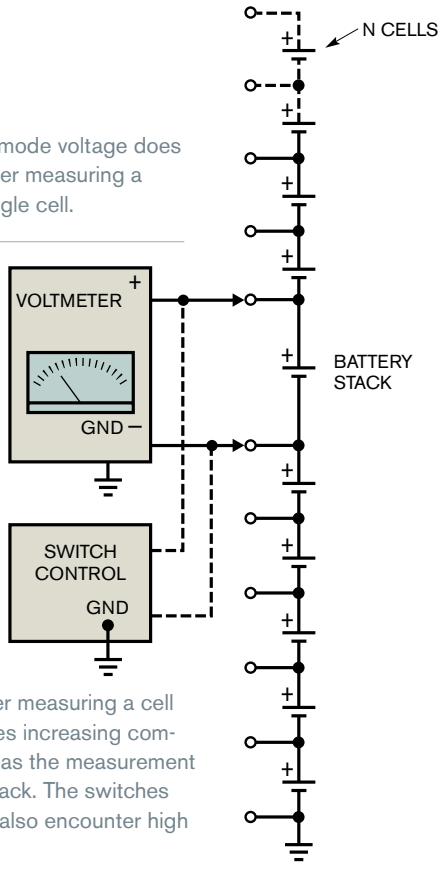

Figure 2 A voltmeter measuring a cell in a stack undergoes increasing common-mode voltage as the measurement proceeds up the stack. The switches and switch control also encounter high voltages.

DETAILED CIRCUIT OPERATION

Figure 4 details the transformer-based sampling voltmeter. It closely follows **Figure 3** with some minor differences, which

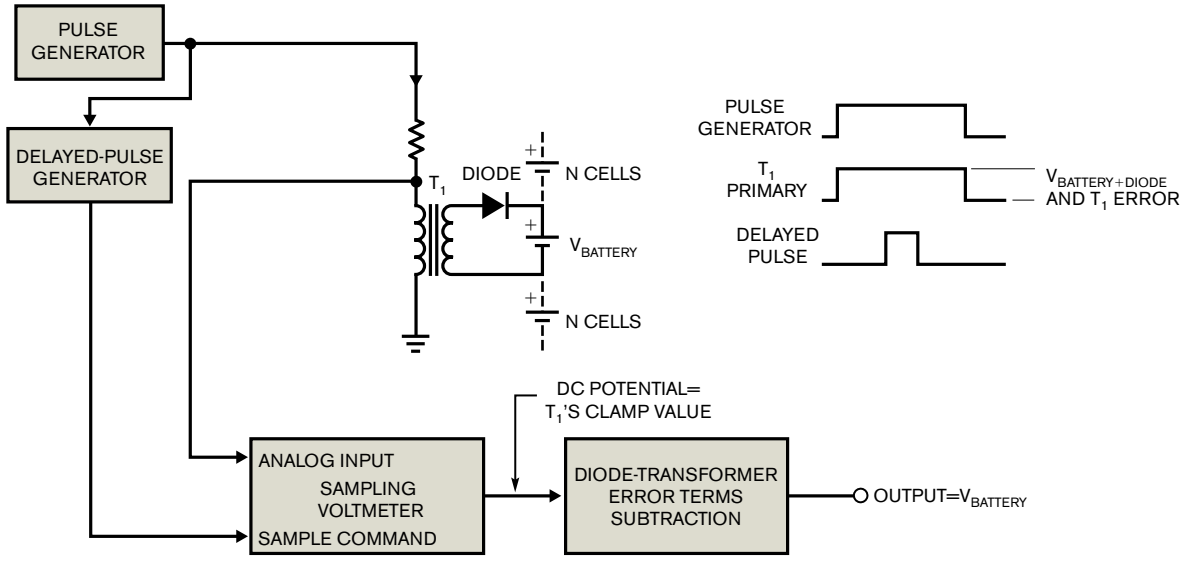

Figure 3 A transformer-based sampling voltmeter operates independently of high common-mode voltages. The pulse generator periodically activates T_1. The delayed pulse triggers a sampling voltmeter, capturing T_1's clamped value. Residual error terms are corrected in the following stage.

this article later describes. The pulse generator produces a 10-µsec-wide event (Trace A, **Figure 5**) at a 1-kHz repetition rate. The pulse generator's low-impedance output drives T_1 through a 10-kΩ resistor and triggers the delayed-pulse generator. T_1's primary, Trace B, responds by rising to a value representing the sum of the diode voltage and the battery voltage, along with a small fixed error that the transformer contributes. T_1's primary becomes clamped at this value. After a time, the delayed pulse, Trace C, generates a pulse, Trace D, closing S_1, allowing C_1 to charge toward T_1's clamped value. After a number of pulses, C_1 assumes a dc level identical to the voltage on T_1's clamped primary. A_1 buffers this potential and feeds differential amplifier A_2. A_2, operating at a gain near unity, subtracts the diode- and transformer-error terms, resulting in a direct reading of battery-voltage output.

Accuracy critically depends on transformer-clamping fidelity over temperature and clamp-voltage range. The carefully designed, specified transformer yields **Figure 6**'s waveforms. Primary, Trace A, and secondary, Trace B, clamping details appear at a highly expanded vertical scale. Clamping flatness is within millivolts; trace-center aberrations derive from S_1-gate feedthrough. Tight transformer-clamp coupling promotes good performance. Circuit accuracy at 25°C is 0.05% over a 0 to 2V battery range with 120 ppm/°C drift, degrading to 0.25% at a battery voltage of 3V. Designers of this circuit used a floating variable-potential battery (see **sidebar** "Floating-output, variable-potential battery simulator" at the Web version of this article at www.edn.com/ms4255).

Several details aid circuit operation. The circuit substitutes the transistor's base-emitter voltage for diodes, providing more consistent initial matching and temperature tracking. The 10-µF capacitor at Q_1 maintains low impedance at frequency, minimizing cell-voltage movement during the sampling interval. Finally, synchronously switched Q_2 prevents T_1's negative-recovery excursion from deleteriously influencing S_1's operation.

This approach's advantage is that its circuitry does not encounter high common-mode voltages; T_1 galvanically isolates the circuit from common-mode potentials associated with the battery voltage. Thus, you can employ conventional low-voltage techniques and semiconductors.

MULTICELL VERSION

The transformer-based method is inherently adaptable to the multicell-battery-stack-measurement problem. **Figure 7**'s conceptual schematic shows a multicell-monitoring version. Each channel monitors one cell. You can read any channel by biasing its appropriate enable line to turn on a FET switch, enabling that channel's transformer. The hardware for each channel typically includes only a transformer, a diode-connected transistor, and a FET switch.

AUTOMATIC CONTROL AND CALIBRATION

This scheme suits digital techniques for automatic calibration. **Figure 8** shows pulse generators, calibration channels, and measurement channels, which feed **Figure 9**'s PIC-16F876A microcontroller. As before, even though the cell stack may reach hundreds of volts, the transformer's galvanic isolation allows the signal-path components to operate at low voltage. The design includes an automatic calibration-circuit microcontroller and reset sections (**Figure 9**) and an automatic calibration-circuit USB interface for development only (**Figure 10**).

A further benefit of processor-driven operation is the elimination of **Figure 4**'s base-emitter-voltage diode-matching requirement. In practice, engineers tested a processor-based

board at room temperature with known voltages at all input terminals. They then read the channels, which furnished the information necessary for the processor to determine each channel's initial base-emitter voltage and gain. The engineers then stored these parameters in nonvolatile memory, permitting a one-time calibration that eliminates both base-emitter-voltage-mismatch- and gain-mismatch-induced errors.

Channels 6 and 7 provide 0 and 1.25V reference voltages, representing cell-voltage extremes. The room-temperature values reside in nonvolatile memory. As temperature changes occur, you use readings from channels 6 and 7 to calculate a change in offset and a change in gain that you apply to the six measurement channels. The calibration continues as temper-

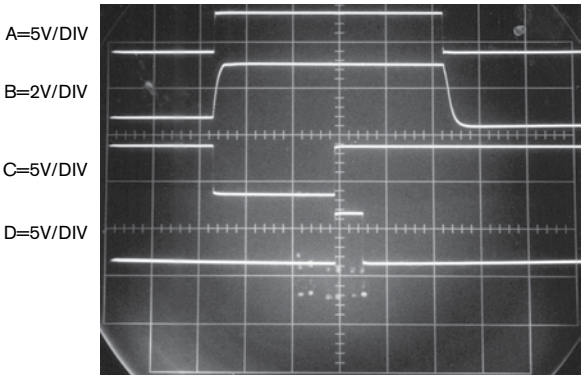

Figure 5 Figure 4's waveforms include the pulse-generator input (Trace A), the T_1 primary (Trace B), the 74HC123's $\overline{Q2}$ delay-time output (Trace C), and S_1's control input (Trace D). Timing ensures that sampling occurs when T_1 settles in the clamped state.

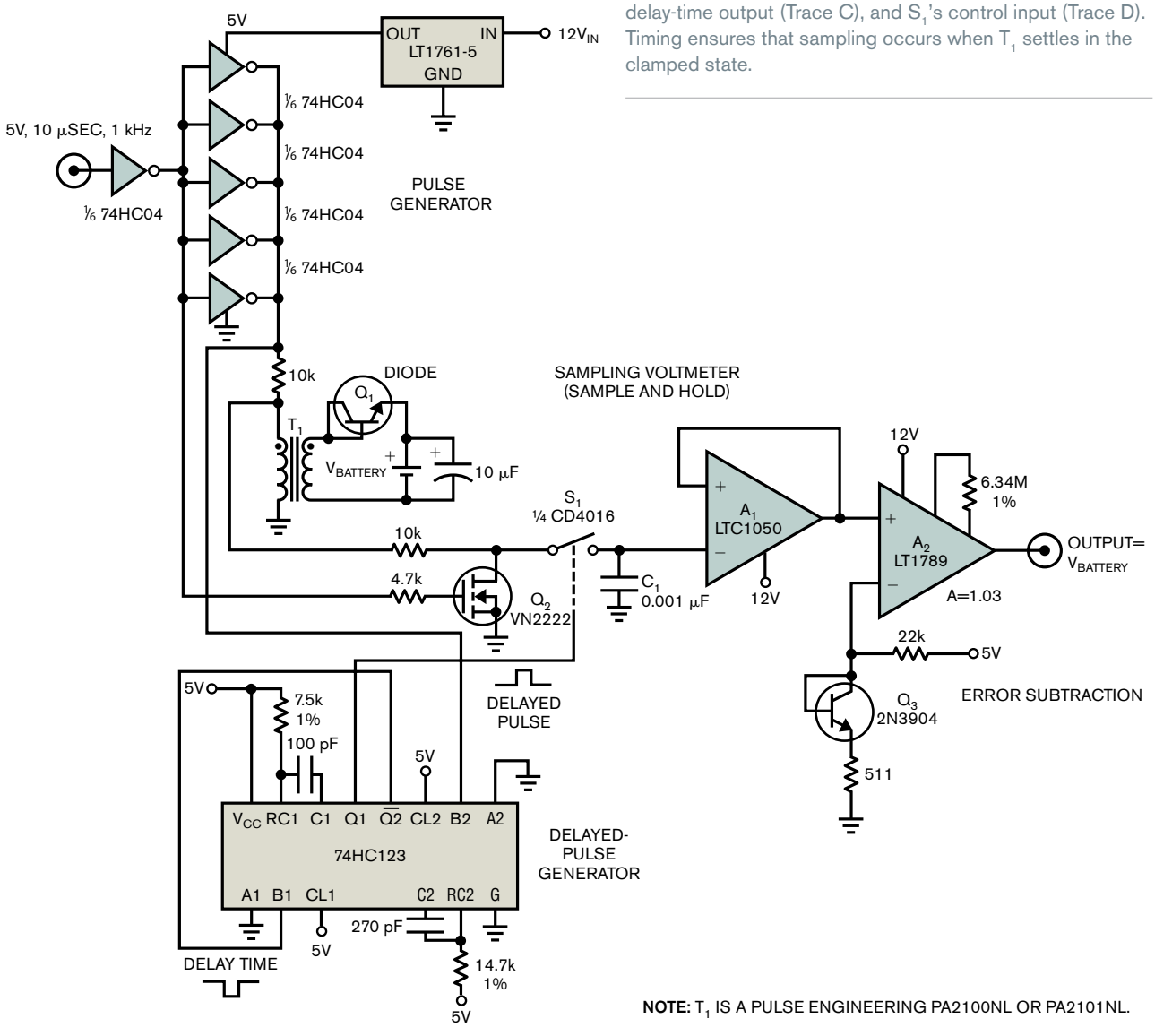

Figure 4 This transformer-fed sampling voltmeter closely follows Figure 3's concept. Error-subtraction terms include Q_3's compensation for Q_1 and resistor/gain corrections for errors in T_1's clamping action. Transistors Q_1, Q_2, and Q_3 replace diodes for more consistent matching. Q_2 prevents T_1's negative-recovery excursion from influencing S_1.

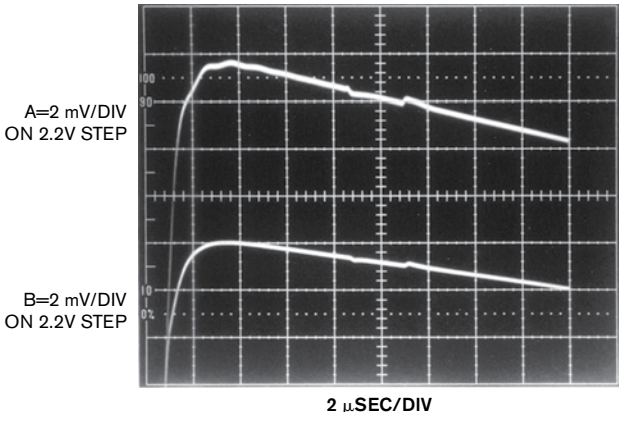

Figure 6 T_1's primary (Trace A) and secondary (Trace B) clamping details have a highly expanded vertical scale showing the primary's and secondary's clamping flatness to be within millivolts. The trace aberrations at the center derive from S_1's gate feedthrough.

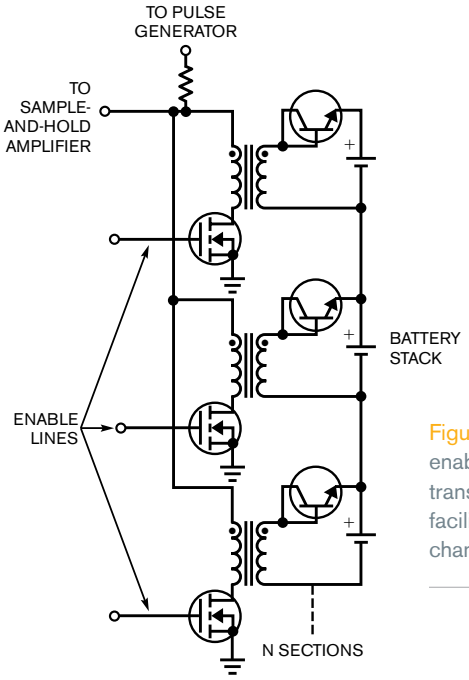

Figure 7 Adding enable lines and transistor switches facilitates multiple channels.

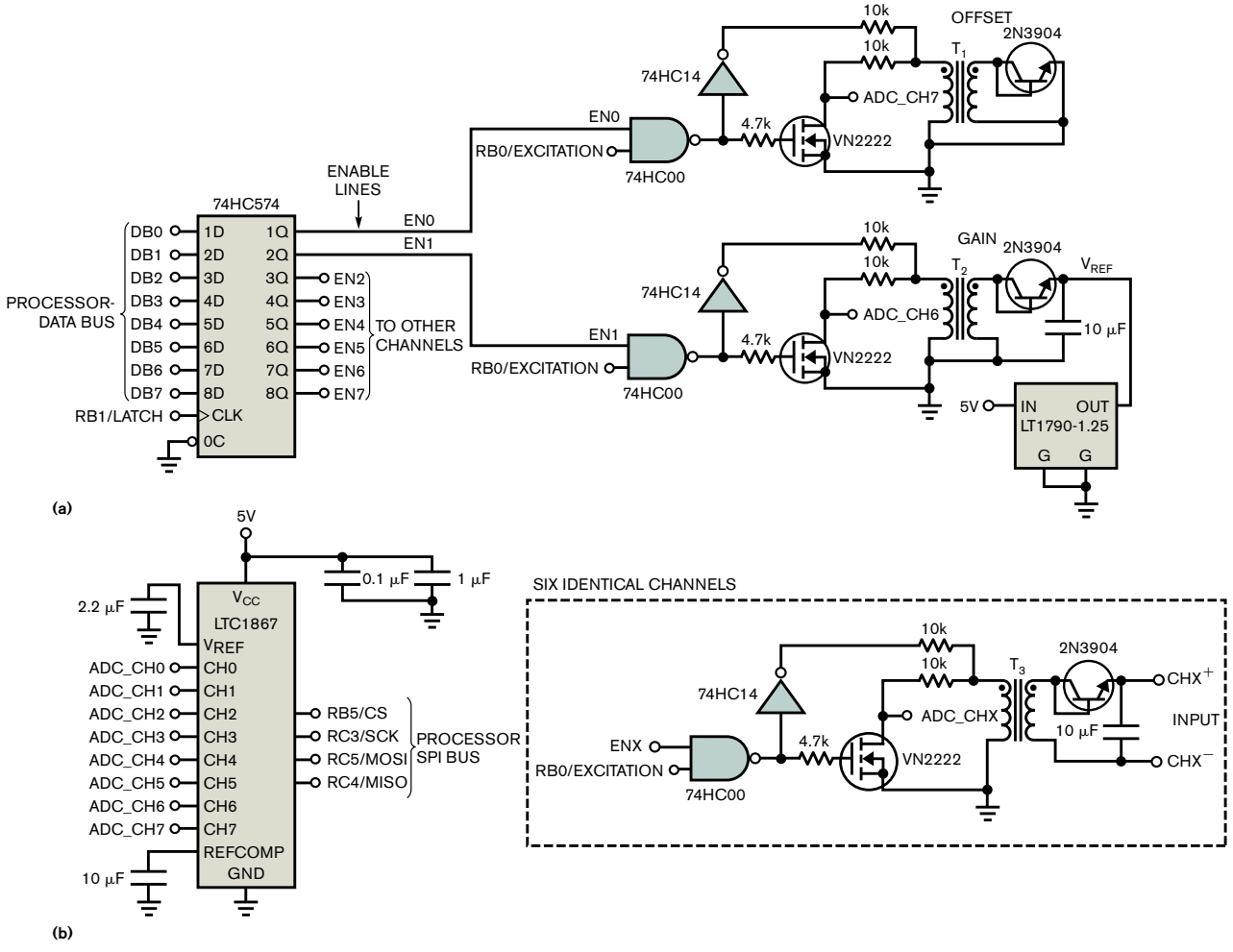

Figure 8 ADC-calibration channels eliminate base-emitter-voltage-matching requirements (a) and compensate for temperature-dependent errors (b).

ature varies because each channel's −2-mV/°C base-emitter-voltage-drift slopes are nearly identical. Similarly, gain errors from channel to channel are nearly identical.

Because you are continuously calibrating the gain and offset, the gain and offset of the LTC1867 drop out of the equation. The only points that must be accurate are the 1.25V reference voltage, which an LT1790-1.25 IC provides, and the 0V measurement, which is easy: Just short the Channel 6 inputs together. The LTC1867 internally amplifies its internal 2.5V reference to 4.096V at the reference-comparator pin, which sets the full scale of the ADC: 4.096V for unipolar mode and ±2.048V in bipolar mode. Thus, the absolute maximum cell voltage that you can measure is 3.396V. And, because the offset measurement is nominally 0.7V at the ADC input, it is never in danger of clamping at 0V. A 0V reading results if the LTC1867 has a negative offset and the input voltage is any positive voltage less than or equal to the offset. Accuracy of the processor-driven circuit is 1 mV over a 0 to 2V input range at 25°C. Drift drops to less than 50 ppm/°C—almost three times lower than that in in **Figure 4**.

The complete firmware code, **Listing 1**, is available with the Web version of this article at www.edn.com/ms4255. The code for this circuit is a good starting point for an actual product. Data appears on a PC screen through an FTDI (Future Technology Devices International, www.ftdichip.com) FT242B USB-interface IC. The PC has FTDI's virtual-communications-port drivers installed, allowing control through any terminal program. Data for all channels continuously appears on the terminal, and simple text commands control program operation.

A timer interrupt occurs 1000 times per second. It controls the pulse generators and ADC and stores the ADC readings in an array that you can read at any time. Thus, if the main program is reading the buffer, the most out of date any reading is is 1 msec.

The software also includes automatic calibration routines. Two functions store a zero reading and a full-scale reading for all channels, including the calibration voltages you apply to channels 6 and 7, to nonvolatile memory. You subsequently use these functions to calibrate out the initial gain and offset errors, as well as the temperature-dependent errors. The entire procedure is to apply 0V to all inputs and issue a command to

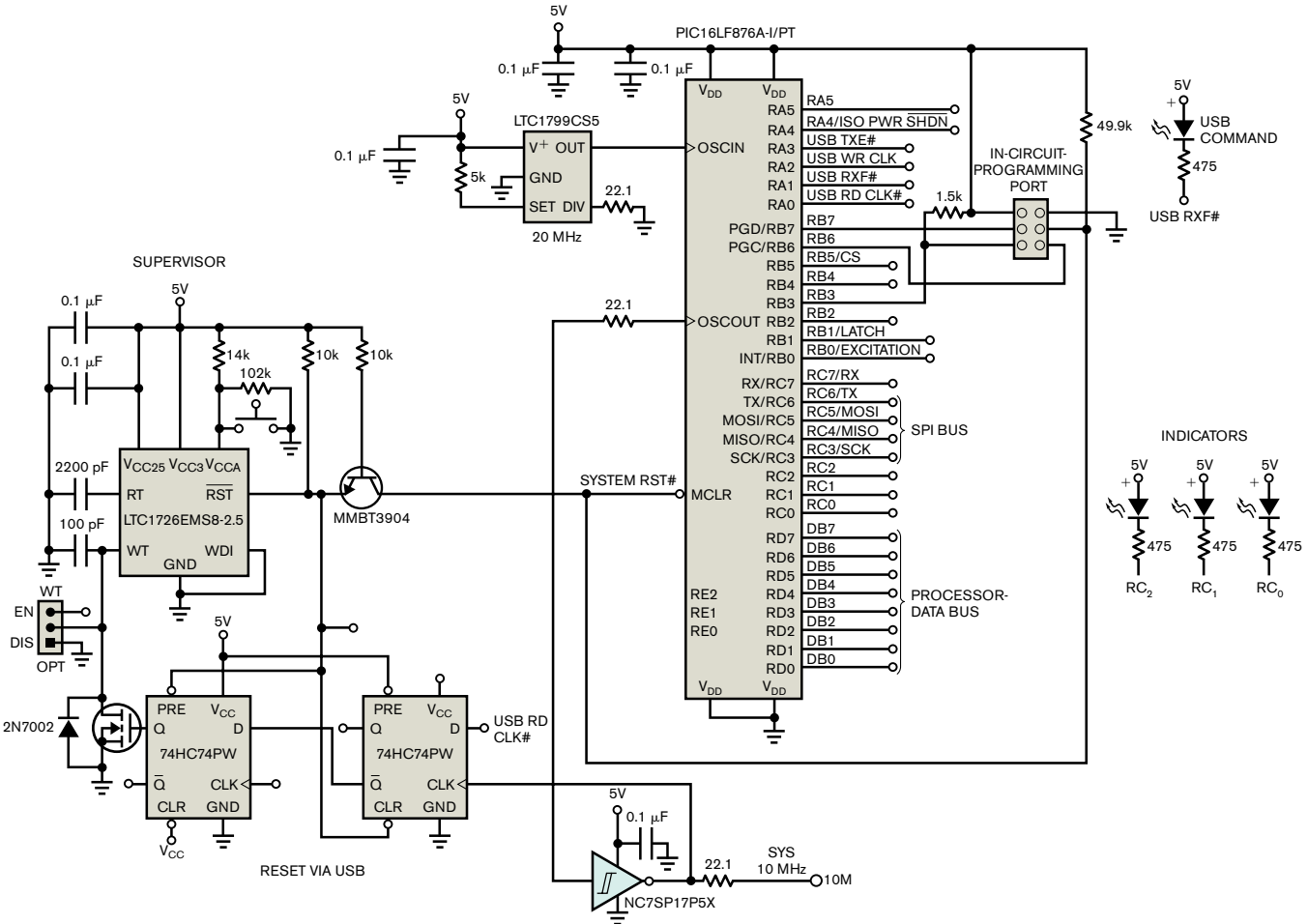

Figure 9 The design includes an automatic-calibration-circuit microcontroller and reset sections.

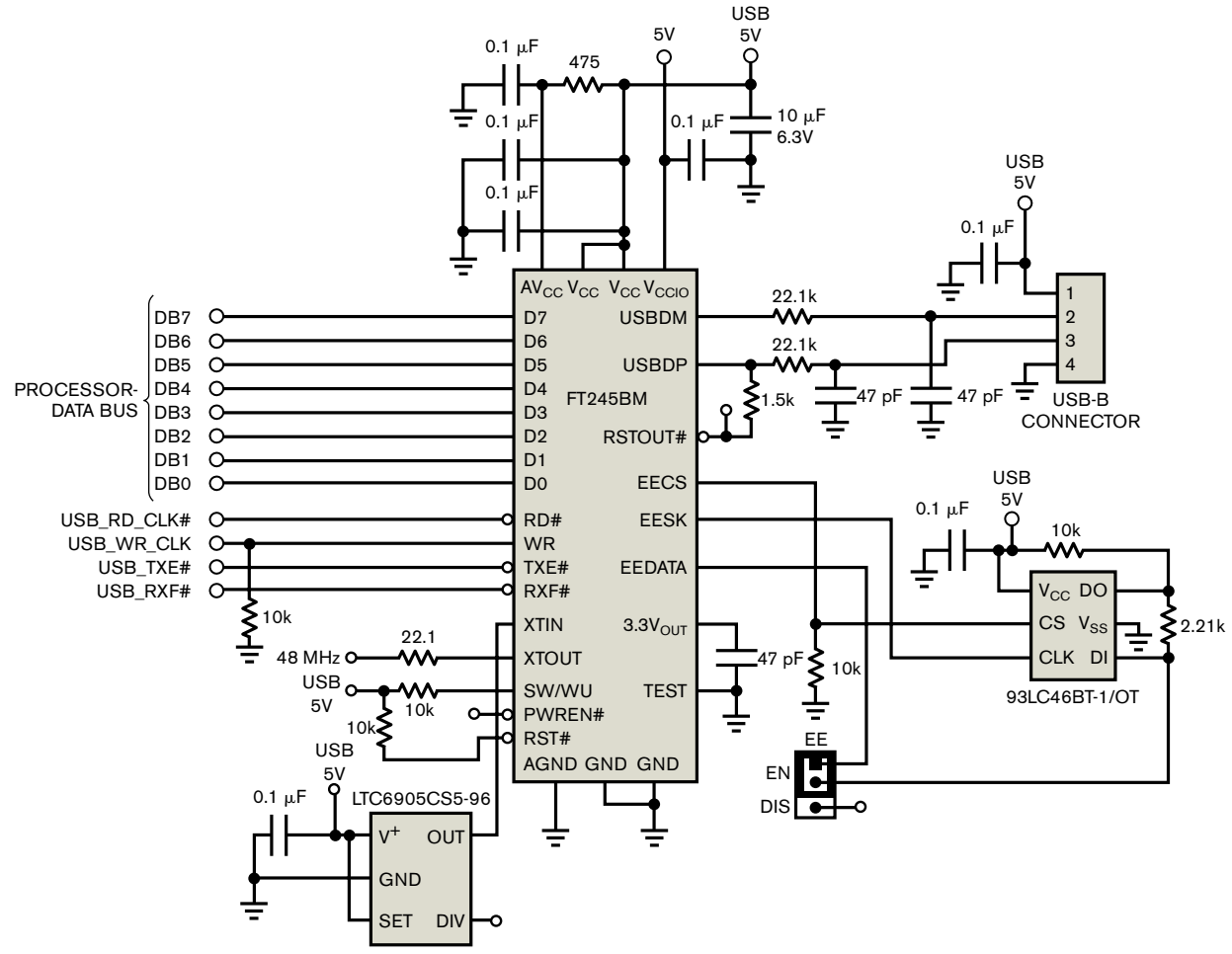

Figure 10 The design includes an automatic-calibration-circuit USB interface for development only.

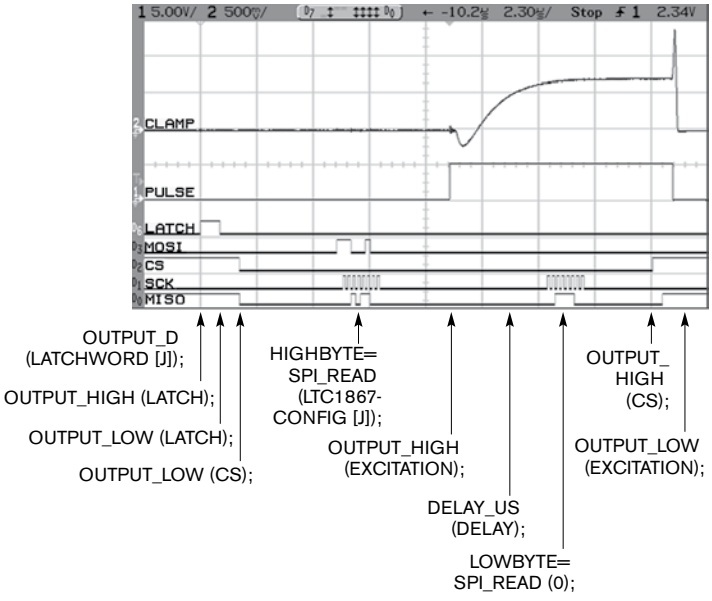

Figure 11 The interrupt-service routine monitors digital signals, excitation pulse, and clamp voltage at the ADC input along with the C code that performs these operations.

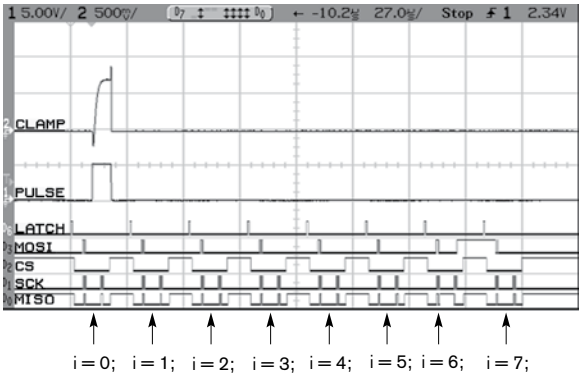

Figure 12 The interrupt-service routine scans eight channels.

store the zero calibration, then apply 1.25V to all inputs and issue a command to store the full-scale calibration. Note that this procedure is no more complicated than a basic performance test that would be part of any manufacturing process. The 1.25V factory-calibration source can be from a voltage calibrator or from a selected LT1790-1.25 that you keep at a stable temperature.

The software also includes a digital filter for testing purpos-

es. The filter is a simple exponential IIR (infinite-impulse-response) filter with a constant of 0.1. This filter reduces the noise in the readings by a factor of the square root of 10.

MEASUREMENT DETAILS

To take a reading from a given channel, the processor must apply the excitation to the transformer, wait for the voltage signal to settle out, take a reading with the ADC, and then remove the excitation. To perform these tasks, an interrupt-service routine occurs once every millisecond. For the details, see **Listing 1** at www.edn.com/ms4255. **Figure 11** shows the digital signals, excitation pulse, and clamp voltage at the ADC input along with the C code that performs these operations. Loading a 3-bit byte high into the 74HC574 latch enables individual channels.

Note that you apply the excitation after 8 bits of the LTC1867 data are read out. This situation is perfectly acceptable, because no conversion is taking place, and all of the data in the LTC1867 output register is static. Depending on the timing of the processor you use, you can apply excitation before reading any data, in the middle of reading data, or after reading the data but before initiating a conversion. If the serial clock is slow—1 MHz, for instance—applying excitation before reading any data would result in the excitation being applied for 16 µsec, which is too long. The only constraints are that the voltage at the ADC input must have enough time to settle properly and that you do not leave the excitation on for too long. **Figure 12** shows the same signals over the entire interrupt-service routine. Similar analog signals are at each transformer and the other LTC1867 inputs.

Many ways exist to add channels to this circuit. **Figure 13** shows a 64-channel concept that decodes the 64 channels in-

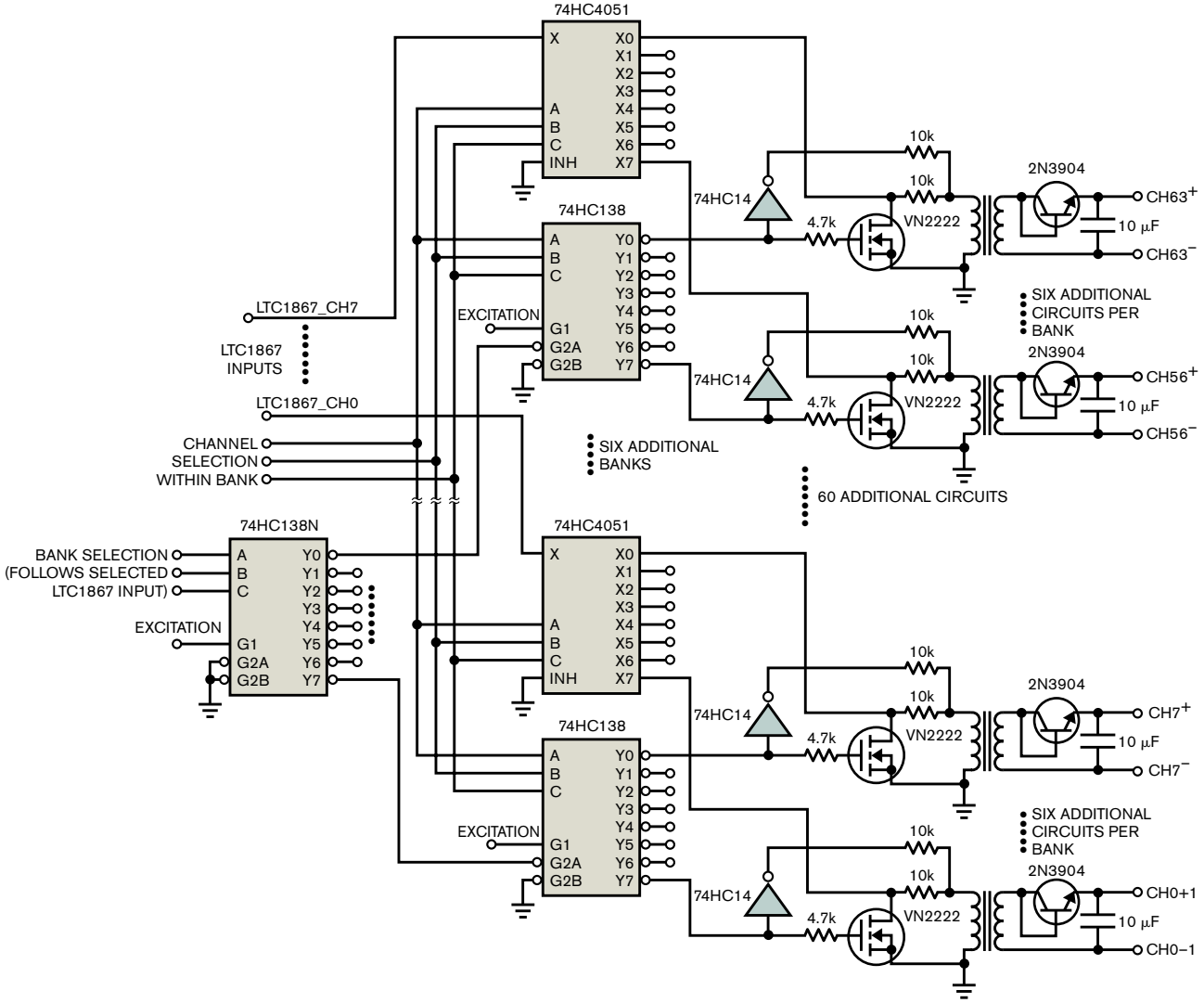

Figure 13 A 64-channel concept decodes the 64 channels into eight banks of eight channels using 74HC138 address decoders.

to eight banks of eight channels using 74HC138 address decoders. The selected bank corresponds to one LTC1867 input that is programmed through the SPI. Some 8-to-1 74HC4051 analog switches perform the additional analog multiplexing. A single 74HC4051 feeding each LTC1867 input gives 64 inputs. The LTC1867, rather than a single-channel ADC, is still a great choice in high-channel-count applications, because it is good idea to break up multiplexer trees into several stages to minimize total channel capacitance. The LTC1867 takes care of the last stage. With a maximum sample rate of 200k samples/sec, it can digitize as many as 200 channels at the maximum 1k-sample/sec limitation of the sense transformer. That's a lot of batteries. EDN

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FLOATING-OUTPUT, VARIABLE-POTENTIAL BATTERY SIMULATOR

A floating-output, variable-potential battery simulator can help in the development of a battery-stack-voltage monitor. This capability permits accuracy verification over a wide range of battery voltage. You can substitute a floating battery simulator for a cell in the stack and directly dial out any desired voltage. Figure A's circuit is simply a battery-powered follower, A_1, with current-boosted output at A_2. The specified LT1021 reference and high-resolution potentiometric divider permit accurate output settling within 1 mV. The composite amplifier unloads the divider and drives a 680-μF capacitor to approximate a battery. Diodes preclude reverse-biasing the output capacitor during supply sequencing, and the 1-μF-capacitor/150-kΩ-resistor combination provides stable loop compensation. Figure B depicts loop response to an input step; no overshoot or untoward dynamics occur despite A_2's huge capacitive load. Figure C shows battery-simulator response (Trace B) to Trace A's transformer clamp pulse. Closed-loop control and the 680-μF capacitor limit simulator-output excursion within 30 μV. This error is so small that it requires noise-averaging techniques and a high-gain-oscilloscope preamplifier to resolve it.

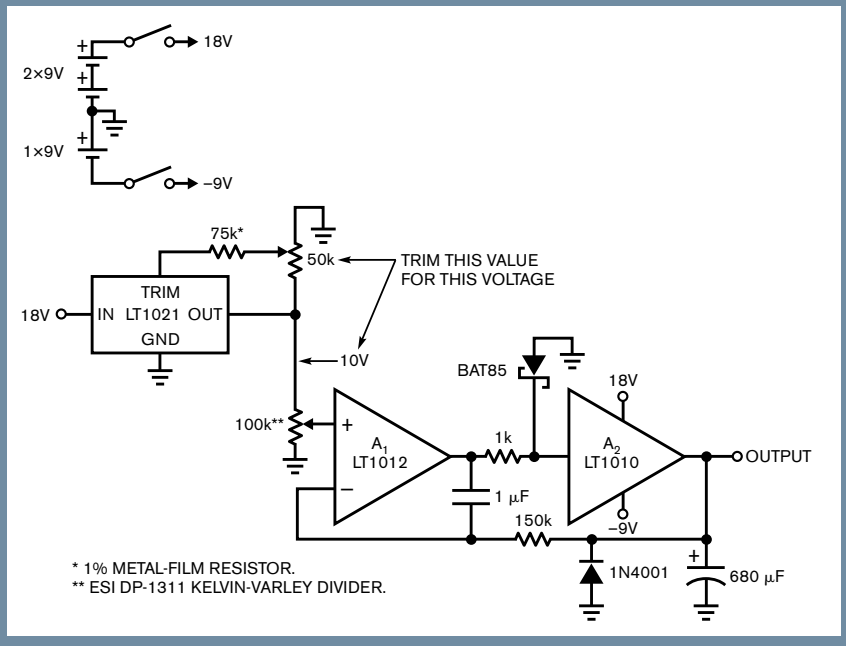

Figure A This battery simulator has a floating output settable within 1 mV. A_1 unloads the Kelvin-Varley divider, and A_2 buffers the capacitive load.

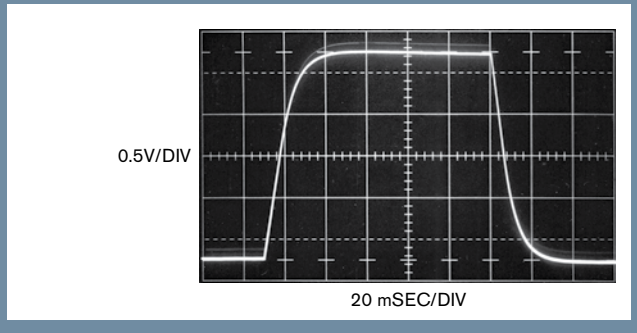

Figure B The 150-kΩ-resistor/1-μF-capacitor compensation network provides clean response despite a 680-μF output capacitor.

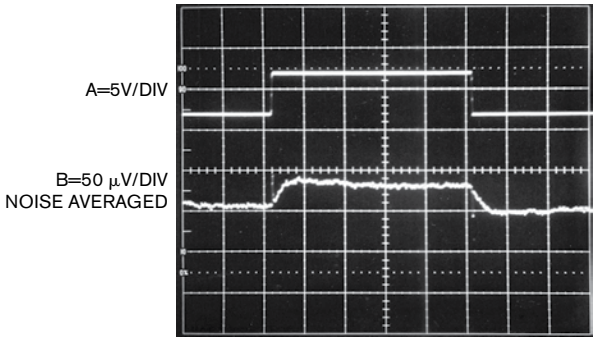

Figure C The battery-simulator output (Trace B) responds to Trace A's transformer-clamp pulse. Closed-loop control and the 680-μF capacitor maintain the simulator output within 30 μV. A noise-averaged, 50-μV/division sensitivity is necessary to resolve a response.

SOME BATTERY-CELL-MEASUREMENT TECHNIQUES JUST DON'T WORK

The so-called battery-stack problem has been around for a long time. Designers have tried various approaches with varying degrees of success to solve it. The problem appears deceptively simple; technically and economically qualified approaches are notably elusive. The following paragraphs present typical candidates and their difficulties.

Figure A presumably solves the problem by converting cell potentials to current, obviating the high common-mode voltages. Op amps feed a multiplexed-input ADC; the decoded ADC output presents cell voltages. This approach has serious flaws. First, the required resistor precision and values are unrealistic, and they become progressively more unrealistic as the number of cells in the stack increases. Additionally, the resistors drain current from the cells, a distinct and often unallowable disadvantage.

Figure B shows an isolation-amplifier-based approach. Isolation amplifiers feature galvanically floating

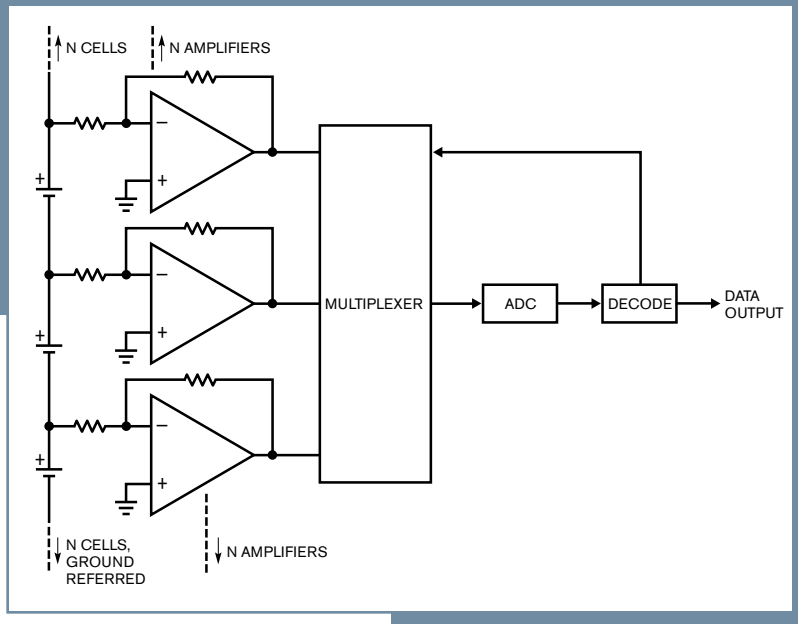

Figure A This unworkable scheme suppresses high common-mode voltages by converting cell potentials to current. The circuit decodes amplifier outputs to derive individual cell voltages. The required resistor precision and values are unrealistic. In addition, the resistors draw current from the cells.

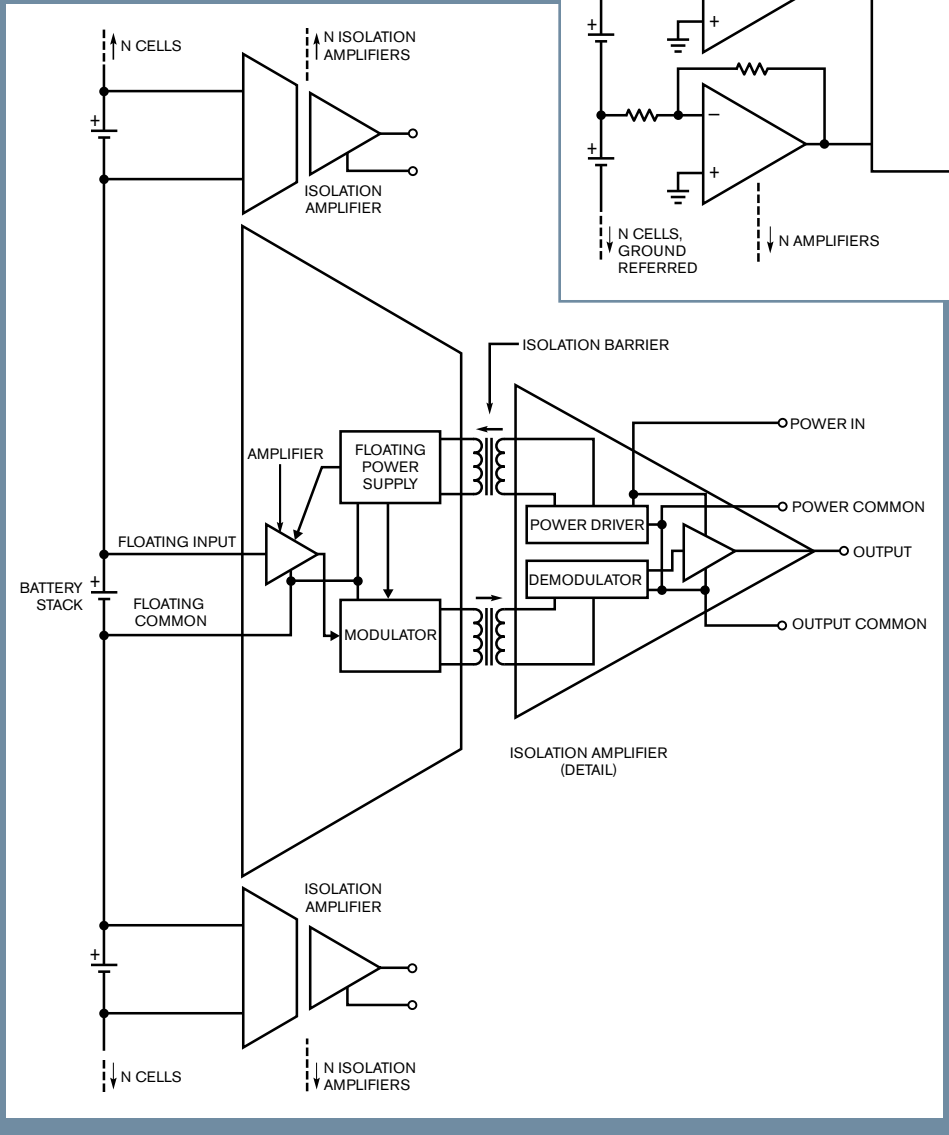

Figure B This isolation amplifier's galvanically floating input eliminates common-mode-voltage effects. The approach works, but it is complex and expensive, requiring one isolation amplifier for each cell.

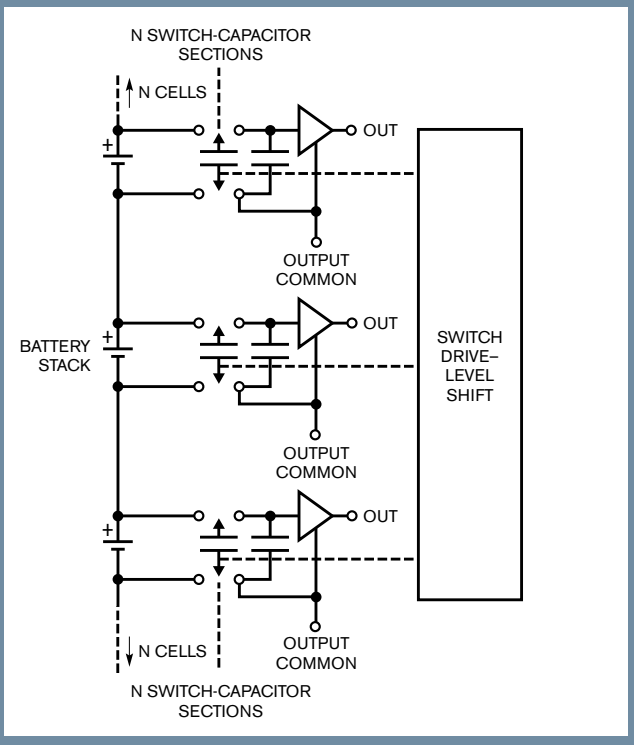

Figure C This switched-capacitor scheme rejects common-mode voltage but requires high-voltage switches, nonoverlapping drive, and a level shift. The switch leakage degrades accuracy. Optically driven switches can simplify the level shift, but breakdown and leakage issues remain.

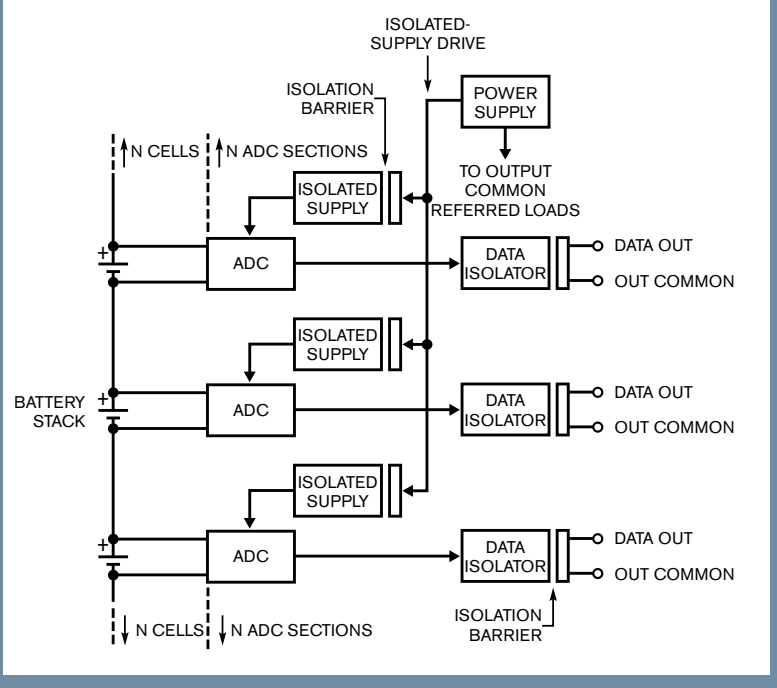

Figure D An ADC per cell requires isolated supplies and data isolators. Multiplexed-input ADCs can minimize ADC usage. You can reduce but not eliminate the isolated-supply population.

inputs that are fully isolated from their output terminals. Typically, the device contains modulation/demodulation circuitry and a floating supply that powers the signal-input section. The amplifier inputs monitor the cell; its isolation barrier prevents battery-stack common-mode voltage from corrupting output-referred measurement results. This approach works well, but the need for one isolation amplifier per cell is complex and expensive. You can simplify this approach by, for example, using one power driver to service many amplifiers, but the method remains costly and involved.

Figure C employs a switched-capacitor technique to measure each cell's voltage and reject common-mode voltage. The clocked switches alternately connect the capacitor across its associated cell and discharge it into an output common-referred capacitor. Old-timers will recognize this configuration as a derivative of the venerable reed-switched "flying-capacitor" multiplexer. After a number of cycles, the output capacitor assumes the cell voltage. A buffer amplifier provides the output. This arrangement rejects common-mode voltages but requires many expensive, high-voltage switches; a high-voltage level shift; and nonoverlapping switch drive. More subtly, switch leakage degrades accuracy, particularly as temperature rises. Optically driven switches, particularly those available as conveniently packaged LED-driven MOSFETs, can simplify the level shift, but expense, voltage-breakdown, and leakage concerns remain.

Figure D's approach eliminates switch-related disadvantages. A dedicated ADC digitizes each cell's potential. The ADC output transmits across an isolation barrier through a data isolator, such as an optical transformer. In its most elementary form, a separate isolated power supply powers each ADC. You can reduce but not eliminate the isolated-supply population. Constraints include cell voltage and the ADC's maximum permissible supply and input-common-mode voltages. Within these limitations, one isolated supply can service several ADC channels. You can further refine the setup by employing multiplexed-input ADCs. Even with these improvements, large battery stacks mandate the use of numerous isolated supplies. Although this scheme is technologically sound, it is complex and expensive.

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AND FRAN GRANVILLE

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READERS SOLVE DESIGN PROBLEMS

JFET-based dc/dc converter operates from 300-mV supply

Jim Williams, Linear Technology Corp, Milpitas, CA

You use a JFET's self-biasing characteristics to build a dc/dc converter that operates from power sources such as solar cells, thermopiles, and single-stage fuel cells, all of which deliver less than 600 mV and sometimes as little as 300 mV. Figure 1 shows the drain-to-source characteristics of an N-channel JFET under zero-bias conditions, which you can produce by connecting its gate and source together. Applying 100 mV causes a current of 10 mA to flow through the device, increasing to 30 mA at 350 mV. Exploiting the JFET's ability to conduct significant current at zero bias makes it possible to design a self-starting, low-input-voltage converter.

The circuit can supply 5V at currents as large as 2 mA—enough to serve many micropowered applications or to provide auxiliary bias for a higher power switched-mode voltage regulator. At 300-mV input, the circuit starts up at load currents of 300 µA. A load current of 2 mA requires an input of 475 mV.

In Figure 2, Q_1, a parallel-connected pair of Philips Semiconductor's (www.semiconductors.philips.com) BF862 JFETs, and Coiltronics' (www.coiltronics.com) Versa-Pac transformer, T_1, form an oscillator in which T_1's secondary winding provides feedback to Q_1's gate. When you first apply power, Q_1's gate rests at 0V, and drain current flows through T_1's primary winding. T_1's phase-inverted secondary winding responds by delivering a negative voltage to Q_1's gate, which turns off Q_1 and interrupts current flow through T_1's primary winding. In turn, T_1's secondary voltage collapses, and sustained oscillations begin. Although the BF862's published specifications do not cover the device's internal geometry, the device has a low on-resistance and maintains a low gate-turn-on threshold voltage. Using a pair of parallel-connected JFETs for Q_1 ensures the low saturation voltage for operation at low power-supply voltages.

Rectifying and filtering the positive-going flyback-voltage impulses on Q_1's drain produce a dc voltage across capacitor C_1. To assist the circuit's start-up, a P-channel MOSFET, Q_2, which requires a gate-to-source voltage of approximately 2V for conduction, initially isolates the output load from the rectifier. When Q_2 conducts, the output voltage increases toward 5V. Comparator IC_1, a Linear Technology (www.linear.com) LTC-1440, draws power from Q_2's source and imposes output-voltage regulation by comparing its internal voltage reference with a sample of the output voltage. The output

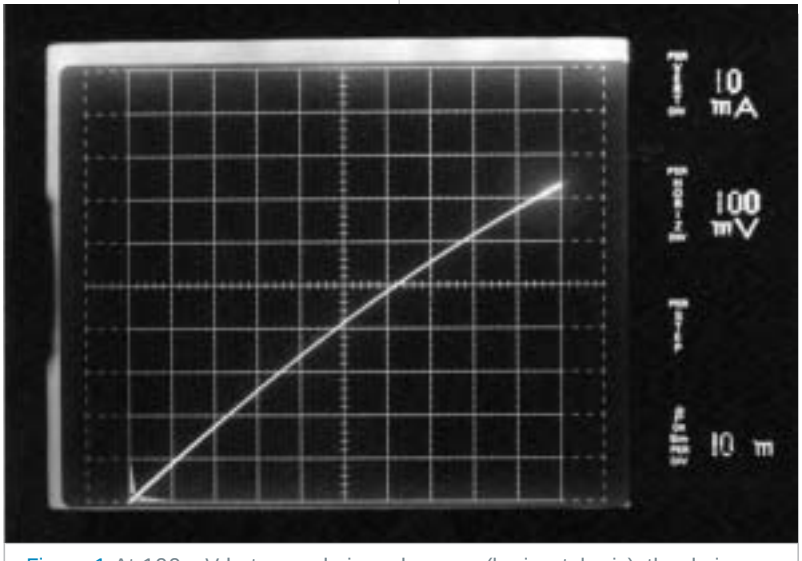

Figure 1 At 100 mV between drain and source (horizontal axis), the drain current reaches 10 mA (vertical axis) and increases to 30 mA at 300 mV.

DIs Inside

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from IC_1 varies Q_1's on-time through Q_3 to close the control loop and maintain output-voltage regulation. Figure 3 shows the ripple voltage present at the power supply's output. When the output voltage decays, comparator IC_1 switches (Trace B, middle) and allows Q_1 to oscillate. The resulting flyback events at Q_1's drain (Trace C, bottom) restore the output voltage.

Using Q_3 as a simple but effective shunt control for Q_1's gate voltage results in a 25-mA quiescent-current drain from the power source. A modification reduces the quiescent drain to 1 mA (Figure 4). Inserting switch Q_4 in series with T_1's secondary winding more efficiently controls Q_1's gate. Bootstrapping the voltage across T_1's secondary winding produces negative-turn-off-bias voltage for Q_4. Figure 5 illustrates how to connect T_1's wind-

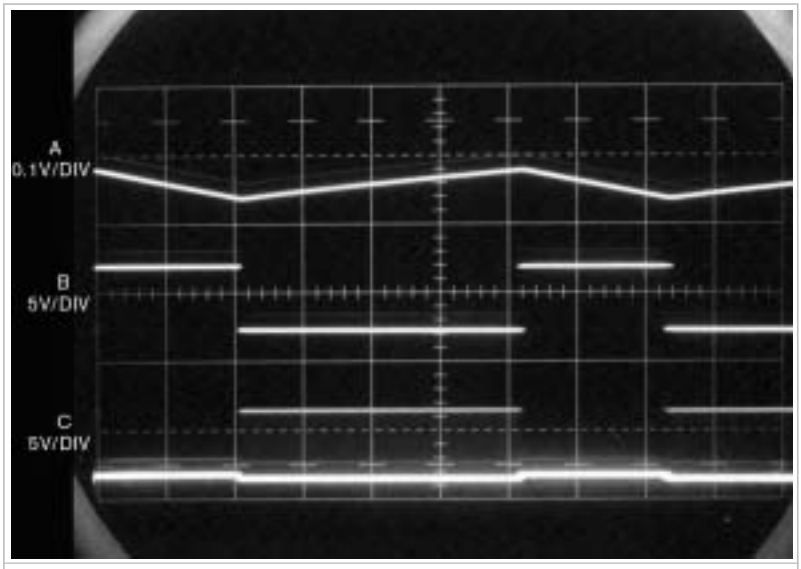
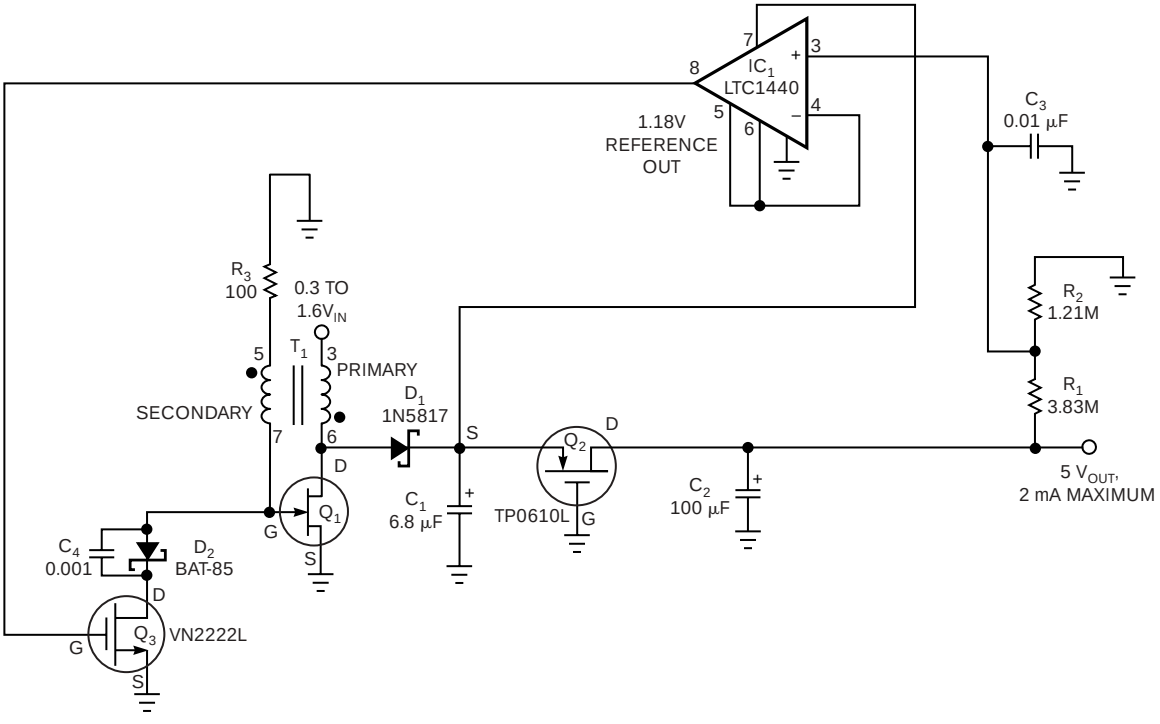


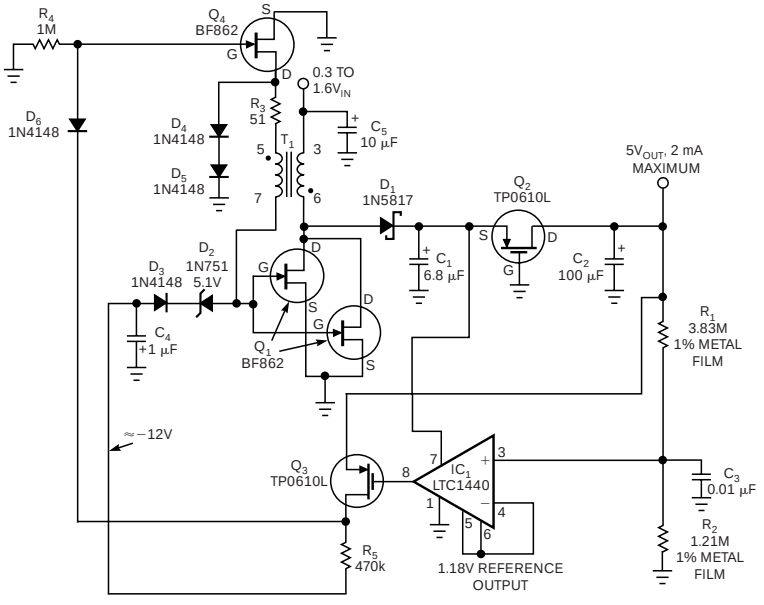
Figure 3 The dc output (Trace A), comparator IC_1's output, and the voltage at Q_1's drain (Trace C) have a horizontal-deflection factor of 5 msec.



NOTES:
1. USE ±1%-TOLERANCE METAL-FILM RESISTORS FOR R_1 AND R_2.
2. CONNECT T_1 AS SHOWN IN FIGURE 5.
3. Q_1 COMPRISES PHILIPS BF862 JFETs CONNECTED IN PARALLEL.

Figure 2 A pair of parallel-connected JFETs allows this dc/dc converter to operate from power sources that supply as little as 300 mV.

ings. When Q_4 switches off, it interrupts the current flowing in T_1's secondary winding and drives T_1's Pin 5 positive. Without diodes D_4 and D_5, the peak voltage would approach 15V and reverse-bias Q_4, an undesirable condition. Under normal operating conditions, excursions of approximately 0.8V appear at Pin 5, necessitating the use of two series-connected diodes to clamp the voltage at a safe level. Zener diode D_3 holds off bias-supply loading to aid start-up during initial power application. EDN



NOTES:
1. USE ±1%-TOLERANCE METAL-FILM RESISTORS FOR R_1 AND R_2.
2. CONNECT T_1 AS SHOWN IN FIGURE 5.
3. Q_1 COMPRISES PHILIPS BF862 JFETs CONNECTED IN PARALLEL.
4. T_1 = COILTRONICS VP1-1400.

Figure 4 Adding Q_3, Q_4, and the bootstrapped negative-bias generator comprising D_2, D_3, and C_4 reduces the circuit's quiescent current from 25 mA to 1 mA.

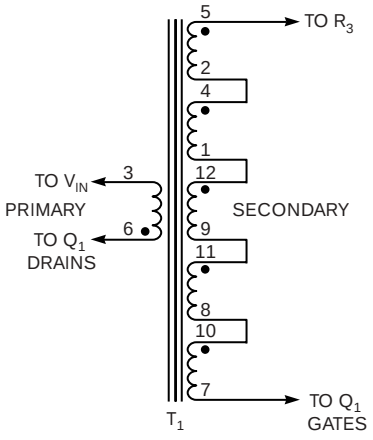


Figure 5 Comprising six independent windings that offer more than 500 configurations, Coiltronics' VP1-1400 serves as a combination feedback and flyback transformer in this application. Connect the windings as shown.

Configurable logic gates' Schmitt inputs make versatile monostables

Glenn Chenier, Allen, TX

You can assemble a pulse-generation circuit from a simple Schmitt-input AND gate plus a resistor-capacitor timing network. However, if you need a logic function that's not a standard catalog item, you need a Schmitt-input gate or inverter and an additional logic gate. Drawing from an earlier Design Idea (Reference 1) and a recent design requirement for adding pulse-generation functions to a crowded pc board, I searched Fairchild Semiconductor's Web site (www.fairchildsemi.com) for small-footprint Schmitt-input logic gates and found only "old faithfuls"—familiar Schmitt-input AND gates and Schmitt buffers.

Disappointed, I investigated other logic offerings from Fairchild and stumbled across a section of the Web site that describes "configurable logic gates." Lo and behold, I suddenly realized I was looking at the solution to my problem. The NC7SZ57 and NC7SZ58 (Reference 2) comprise tiny, six-pin surface-mount packages that you can configure as inverters or as AND, OR, or XOR gates, all of which allow the inversion of one input. These devices feature inverted outputs, overvoltage-input tolerance, and high current drive.

Every input has hysteresis, making these devices ideal for timed pulse generation. A design that combines digital logic with analog interfaces often requires timed pulses and delays, along with pulse shorteners and stretchers. For applications in which exact pulse times are not critical, the added feature of Schmitt inputs allows the delay of one input using an RC (resistance-capacitance) timing network. When the slowly changing RC circuit's output crosses the analog-level upper- or lower-trip-point thresholds, the Schmitt feature converts the slowly rising and falling voltages to fast digital edges.

Texas Instruments (www.ti.com)

offers functional equivalents—the SN74LVC1G57 and SN74LVC1G58 (Reference 3). Both companies' devices offer upper- and lower-trip-point-voltage thresholds averaging 37 and 63%, respectively, of V_{CC}, or approximately one RC time constant on the rising or the falling edges. According to the published data sheets from the manufacturers' Web sites, Texas Instruments' versions impose somewhat tighter tolerances on the analog threshold levels and thus deliver tighter timing tolerances than do the Fairchild parts.

For digital-analysis purposes, any voltage below the upper trip point for a rising edge effectively represents a logic zero, and any voltage above the lower trip point for a falling edge represents a logic one. These conditions are true only after the input crosses a respective trip point, such as a rising edge that approaches but never crosses the upper trip point. This voltage remains a logic zero, even if the voltage then drops back to ground potential on its falling edge.

Figure 1a shows some typical circuit implementations. Note that these circuits lack some of the niceties of genuine monostables. For example, a circuit doesn't retrigger until after its RC network has stabilized or about five time constants have elapsed. The RC time constant must be five times shorter than the time between triggering events. Devices from the SN74LVC1G57 family produce the waveforms in Figure 1b, and circuits using the SN74LVC1G58-family devices produce the inverse of these waveforms. The circuits' operation is straightforward. The RC circuits delay one input, so that the inputs momentarily rest at opposite states. When one RC time constant elapses, the delayed voltage crosses the Schmitt upper- or lower-trip-point thresholds, and the delayed input catches up to the straight-through input.

Of unusual interest and unlike the usual variety of monostable that triggers only from a voltage transition in one direction, the XOR implementation functions as a monostable triggered by both the rising and the falling edges, enabling it to function as a frequency doubler for generating strobe pulses on rising and falling clock edges. You can make any inverting-gate configuration into an oscillator by feeding back its inverted output to an RC-delayed Schmitt input and enabling the gate's remaining input. However, once the XOR oscillator's remaining gate switches off the oscillation, the gate's output state hangs at either a one or a zero to produce a truly random state derived from the oscillation's nonsynchronous relationship to the timing of the disabling input. EDN

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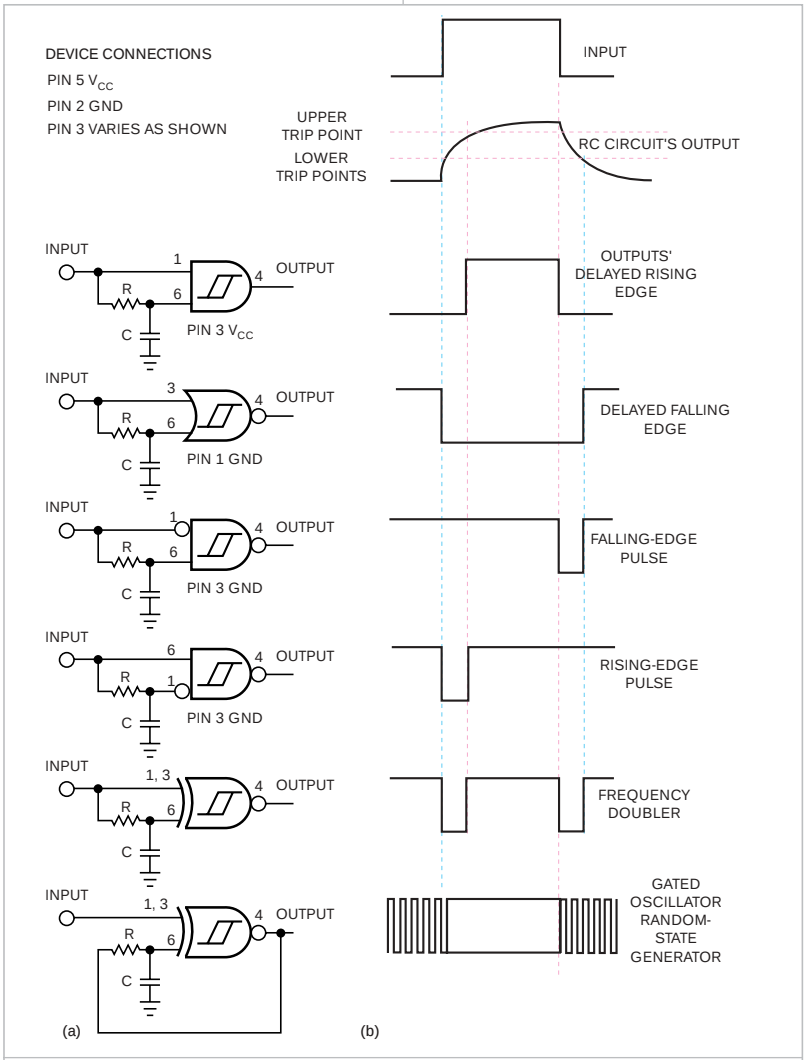


Figure 1 One gate plus an RC network (a) can deliver a range of useful timed outputs (b).

Stealth-mode LED controls itself

Howard Myers, Greensboro, NC

Since the LED's invention more than 30 years ago, its emission efficiency has steadily increased, and, although it may surprise you, the increased conversion efficiency works in two directions. Certain bright, efficient LEDs, such as Hewlett-Packard's (www.hp.com) HLMP-EG30-NR000, a red emitter molded in clear encapsulation, also exhibit significant photovoltaic action. The circuit in Figure 1 shows how you can put an LED's photovoltaic characteristics to work. Using the same components, older, red LEDs also function but with lower light output in this circuit. This Design Idea circuit describes an LED that controls itself by determining whether it's on or off without the assistance of any light sensor other than its own characteristics. When you darken the LED, it turns on, and, when you illuminate it, it turns off. The circuit's main components comprise LED D_1, micropower operational amplifier IC_1, one-shot IC_{2A}, and transistor switch Q_1 to control current through the LED.

When dark, the LED produces no photovoltaic current. When moderate lighting, such as that in an office or a lab, illuminates it, it generates 50 to 100 mV into a 4.7-MΩ load resistor. Comparator op amp IC_1 compares the voltage that the LED produces with a threshold reference voltage of approximately 50 mV. You can vary the circuit's sensitivity threshold by altering the values of resistors R_1 and R_2 in the voltage divider that connects to IC_1's Pin 2.

When ambient light decreases, the LED produces less voltage, and, when the voltage falls below the 50-mV threshold, the op amp's output goes low and triggers one-shot IC_{2A}. The one-shot turns on transistor Q_1 for an interval, lighting the LED for approximately 3 msec until the one-shot's output goes low. In a darkened room, the cycle repeats at a 200-Hz rate, and the LED blinks repeatedly with short off periods. At high flash rates, the LED appears to be continuously on.

The circuit's current drain in the daylight state mainly comprises the current driving the reference-bias network: 3.6V/162 kΩ=22 μA. In both day and night modes, with the LED drawing a few milliamperes when illuminated, a battery that can deliver 1 Ahr would power the circuit for a couple of months. You can reduce the current by increasing the values of R_1 and R_2. Given the circuit's low and intermittent current drain in a well-lighted environment, a 1-Ahr lithium cell's service life should approach its shelf life. EDN

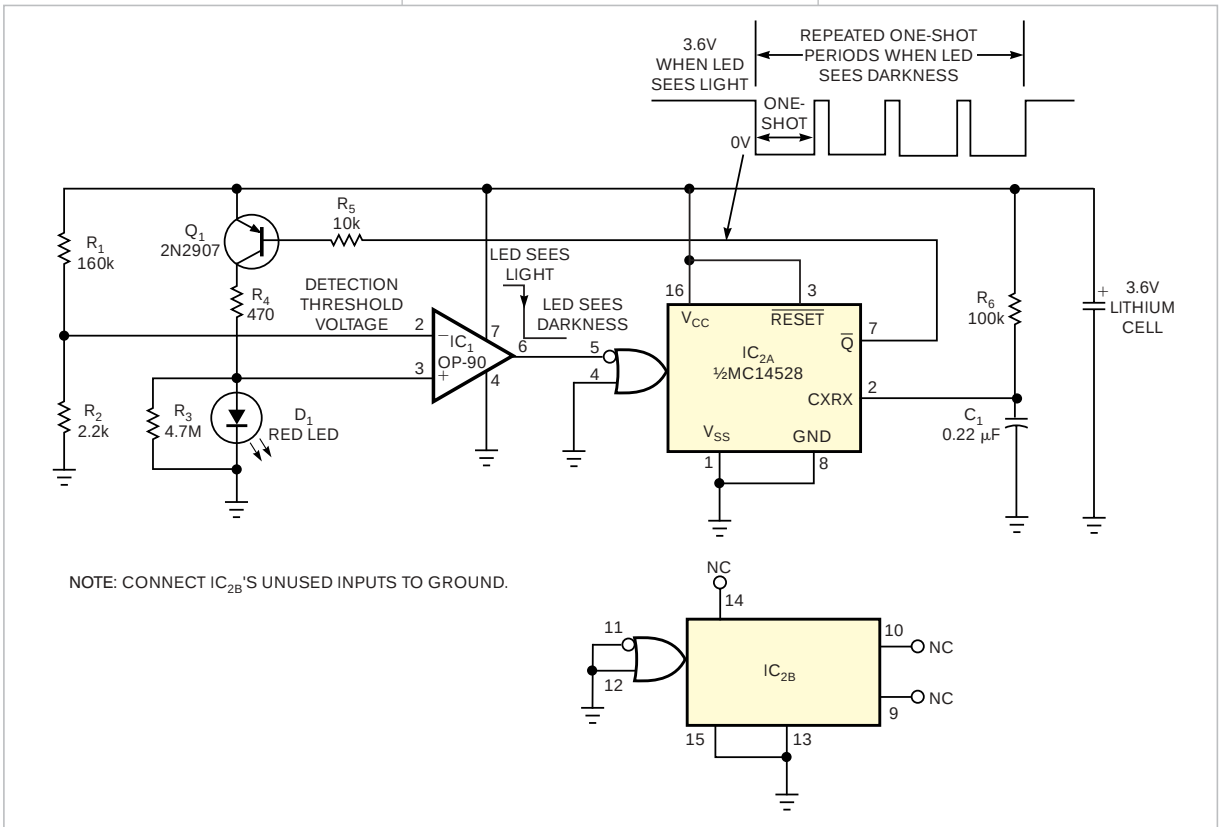


Figure 1 An efficient LED forms the heart of a light-sensitive "mystery lamp" that contains no apparent photodetector.

Data-acquisition system captures 16-bit voltage measurements using the USB

Terry Millward, Maxim Integrated Products Inc, Bionay, Switzerland

The USB has become the interface of choice for connecting to PCs. Available on all relatively modern PCs, the USB offers a standard connector and can supply power to peripherals at 5V and as much as 100 mA of current. The circuit in Figure 1 combines Maxim's (www.maxim-ic.com) MAX1168, a low-power, 16-bit ADC, with a small USB-interface module to make a simple, eight-channel, 16-bit measurement system. The MAX1168 includes eight input channels, an SPI (serial-peripheral-interface) port, a 4.096V reference, and a clock oscillator. The MAX1168 operates from a 5V supply and can convert individual channels, execute multiple conversions on one channel, or scan the channels sequentially and store measured data on-chip.

Based on a Cypress (www.cypress.com) CY7C63743 controller, USBmicro's (www.usbmicro.com) U421 USB-interface module provides as many as 16 I/O lines and an option to use some of those lines as an SPI port at selectable clock rates of 62.5 kHz, 500 kHz, 1 MHz, or 2 MHz. Firmware on the U421 allows generic access to SPI read-and-write devices, and the device's general-purpose I/O lines can serve as slave-select lines for addressing multiple SPI devices. One I/O line controls the MAX1168's chip-select input. When you use it with an

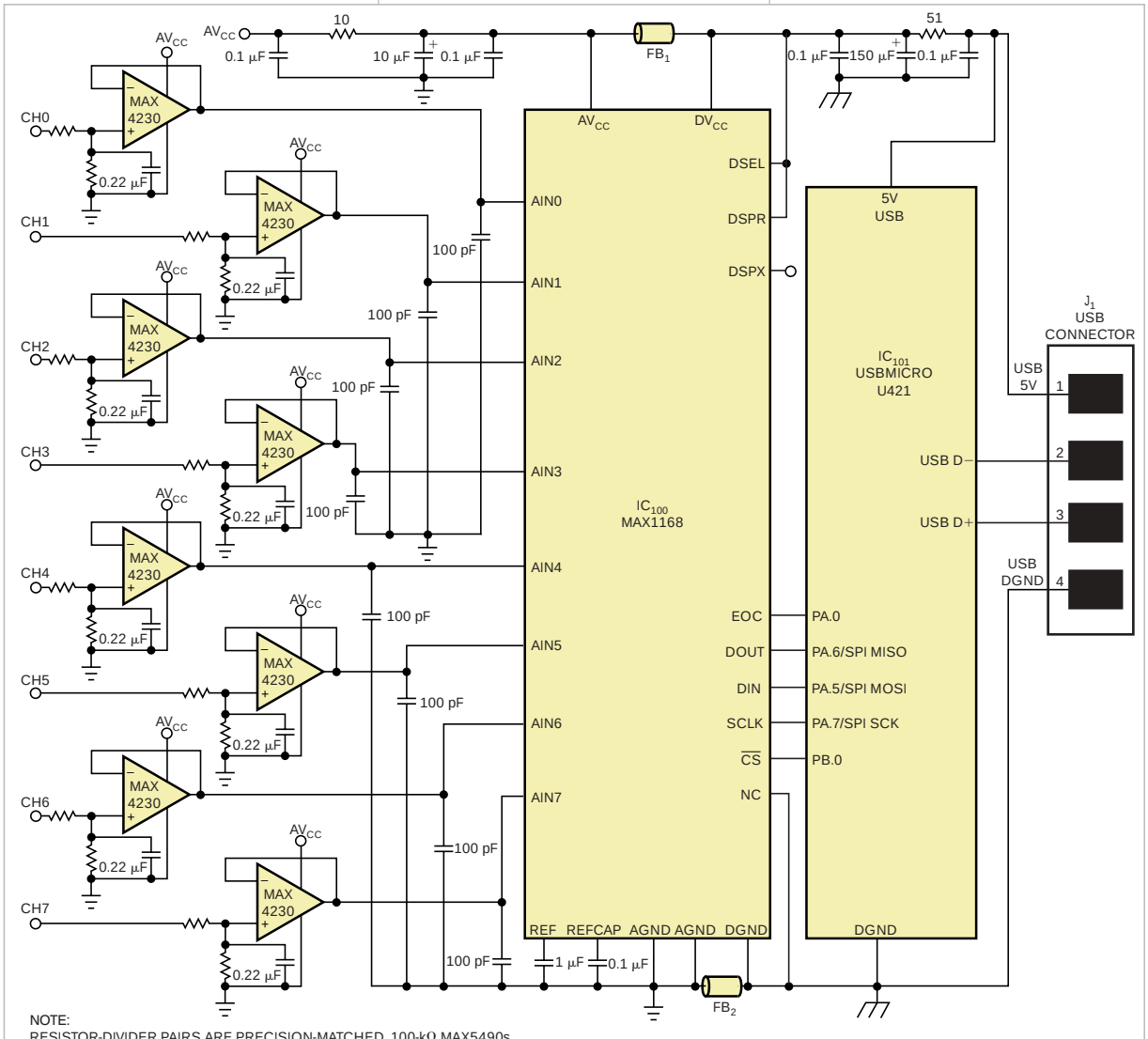


Figure 1 This simple data-acquisition system provides eight channels of 16-bit data to a host computer through a USB interface.

HID (human-interface device), the U421 USB controller can transfer data at rates as high as 800 bytes/sec. With additional filtering to reduce noise, the USB port provides 5V power to the circuit.

The MAX1168's sample-and-hold circuit must acquire the input voltage and charge its 45-pF holding capacitor in 3 μsec and thus requires a fast amplifier to minimize acquisition errors. Available in dual and quad versions, the MAX4230 provides a 10-MHz bandwidth, 2V/μsec slew rate, rail-to-rail inputs and outputs, and the ability to operate from a 5V rail or from voltages as low as 2.7V. The MAX4230's bias current—typically, 50 pA—allows significant input impedance without affecting accuracy.

To provide protection from overvoltages and apply input-voltage scaling, each buffer amplifier's input includes a 100-kΩ precision-matched resistive divider. This application uses Maxim's MAX5490VA10000 10-to-1 dividers, which provide a scaling factor of $^1/_{11}$, to allow maximum readable inputs of 45V at resolutions of 687.5 μV.

Figure 2 User-interface software for the data-acquisition system allows selection of operating parameters. In this image, the lower three channels are unselected and hence are not visible in the display.

Written in Microsoft's Visual Basic.Net, Standard Edition, the evaluation software provides commands to the U421 through the USBm.dll DLL (dynamic-linking-library) file. The demo program sets the MAX1168 to scan all eight channels and display the results. When you run the program, the Visual Basic form allows you to set the reference voltage to allow for the input divider, select the scan time, and enable any of the eight input channels for screen display (Figure 2). You can download the evaluation software at www.maxim-ic.com/MAX=1168DI. EDN

ACKNOWLEDGMENT

Thanks to Robert Severson of USBmicro for his help with the interface.

BY JIM WILLIAMS • LINEAR TECHNOLOGY CORP

High-voltage, low-noise dc/dc converters

YOU CAN MAKE A 1-kV DC/DC CONVERTER WITH ONLY 100 μV OF NOISE.

Photomultipliers, avalanche photodiodes, ultrasonic transducers, condenser microphones, radiation detectors, and similar devices require high-voltage, low-current biasing. Additionally, the high voltage must be free of noise. A common requirement is less than 1 mV of noise, and these devices sometimes require noise to be less than a few hundred microvolts. Switching-regulator configurations cannot normally achieve this performance level without employing special techniques. One aid to achieving low noise is the fact that load currents rarely exceed 5 mA. This freedom permits the use of output-filtering methods that are otherwise impractical.

This article describes a variety of circuits featuring outputs of 200 to 1000V with less than 100 μV of output noise in a 100-MHz bandwidth. Special techniques, most notably power stages that minimize high-frequency harmonic content, enable this performance. Although sophisticated, all these examples use standard, commercially available magnetic components. This provision should help you quickly arrive at a manufacturable design.

Before proceeding any further, understand that you should use caution in the construction, testing, and use of the circuits this article describes. High-voltage, lethal potentials are present in these circuits. Use extreme caution in working with and making connections to these circuits. Again, these circuits contain dangerous, high-voltage potentials.

RESONANT ROYER-BASED CONVERTERS

The resonant Royer topology suits low-noise operation due to its sinusoidal power delivery (**references 1** and **2**). The resonant Royer is attractive because transformers for LCD-backlight service are readily available. These transformers are available from multiple sources, well-proven, and competitively priced. **Figure 1**'s resonant Royer topology achieves 100-μV-p-p noise at 250V output by minimizing high-frequency harmonics in the power-drive stage. The self-oscillating resonant Royer circuitry comprises Q_2, Q_3, C_1, T_1, and L_1. Current flow through L_1 causes the T_1, Q_2, Q_3, and C_1 circuitry to oscillate in resonant fashion, supplying sine-wave drive to T_1's primary with resultant sinelike high voltage appearing across the secondary.

T_1's rectified and filtered output feeds back to amplifier-reference A_1, which biases the Q_1 current sink, completing a control loop around the Royer converter. L_1 ensures that Q_1 maintains constant current at high frequency. Milliampere-level output current allows the presence of a 10-kΩ resistor in the output filter. This resistor greatly aids filter performance with minimal power loss. The low cur-

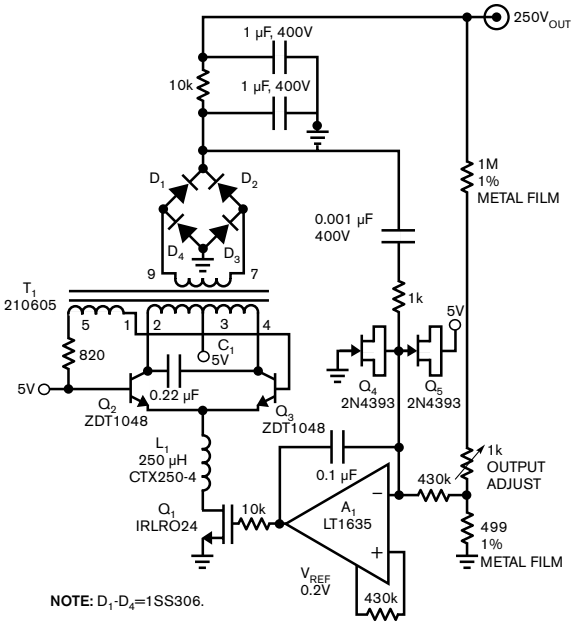


Figure 1 This current-fed resonant Royer converter produces a high-voltage output. Amplifier A_1 biases the Q_1 current sink. This step creates a feedback loop that stabilizes the output voltage. Amplifier A_1's 0.001-μF-capacitor, 1-kΩ-resistor network creates a phase lead relative to the output filter, thereby optimizing transient response. Low-leakage clamp diodes D_5 and D_6 protect A_1.

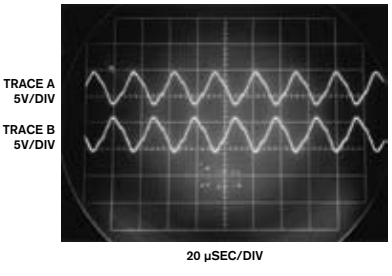


Figure 2 The waveforms of a resonant Royer collector are distorted sinusoids, containing no high-frequency content.

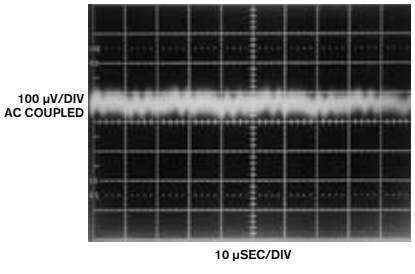


Figure 3 The output noise of the circuit in Figure 1 is barely discernible relative to the instrumentation's 100-μV noise floor.

rent requirements permit certain freedoms in the output filter and feedback network (see **sidebar** "Feedback considerations in high-voltage dc/dc converters" at www.edn.com/ms4295). The RC path to A_1's negative input combines with the 0.1-µF capacitor to compensate A_1's loop. D_5 and D_6, low-leakage clamps, protect A_1 during start-up and transient events. Although **Figure 2**'s collector waveforms are distorted, no high-frequency content is present.

The circuit's low harmonic content combines with the RC-output filter to produce a transcendently clean output. Output noise (**Figure 3**) is just discernible in the monitoring instrumentation's 100-µV noise floor (**Reference 3**).

Figure 4's variant of **Figure 1** maintains 100-µV output noise and extends the input-supply range to 32V. Q_1 may require heat-sinking at high input-supply voltage. Converter and loop operation remains the same as in **Figure 1**, although **Figure 4** re-establishes compensation components to accommodate the LT1431 control element.

The previous resonant Royer examples use linear control of converter current to furnish harmonic-free drive. The trade-off is decreased efficiency, particularly as input voltage scales. You can improve efficiency by employing switched-mode current drive to the Royer converter. Unfortunately, such switched drive usually introduces noise. However, you can counter this undesirable consequence.

Figure 5 replaces the linearly operated current sink with a switching regulator. The Royer converter and its loop are the same as in **Figure 4**; **Figure 6**'s transistor-collector waveshape (Trace A) is similar to that of the other circuits. The high-speed, switched-mode current-sink drive (Trace B) efficiently feeds L_1. This switched operation improves efficiency but degrades output noise. **Figure 7** shows switching-regulator harmonic clearly responsible for 3-mV-p-p output noise—about 30 times greater than that of the linearly operated circuits.

Careful examination of **Figure 7** reveals almost no Royer-based residue. Switching-regulator artifacts dominate the noise. Eliminating this switching-regulator-originated noise and maintaining efficiency requires special circuitry, but this circuitry is readily available (**Figure 8**). The resonant Royer converter and its loop are reminiscent of the circuits in the preceding **figures**. The fundamental difference is the LT1534 switching regulator that uses controlled transition times to retard high-frequency harmonic and maintain efficiency. This approach blends switching and linear-current-sink benefits (**Reference 3**). R_V and R_I set the voltage and current-transition rate, respectively, which represents a compromise between efficiency and noise reduction.

Figure 9's Royer collector waveshape (Trace A) is nearly identical to the one that **Figure 5**'s circuit produces. Trace B, depicting LT1534-controlled transition times, markedly departs from its **Figure 5** counterpart. These controlled transition times dramatically reduce output noise (**Figure 10**) to 150 µV p-p—a 20-fold improvement over **Figure 7**'s LTC3401-based results.

Figure 11 is essentially identical to **Figure 8**, except that it produces a −1000V output. A_1 provides low impedance, inverting feedback to the LT1534. **Figure 12a**'s output noise measures less than 1 mV. As before, resonant Royer ripple dominates the noise; no high-frequency content is detectable.

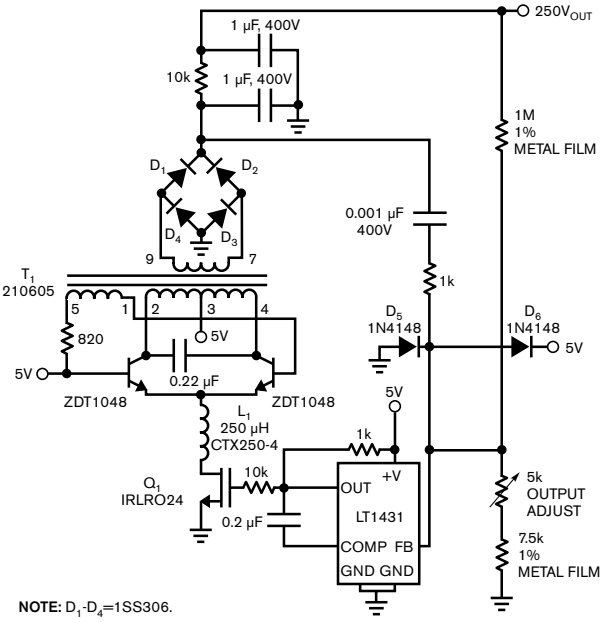


Figure 4 This variant of Figure 1 employs the LT1431 regulator, maintains 100-µV output noise, and extends the input-supply range to 32V. Transistor Q_1 may require a heat sink if input-supply voltages are high.

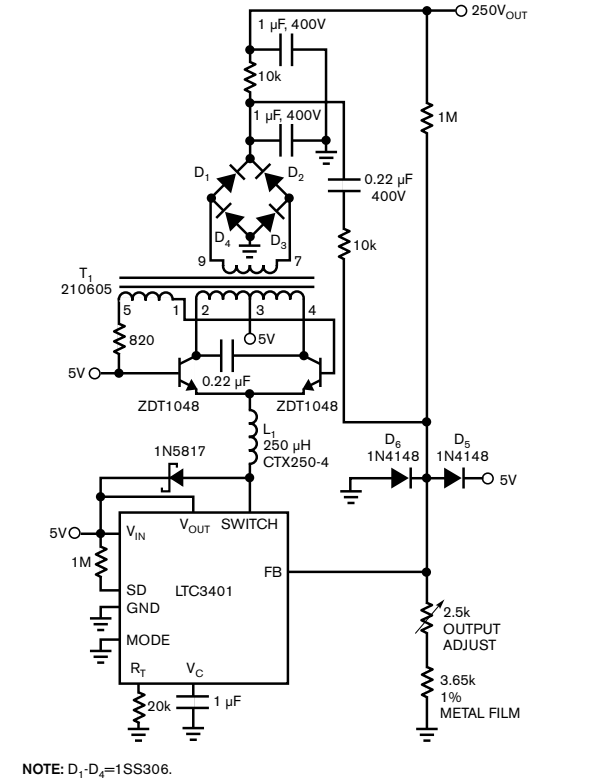


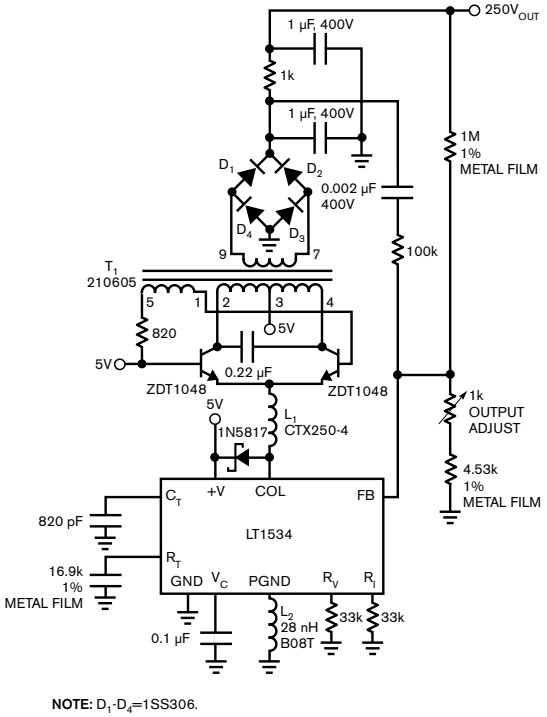
Figure 5 In this circuit, a switching regulator replaces the linearly operated current sink of Figure 4. This approach minimizes heating, although the output noise increases.

It is worth noting that this noise figure proportionally improves with increased filter-capacitor values. For example, **Figure 12b** indicates only 100-µV noise with 10-times-higher filter-capacitor values, although the capacitors are physically large. The original values represent a reasonable compromise between noise performance and physical size.

PUSH-PULL CONVERTERS

Controlled transition techniques are also directly applicable to push-pull architectures. **Figure 13** uses a controlled transition push-pull regulator in a simple loop to control a 300V output converter. Symmetrical-transformer drive and controlled switching-edge times promote low output noise. The D_1- through D_4-connected damper further minimizes residual aberrations. In this case, the output filter uses inductors, although you could employ appropriate resistor values. **Figure 14** displays smooth transitions at the transformer secondary outputs. (Trace A is T_1 Pin 4, and Trace B is T_1 Pin 7.) The absence of high-frequency harmonic results in extremely low noise. **Figure 15**'s fundamental-related output residue approaches the 100-µV measurement noise floor in a 100-MHz bandpass. This performance is spectacularly low noise in any dc/dc converter, and certainly in one providing high voltage. Here, at 300V output, noise represents less than 1 part in 3 million.

Figure 16 is similar, except that output range varies from 0 to 300V. An LT3439, which contains no control elements, replaces the LT1533. It simply drives the transformer with 50%-duty-cycle, controlled switching transitions. A_1, Q_1, and Q_2 enforce feedback control by driving current into T_1's primary center tap. A_1 compares a resistively derived portion of the output with a user-supplied control voltage. These values produce a 0 to 300V output in response to a 0 to 1V control voltage. An RC network from Q_2's collector to A_1's positive input compensates the loop. Collector waveforms and output-noise signature are nearly identical to those in **Figure 13**. Output noise is 100 µV p-p over the entire 0 to 300V output range.



NOTE: D_1-D_4=1SS306.

Figure 8 The LT1534 switching regulator features controlled transition times that minimize high-frequency harmonics and maintain low heat dissipation. The approach blends the benefits of switching- and linear-current-sink circuits.

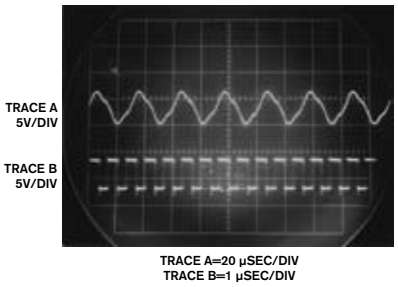


Figure 6 The resonant Royer collector waveshape (Trace A) is similar to that of the previous circuits. An efficient, high-speed, switched-mode current-sink drive feeds inductor L_1 (Trace B).

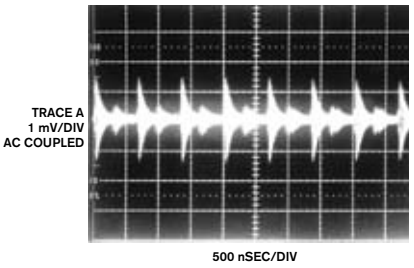


Figure 7 The switching-regulator harmonic in Figure 5 results in 3-mV-p-p output noise.

provide surprisingly good performance, particularly at low output current. **Figure 17**'s design provides 200V from a 5V input (**references 4** and **5**). The scheme is a basic inductor-flyback-boost regulator with some important deviations. Q_1, a high-voltage device, resides between the LT1172 switching regulator and the inductor. This approach permits the regulator to control Q_1's high-voltage switching without undergoing high-

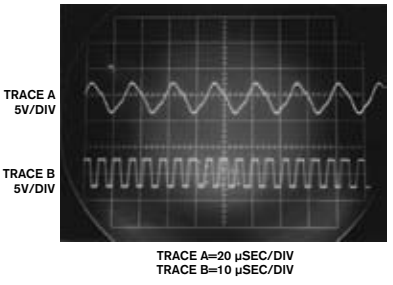


Figure 9 The resonant Royer collector waveshape is identical to that of the LT3401 circuit in Figure 5 (Trace A). The controlled transition times of the LT1534 current sink attenuate the high-frequency harmonics (Trace B).

FLYBACK CONVERTERS

You don't usually associate flyback converters, with their abrupt, poorly controlled energy delivery, with low-noise output. However, careful magnetic selection and layout can

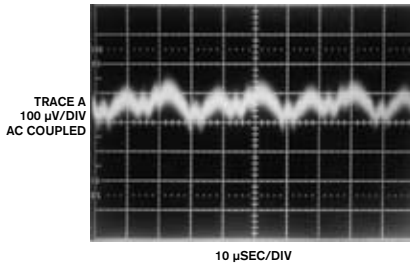
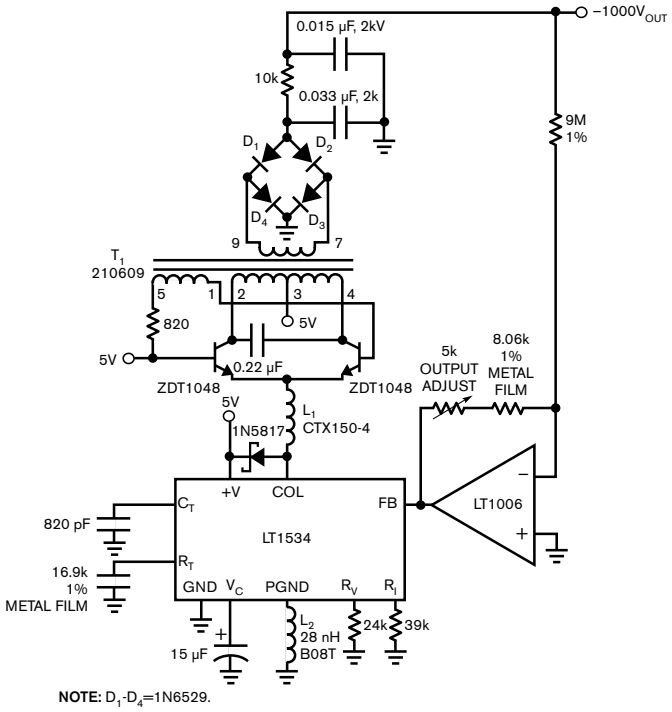
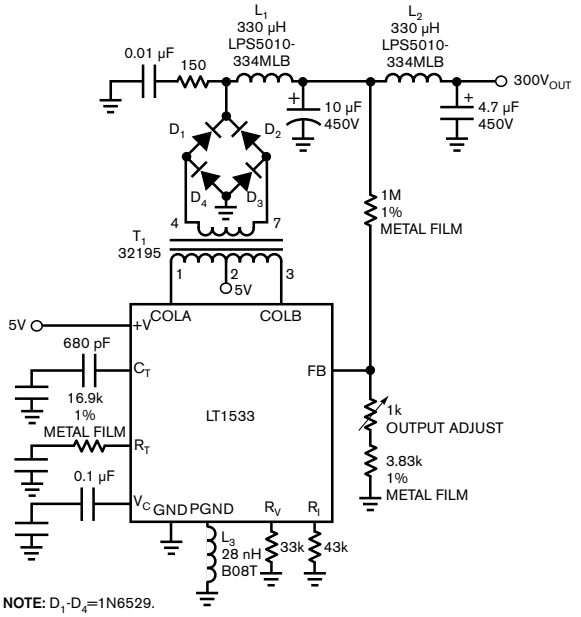


Figure 10 The controlled transition times dramatically lower noise to 150 µV p-p, a 20-fold improvement over that of Figure 7.



NOTE: D$_1$-D$_4$=1N6529.

Figure 11 This −1000V negative-output converter uses the controlled-transition-time feature of the LT1534. Amplifier A$_1$ provides low impedance, inverting feedback to the LT1534 IC.



NOTE: D$_1$-D$_4$=1N6529.

Figure 13 This converter circuit features a push-pull drive with controlled transitions and provides a 300V output. The symmetrical-transformer drive and slow edge transitions promote low output noise.

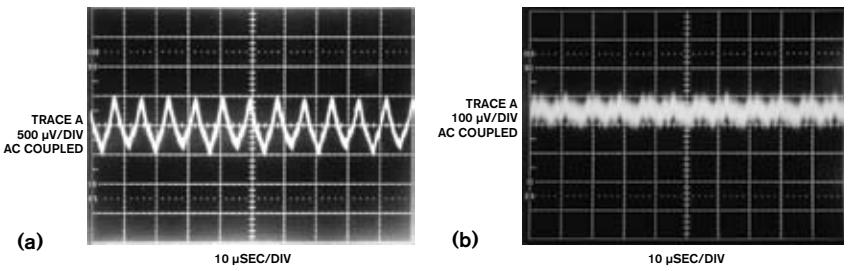


Figure 12 The −1000V converter's output noise measures less than 1 mV—that is, 1 ppm, or 0.0001%—in a 100-MHz bandwidth (a). The resonant Royer ripple voltage dominates the residue. There is no detectable high-frequency content. Output noise decreases to 100 µV by using 10-times-larger filter capacitors than those in Figure 11 (b). The penalty is the size of the capacitors.

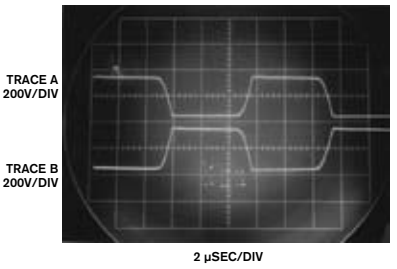


Figure 14 The outputs of the transformer secondary have no high-frequency artifacts.

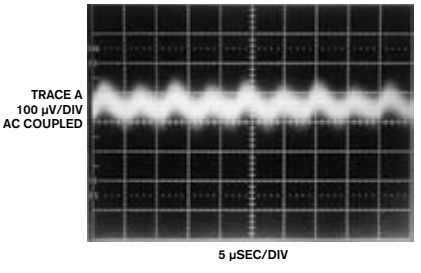


Figure 15 The output noise of the push-pull converter circuit in Figure 13 is barely discernible relative to the instrumentation's 100-µV noise floor. No wideband components appear in the 100-MHz measurement passband.

voltage stress. Q_1, operating as a cascode with the LT1172's internal switch, withstands L_1's high-voltage flyback events (**references 6** through **10**).

Diodes associated with Q_1's source-terminal clamp, L_1, originated spikes arriving through Q_1's junction capacitance. The high voltage is rectified and filtered, forming the circuits' output. The ferrite bead and 100 and 300Ω resistors aid filter efficiency (**references 11** and **12**). Feedback to the regulator stabilizes the loop and the V_C-pin network provides frequency compensation. A 100-kΩ path from L_1 bootstraps Q_1's gate drive to about 10V, ensuring saturation. The output-connected diode provides short-circuit protection by shutting down the LT1172 if the output is accidentally grounded.

Figure 18's traces A and C are LT1172 switch current and voltage, respectively. Q_1's drain is Trace B. Current-ramp termination results in a high-voltage flyback event at Q_1's drain. A safely attenuated version of the flyback appears

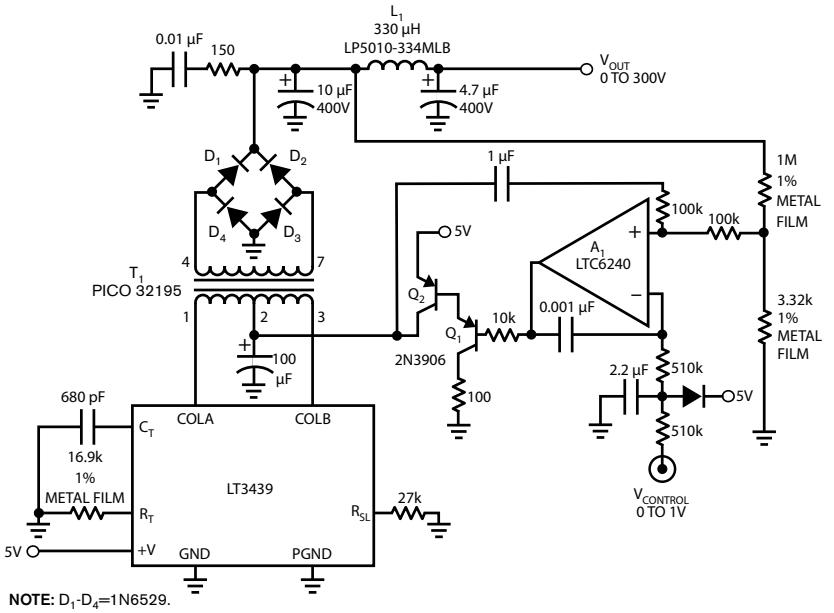


Figure 16 This circuit provides full-range adjustability. The control input, $V_{CONTROL}$, sets transformer T_1's drive voltage through Q_1 and Q_2. A 1-MΩ/3.32-kΩ resistive divider provides feedback that A_1's input capacitors stabilize. Waveforms are similar to those of Figure 13. The output noise is 100 µV p-p.

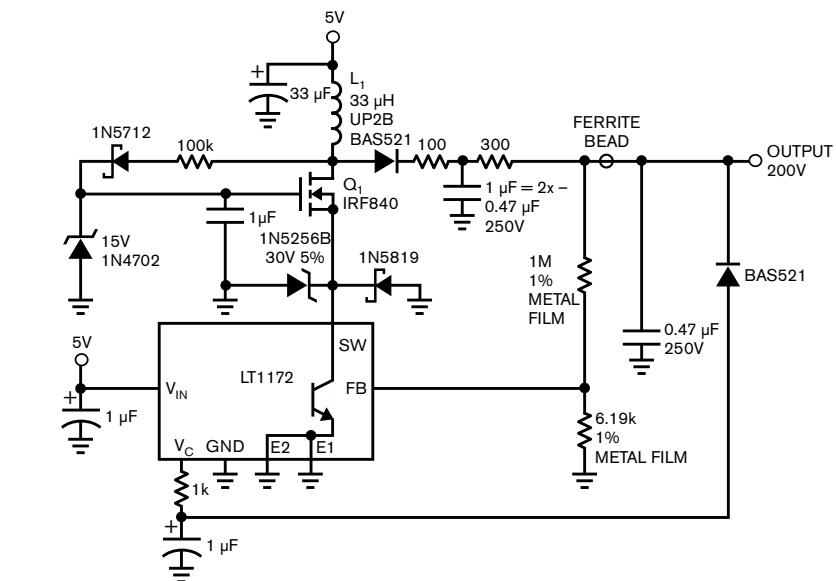


Figure 17 This converter has an output of 5 to 200V. Transistor Q_1 is in cascode with the LT1172 and switches the high voltage. This approach allows a low-voltage regulator to control the output. Diode clamps protect the regulator from transients. Flyback events at L_1 bootstrap Q_1's gate drive through the 100-kΩ resistor. The diode that connects to the output and the 300Ω resistor provide short-circuit protection. The ferrite bead and the 100 and 300Ω resistors minimize high-frequency output noise.

at the LT1172 switch. The sinusoidal signature, due to inductor ring-off between conduction cycles, is harmless. **Figure 19**, output noise, comprises low-frequency ripple and wideband, flyback-related spikes measuring 1 mV p-p in a 100-MHz bandpass.

In a transformer-coupled flyback cir-

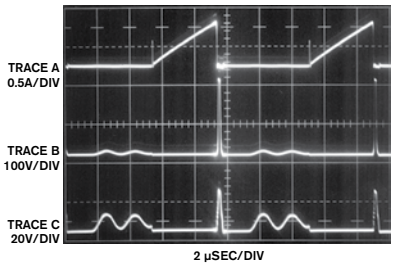


Figure 18 Waveforms for the 5 to 200V converter include the LT1172 switch current and voltage (traces A and C, respectively) and Q_1's drain voltage (Trace B). The termination of the current ramp results in a high-voltage flyback event at the drain of Q_1. A safely attenuated version appears at the LT1172 switch. The inductor ring-off between current-conduction cycles creates the sinusoidal signature, but it is harmless.

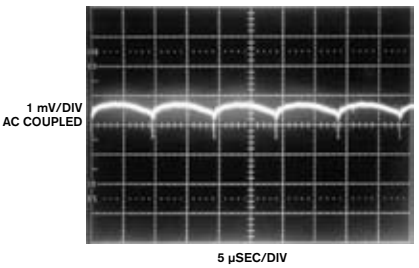


Figure 19 The output noise of the circuit in Figure 17 is 1 mV p-p in a 100-MHz bandpass. The noise comprises low-frequency ripple and wideband, flyback-related spikes.

cuit, the transformer secondary provides voltage step-up referred to the flyback-driven primary (**Figure 20**). The 4.22-MΩ resistor supplies feedback to the regulator, closing a control loop. A 10-kΩ, 0.68-µF filter network attenuates high-frequency harmonic with minimal voltage drop. **Figure 21** clearly shows flyback-related transients in the output noise, although they are within 300 µV p-p.

The circuit in **Figure 22** employs the LT3468 photoflash-capacitor charger as a general-purpose, high-voltage dc/dc converter. Normally, the LT3468 regulates its output at 300V by sensing T_1's flyback-pulse characteristic. This circuit allows the LT3468 to regulate at lower voltages by truncating its charge cycle before the output reaches 300V. A_1 compares a divided-down portion of the output with the program input voltage. When the output-derived potential at A_1's negative input exceeds the program voltage at A_1's positive input, A_1's output goes low, shutting down the LT3468. The feedback capacitor provides ac hysteresis, sharpening A_1's output to prevent chattering at the trip point. The LT3468 remains shut down until the

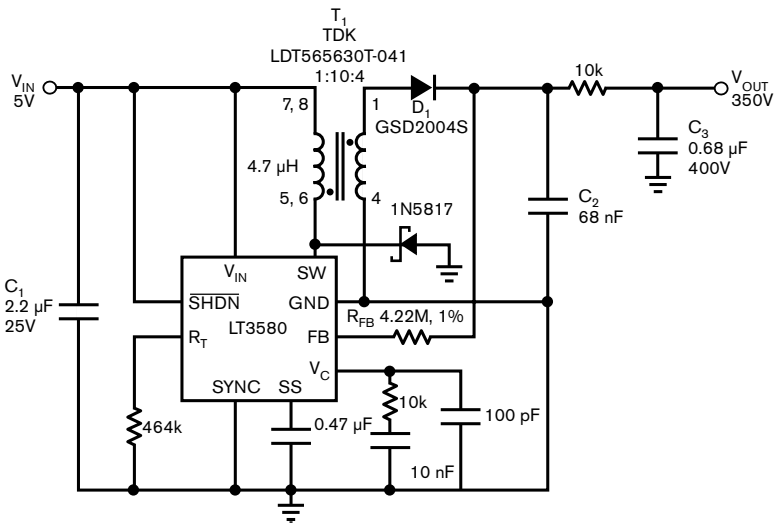


Figure 20 This 5V-powered transformer-coupled flyback converter produces a 350V output (courtesy Albert M Wu, Linear Technology).

output voltage drops low enough to trip A_1's output high, turning it back on. In this way, A_1's duty cycle modulates the LT3468, causing the output voltage to stabilize at a point that the program input determines.

Figure 23's 250V-dc output (Trace B) decays down about 2V until A_1 (Trace A) goes high, enabling the LT3468 and restoring the loop. This simple circuit works well, regulating over a programmable 0 to 300V range, although its inherent hysteretic operation mandates the unacceptable 2V output-ripple noted. The loop-repetition rate varies with the input voltage, output setpoint, and load, but the ripple is always present.

The circuit in **Figure 24** greatly reduces ripple amplitude, although complexity increases. The circuit's postregulator reduces the output ripple and noise of **Figure 22**'s circuit to only 2 mV. A_1 and the LT3468 are identical to **Figure 23**'s circuit, except for the 15V zener diode in series with the 10-MΩ/100-kΩ feedback divider. This component causes C_1's voltage, and hence Q_1's collector, to regulate 15V above the $V_{PROGRAM}$ input-dictated point. The $V_{PROGRAM}$ input also routes to the A_2-Q_2-Q_1 linear postregulator. A_2's 10-MΩ/100-kΩ feedback divider has no zener diode, so the postregulator follows the $V_{PROGRAM}$ input with no offset. This arrangement forces 15V across Q_1 at all output voltages. This figure is high enough to eliminate undesirable ripple and noise from the output and keep Q_1's dissipation low.

Q_3 and Q_4 form a current limit, protecting Q_1 from overload. Excessive current through the 50Ω shunt turns on Q_3. Q_3 drives Q_4, shutting down the LT3468. Simultaneously, a portion of Q_3's collector current turns on Q_2 hard, shutting off Q_1. This loop dominates the normal regulation feedback, protecting the circuit until you remove the overload.

Figure 25 shows just how effective the postregulator is. When A_1 (Trace A) goes high, Q_1's collector (Trace B) ramps up in response. Note the LT3468's switching artifacts on the ramp's upward slope. When the A_1-LT3468 loop is satisfied, A_1 goes low and Q_1's collector ramps down. The output postregulator (Trace C), however, rejects the ripple, showing only 2 mV of noise. The slight blurring of the trace derives from A_1-LT3468 loop jitter.

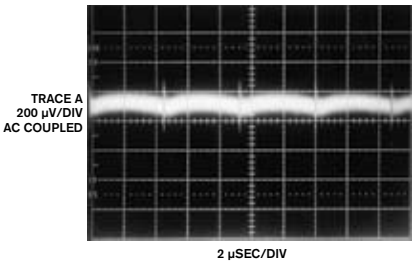


Figure 21 The high-speed transients in the circuit of Figure 20 produce a noise signature within 300 µV p-p.

CIRCUIT CHARACTERISTICS

Table 1 (at www.edn.com/ms4295) summarizes and notes the salient characteristics of the circuits in this article. This **table** is only a generalized guideline and not an indicator of capabilities or limits. Too many variables and exceptions exist to accommodate the cate-

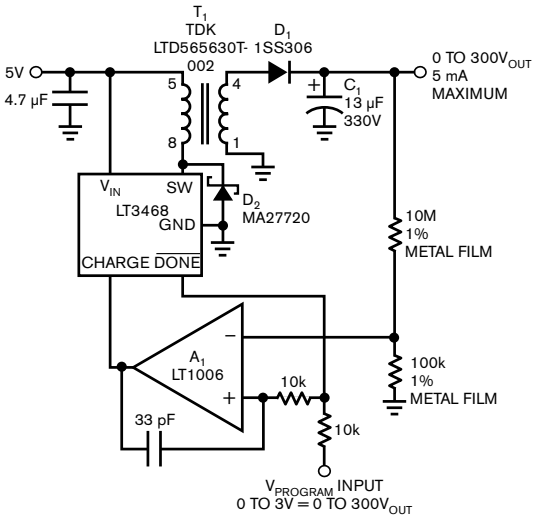


Figure 22 This regulator output is voltage-programmable between 0 and 300V. Amplifier A_1 controls the regulator output by modulating the duty cycle of the LT3468/T_1 dc/dc converter's power delivery.

gorical statement the **table** implies. The interdependence of circuit parameters makes summarizing or rating various approaches a hazardous exercise. There is simply no intellectually responsible way to streamline the selection and design process if you want optimum results. A meaningful choice must be the outcome of laboratory-based experimentation. Too many interdependent variables and surprises exist for a systematic, theoretically based selection. Tables such as this one seek authority through glib simplification, and simplification is disaster's deputy. Nonetheless, **Table 1** (at www.edn.com/ms4295), in all its glory, lists input-supply range, output voltage, and current, along with comments for each circuit. EDN

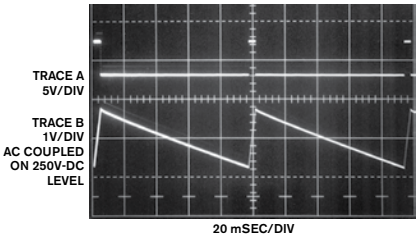


Figure 23 The duty-cycle-modulated operation of the circuit in Figure 22 shows that the high-voltage output (Trace B) ramps down until A_1 (Trace A) goes high. This approach enables the LT3468/T_1 to restore the output. The loop-repetition rate varies with input voltage, output setpoint, and load.

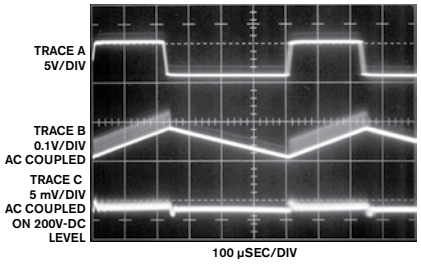


Figure 25 The low-ripple output (Trace C) is apparent in the postregulator's operation. Traces A and B are the output of A_1 and Q_1's collector, respectively. The blurring of the trace, right of the photo's center, derives from loop jitter.

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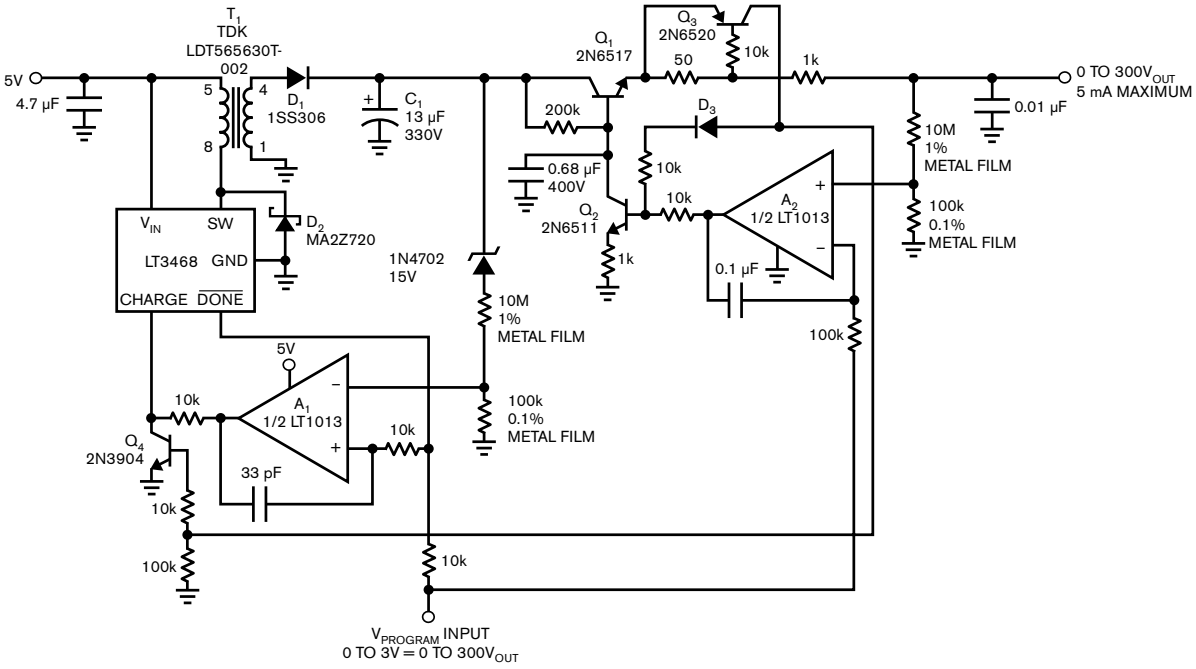

Figure 24 Adding postregulation to the circuit of Figure 22 reduces the output ripple from 2V to 2mV. An LT3468-based dc/dc converter, similar to the one in Figure 22, delivers high voltage to the collector of Q_1. Amplifier A_2 and Q_1 and Q_2 form a tracking, high-voltage linear regulator. The zener diode sets Q_1's collector-to-emitter voltage to 15V, ensuring tracking with minimal power dissipation. Transistors Q_3 and Q_4 limit the short-circuit output current.

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DIODE-TURN-ON-TIME-INDUCED FAILURES IN SWITCHING REGULATORS

NEVER HAVE SO MANY HAD SO MUCH TROUBLE WITH SO FEW TERMINALS.

BY JIM WILLIAMS AND DAVID BEEBE • LINEAR TECHNOLOGY CORP

Most circuit designers are familiar with diode dynamic characteristics, such as charge storage, voltage-dependent capacitance, and reverse recovery time. Manufacturers less commonly acknowledge and specify diode forward turn-on time. This parameter describes the time required for a diode to turn on and clamp at its forward-voltage drop. Historically, this extremely short time, measured in nanoseconds, has been so small that user and vendor alike have essentially ignored it. They rarely discuss and almost never specify it. Recently, switching-regulator clock rate and transition time have become faster, making diode-turn-on time a critical issue. The industry has mandated increased clock rates to achieve smaller magnetics; decreased transition times somewhat aid overall efficiency but are principally needed to minimize IC heat rise. At clock speeds beyond about 1 MHz, transition-time losses are the primary sources of die heating.

A potential difficulty due to diode-turn-on time is that the resultant transitory overshoot voltage across the diode, even when restricted to nanoseconds, can induce overvoltage stress, causing switching-regulator-IC failure. As such, careful testing is required to qualify a given diode for a particular application to ensure reliability. This testing, which assumes low-loss surrounding components and layout in the final application, measures turn-on overshoot voltage due to diode parasitics only. Improper associated component selection and layout will contribute additional overstress terms.

DIODE TURN-ON TIME

Figure 1 shows typical step-up and step-down voltage converters. In both cases, the assumption is that the diode clamps switch pin-voltage excursions to safe limits. In the step-up case, the switch pin's maximum allowable forward voltage defines this limit. The switch pin's maximum allowable reverse voltage sets the step-down case limit.

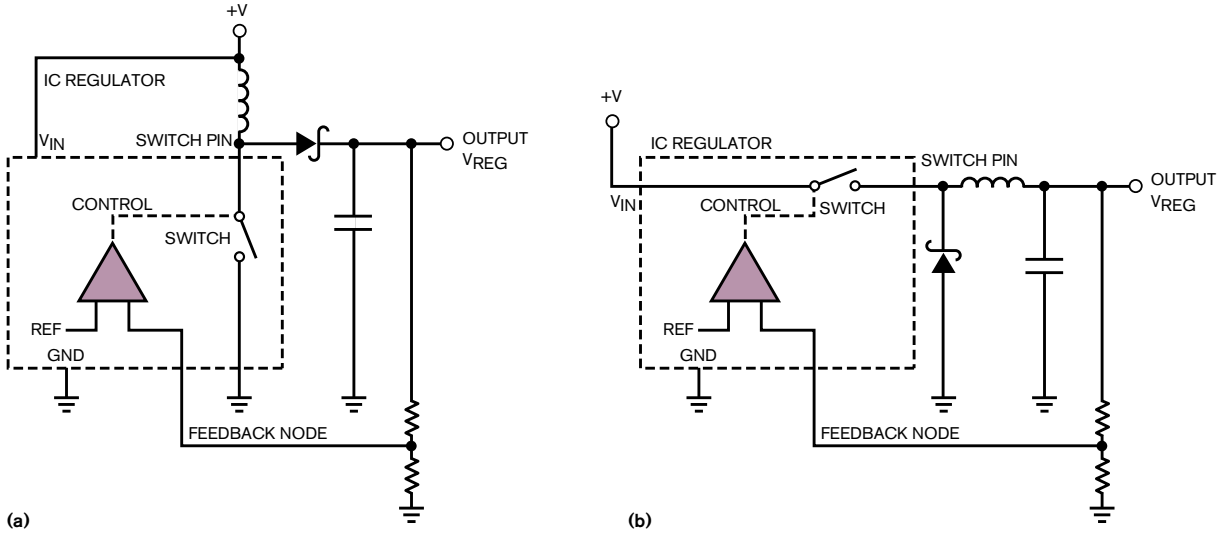

Figure 1 In both typical-voltage-step-up (a) and step-down converters (b), assume that the diode clamps the switch pin-voltage excursion to a safe limit.

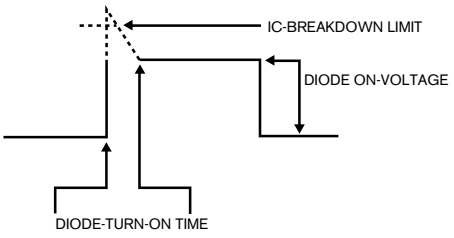

Figure 2 The diode-forward-turn-on time permits transient excursion above nominal diode clamp voltage, potentially exceeding the IC-breakdown limit.

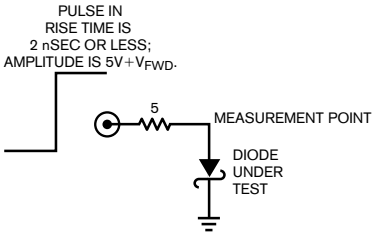

Figure 3 A conceptual method tests diode-turn-on time at 1A. The input step must have an exceptionally fast, high-fidelity transition.

Figure 2 indicates that the diode requires a finite length of time to clamp at its forward voltage. This forward-turn-on time permits transient excursions above the nominal diode-clamp voltage, potentially exceeding the IC's breakdown limit. You typically measure the turn-on time in nanoseconds, making observation difficult. A further complication is that the turn-on overshoot occurs at the amplitude extreme of a pulse waveform, precluding high-resolution amplitude measurement. You must consider these factors when designing a diode-turn-on-test method.

Figure 3 shows a conceptual method for testing diode-turn-on time. Here, the test is performed at 1A, although you could use other currents. A pulse steps 1A into the diode under test via the 5Ω resistor. You measure turn-on-time-voltage excursion directly at the diode under test. The **figure** is deceptively simple. In particular, the current step must have an exceptionally fast, high-fidelity transition, and faithful turn-on time determination requires substantial measurement bandwidth.

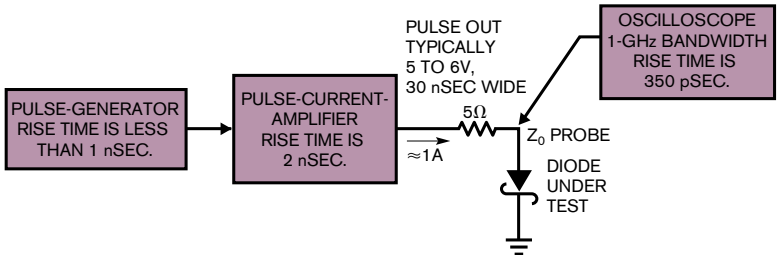

Figure 4 A detailed measurement scheme indicates necessary performance parameters for various elements.

DETAILED MEASUREMENT

Figure 4 offers a more detailed measurement scheme. The design requires a less-than-1-nsec-rise-time pulse generator; a 1A, 2-nsec-rise-time amplifier; and a 1-GHz oscilloscope. These specifications represent realistic operating conditions; you may select other currents and rise times by altering appropriate parameters (see **sidebar** "Connections, cables, attenuators, probes, and picoseconds").

The pulse amplifier necessitates careful attention to circuit configuration and layout. As **Figure 5** shows, the amplifier includes a paralleled, Darlington-driven RF-transistor-output stage. The collector-voltage adjustment, or rise-time trim, peaks Q_4 to Q_6 F_T; an in-

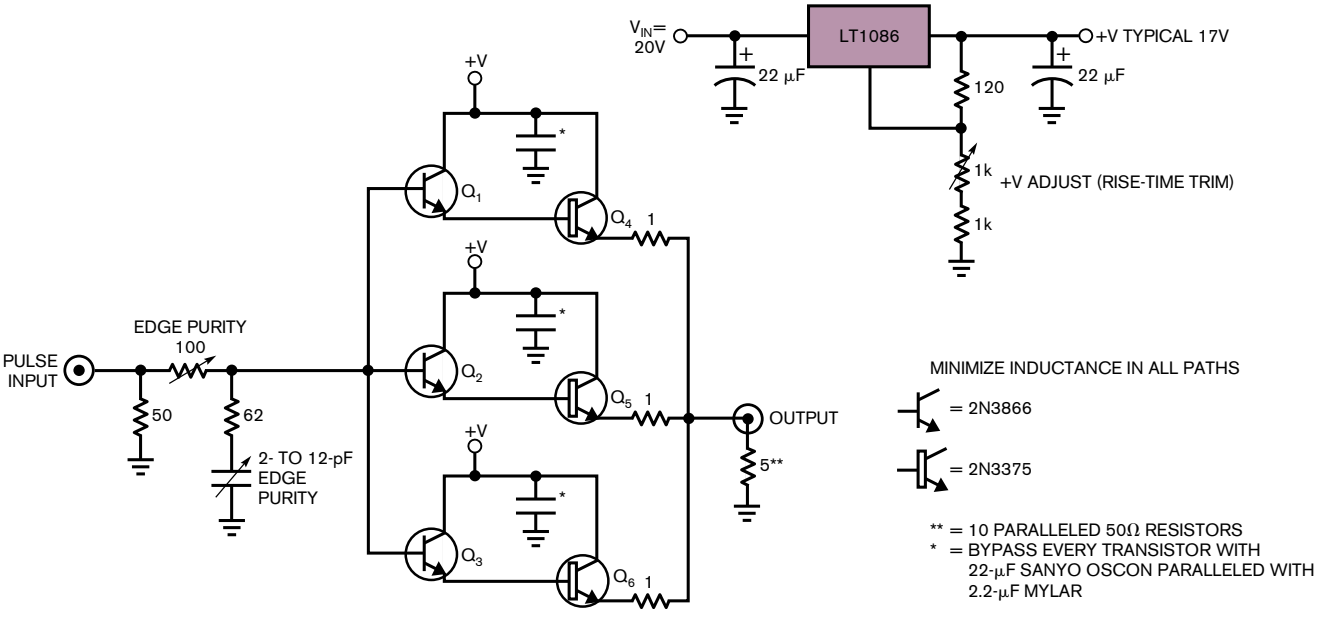

Figure 5 The pulse amplifier includes a paralleled, Darlington-driven RF-transistor-output stage. Collector-voltage adjustment, or rise-time trim, peaks Q_4 to Q_6 F_T, and the input-RC network optimizes output-pulse purity. A low-inductance layout is mandatory.

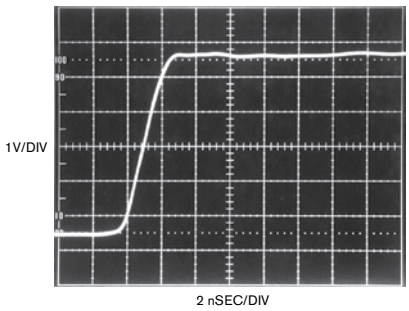

Figure 6 For a pulse-amplifier output into 5Ω, the rise time is 2 nsec with minimal pulse-top aberrations.

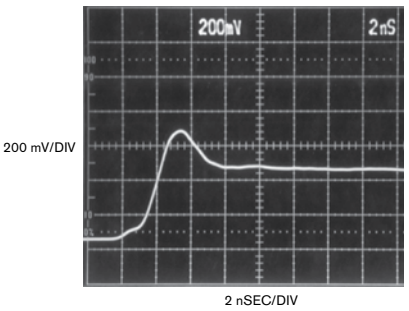

Figure 8 Diode 1 overshoots steady-state forward voltage for approximately 3.6 nsec, peaking at 200 mV.

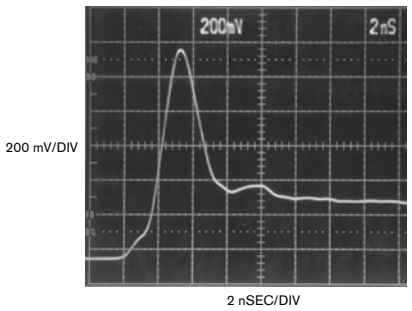

Figure 9 Diode 2 peaks at approximately 750 mV before settling in 6 nsec, more than twice the steady-state forward voltage.

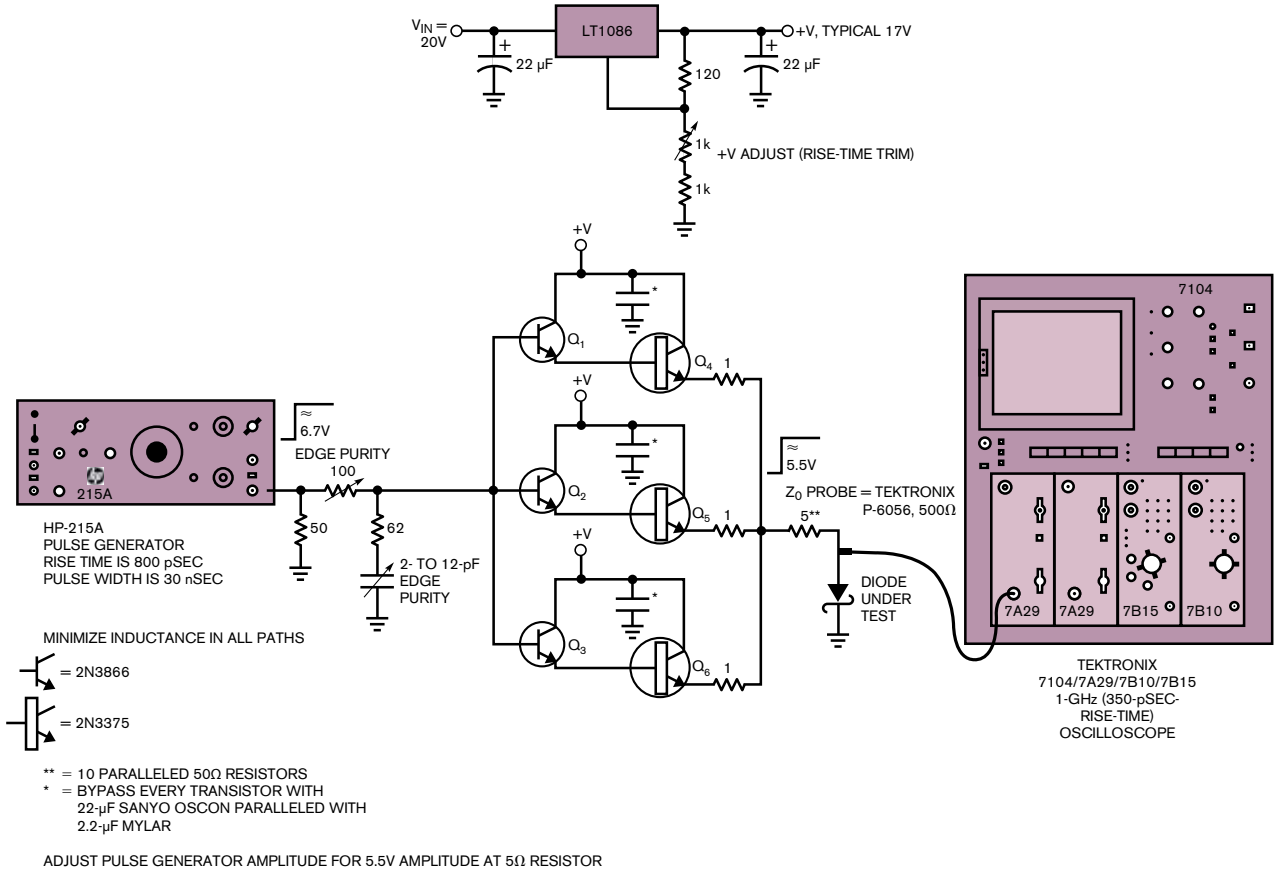

Figure 7 A complete diode-forward-turn-on-time-measurement arrangement includes a subnanosecond rise-time pulse generator, pulse amplifier, Z_0 probe, and 1-GHz oscilloscope.

put-RC network optimizes output-pulse purity by slowing the input-pulse rise time to within the amplifier passband. Paralleling allows Q_4 to Q_6 to operate at favorable individual currents, maintaining bandwidth. When you optimize the mildly interactive edge-purity and rise-time trims, **Figure 6** indicates, the amplifier produces a transcendently clean 2-nsec rise-time output pulse devoid of ringing, alien components, or post-transition excursions. Such performance makes diode-turn-on-time testing practical (see **sidebar** "Verifying rise-time-measurement integrity" in the Web version of this article at www.edn.com/090108df).

Figure 7 depicts the complete diode-forward-turn-on-time-measurement arrangement. The pulse amplifier, driven by a subnanosecond pulse generator, drives the diode under test. A Z_0 probe monitors the measurement point and feeds a 1-GHz oscilloscope.

DIODE TESTING

The measurement-test fixture, properly equipped and constructed, permits diode-turn-on-time testing with excellent time and amplitude resolution. **Figures 8** through **12** show results for five diodes from various manufacturers. **Figure 8** (Diode 1) overshoots steady-state

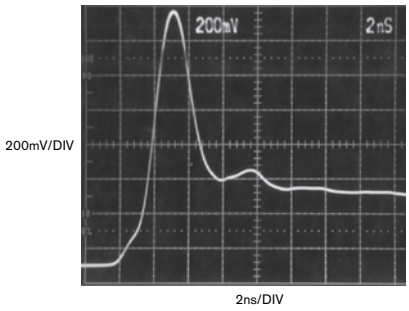

Figure 10 Diode 3 peaks at 1V above nominal 400-mV V_{FWD}, a 2.5× error.

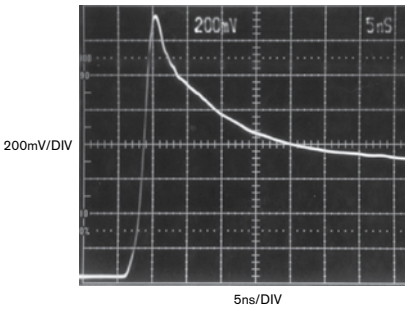

Figure 11 Diode 4 peaks at approximately 750 mV with lengthy tailing toward the V_{FWD} value. (Note the horizontal 2.5-times scale change.)

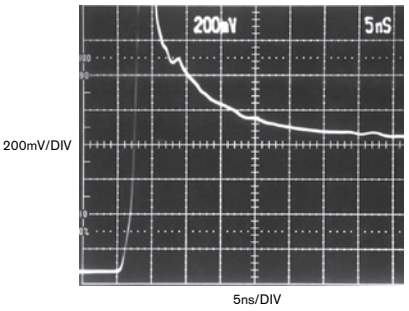

Figure 12 Diode 5 peaks offscale with extended tailing. Note the horizontal slower scale compared with figures 8 through 10.

forward voltage for 3.6 nsec, peaking at 200 mV, offering the best performance of the five. **Figures 9** through **12** show increasing turn-on amplitudes and times. In the worst cases, turn-on amplitudes exceed nominal clamp voltage by more than 1V, and turn-on times extend for tens of nanoseconds. **Figure 12** culminates this unfortunate parade with huge time and amplitude errors. Such errant excursions can and will cause IC-regulator breakdown and failure. The lesson here is clear: You must characterize and measure diode turn-on time in any given application to ensure reliability. EDN

For more sidebars related to this article and a list of references used, go to www.edn.com/090108df.

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CONNECTIONS, CABLES, ADAPTERS, ATTENUATORS, PROBES, AND PICOSECONDS

You must consider rise-time signal paths of less than 1 nsec as transmission lines. Connections, cables, adapters, attenuators, and probes represent discontinuities in this transmission line, deleteriously affecting its ability to faithfully transmit the desired signal. The degree of signal corruption that a given element contributes varies with its deviation from the transmission line's nominal impedance. The practical result of such aberrations is degradation of pulse rise time, fidelity, or both. Accordingly, you should minimize the introduction of elements or connections to the signal path and use high-grade components for connections and elements.

Any form of connector, cable, attenuator, or probe must be fully specified for high-frequency use. Familiar BNC hardware becomes lossy at rise times much faster than 350 psec. SMA components are preferable for the rise times this article describes. Additionally, to minimize inductance, cable-induced mismatch, and distortion, connect the pulse-amplifier output directly to the diode under test without using cable. Avoid mixing signal-path hardware types via adapters. Adapters introduce significant parasitics, resulting in reflections, rise-time degradation, resonances, and other degrading behavior. Similarly, make oscilloscope connections directly to the instrument's 50Ω inputs, avoiding probes. If you must use probes, introduction to the signal path mandates attention to their connection mechanism and high-frequency compensation. Passive low-impedance types, commercially available in 500Ω and 5-kΩ impedances, have input capacitance of less than 1 pF (see sidebar "About low-impedance probes" in the Web version of this article at www.edn.com/090108df). You must carefully frequency-compensate any such probe before use, or measurement may be misrepresented. Inserting the probe into the signal path necessitates some form of signal pick-off, which nominally does not influence signal transmission. In practice, some amount of disturbance must be tolerated and its effect on measurement results evaluated. High-quality signal pick-offs always specify insertion loss, corruption factors, and probe-output scale factor.

Be vigilant when designing and maintaining a signal path. Skepticism, tempered by enlightenment, is a useful tool when constructing a signal path, and no amount of hope is as effective as preparation and directed experimentation.

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HOW MUCH BANDWIDTH IS ENOUGH?

Accurate wideband-oscilloscope measurements require bandwidth. Just how much do they need? A classic guideline is that end-to-end measurement-system rise time is equal to the root-sum-square of the system's components' rise times. The simplest case is two components: a signal source and an oscilloscope. Figure A's plot of $\sqrt{(\text{signal}^2+\text{oscilloscope}^2)}$ rise time versus error is illuminating. The figure plots signal-to-oscilloscope rise-time ratio versus observed rise time. Rise time is bandwidth restated in the time domain, where rise time (nsec)=350/bandwidth in megahertz.

The curve shows that measurement accuracy inside about 5% requires an oscilloscope three to four times faster than the input-signal rise time.

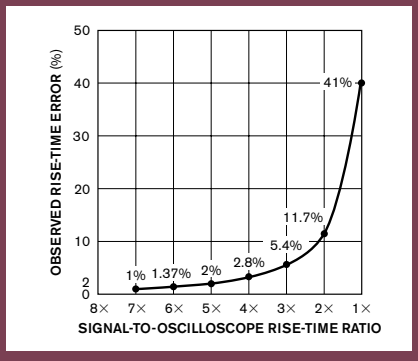


Figure A The measurement error rises rapidly as the signal-to-oscilloscope rise-time ratio approaches unity.

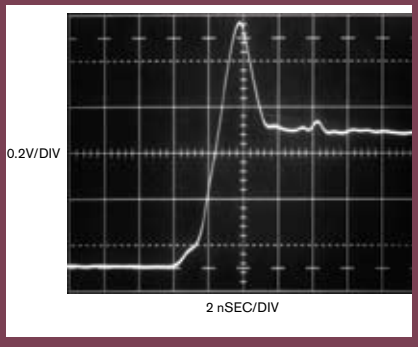


Figure B A typical diode turn-on viewed in a 2.5-GHz sampled bandpass displays 500-mV turn-on peak voltage.

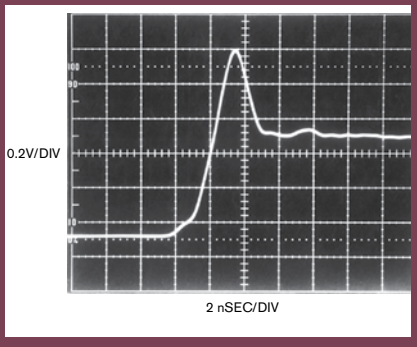


Figure C Figure B's diode turn-on observed in a 1-GHz real-time bandwidth has nearly identical characteristics, indicating adequate oscilloscope bandwidth.

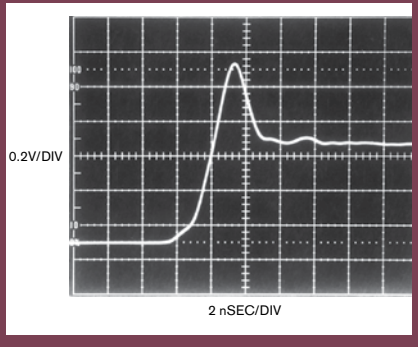


Figure D A 600-MHz oscilloscope bandwidth results in an approximately 440-mV observed peak, a 12% amplitude error.

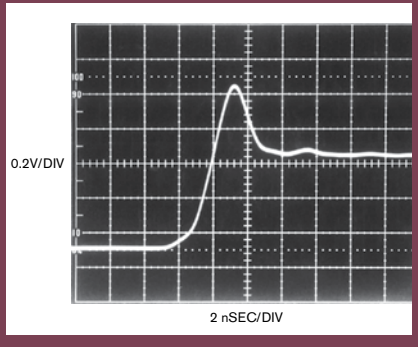


Figure E A 400-MHz measurement bandwidth causes 20% error.

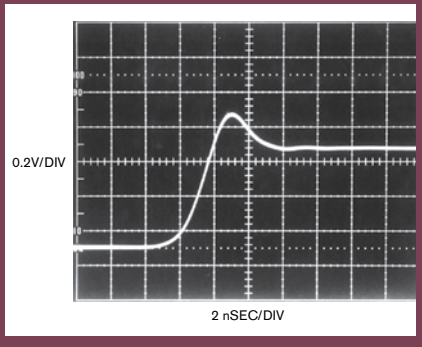


Figure F A 60% error occurs with a 200-MHz oscilloscope bandwidth.

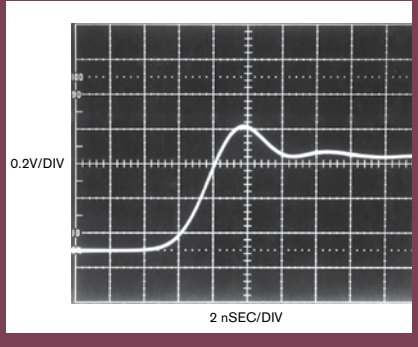


Figure G A 65% error occurs in the 75-MHz bandwidth.

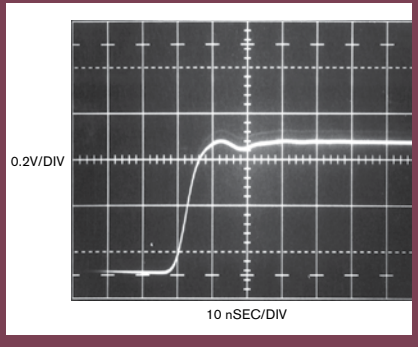


Figure H A 50-MHz oscilloscope just hints at peaking.

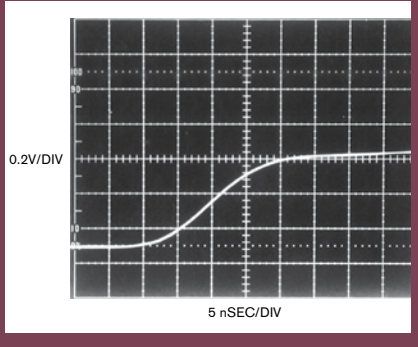


Figure I A 20-MHz oscilloscope bandwidth presentation is smooth and worthless.

TABLE A CARDINAL POINTS OF RISE TIME/BANDWIDTH

Rise time	Bandwidth
70 psec	5 GHz
350 psec	1 GHz
700 psec	500 MHz
1 nsec	350 MHz
2.33 nsec	150 MHz
3.5 nsec	100 MHz
7 nsec	50 MHz
35 nsec	10 MHz
70 nsec	5 MHz
350 nsec	1 MHz

Therefore, trying to measure a 1-nsec-rise-time pulse with a 350-MHz oscilloscope with a rise time of 1 nsec leads to erroneous conclusions. The curve indicates a monstrous 41% error. Note that this curve does not include the effects of passive probes or cables connecting the signal to the oscilloscope. Probes do not necessarily follow root-sum-square law, and you must carefully choose and apply them for a given measurement. Table A gives 10 cardinal points of rise-time/bandwidth equivalency between 1 MHz and 5 GHz.

Figures B through I illustrate pertinent effects of these considerations by viewing the main article's diode-turn-on-time measurement at various bandwidths. Figure B displays a typical diode turn-on in a 2.5-GHz sampled bandpass, showing 500-mV turn-on amplitude. Figure C's 1-GHz bandwidth measurement has nearly identical characteristics, indicating adequate oscilloscope bandwidth. The dramatic error in observed turn-on overshoot amplitude as bandwidth decreases in succeeding figures is readily apparent and should not be lost to the experimenter.

LESS-THAN-1-nSEC-RISE-TIME PULSE GENERATORS FOR THE RICH AND POOR

The pulse amplifier requires a less-than-1-nsec-input-rise-time pulse to cleanly switch current to the diode under test. Most general-purpose pulse generators have rise times of 2.5 to 10 nsec. Instrument rise times of less than 2.5 nsec are relatively rare, with only a select few types getting down to 1 nsec. The ranks of less-than-1-nsec-rise-time generators are even thinner, and costs are excessive. Subnanosecond-rise-time generation, particularly if you want relatively large swings of 5 to 10V, employs arcane technologies and exotic construction techniques. Available instruments in this class work well but can easily cost $10,000, with prices rising toward $30,000 depending on features. For benchwork, or even production testing, there are substantially less expensive approaches.

The secondary market offers less-than-1-nsec-rise-time pulse generators at attractive cost. The Hewlett-Packard HP-8082A transitions in less than 1 nsec, has a full complement of controls, and costs about $500. The Tektronix type 111 has edge times of 500 psec, with fully variable repetition rate and external-trigger capabilities. External charge-line length sets the pulse width. The device usually costs about $25. The HP-215A, long out of manufacture, has 800-psec edge times and is a clear bargain, typically costing less than $50.

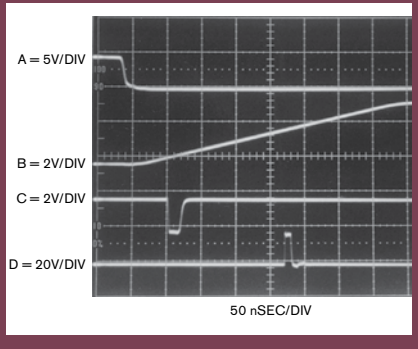


Figure B The pulse generator's waveforms include the clock (Trace A), Q_2's collector ramp (Trace B), the trigger output (Trace C), and the pulse output (Trace D). The delay sets the output pulse approximately 170 nsec after the trigger output.

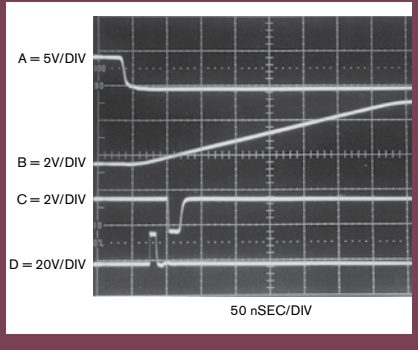


Figure C The pulse generator's waveforms are delay adjusted for the output pulse occurrence (Trace D) 25 nsec before the trigger output (Trace C). All other activity is identical to **Figure B**.

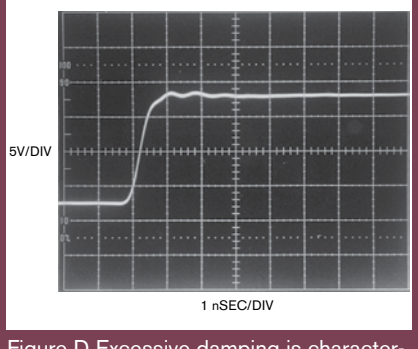


Figure D Excessive damping is characterized by front-corner rounding and minimal pulse-top aberrations. The trade-off is a relatively slow rise time.

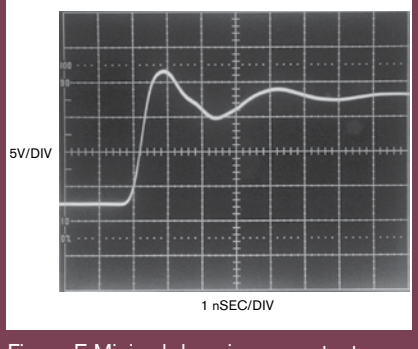


Figure E Minimal damping accentuates rise time, although pulse-top ringing is excessive.

This instrument also has a versatile trigger output, permitting continuous trigger-time phase adjustment from before to after the main output. External-trigger impedance, polarity, and sensitivity are also variable. The output, which a stepped attenuator controls, puts a clean ±10V pulse into 50Ω in 800 psec.

A potential problem with older instruments is availability. As such, Figure A shows a circuit for producing subnanosecond-rise-time pulses. Rise time is 400 psec, with adjustable pulse amplitude. Output pulse occurrence is settable from before to after a trigger output. This circuit uses an avalanche pulse generator to create extremely fast rise-time pulses.

Q_1 and Q_2 form a current source that charges the 1000-pF capacitor. When the LTC1799 clock is high (Trace A, Figure B), both Q_3 and Q_4 are on. The current source is off, and Q_2's collector (Trace B) is at ground. C_1's latch input prevents it from responding, and its output remains high. When the clock goes low, C_1's latch input is disabled and its output drops low. The Q_3 and Q_4 collectors lift, and Q_2 comes on, delivering constant current to the 1000-pF capacitor (Trace B). The resulting linear ramp is applied to C_1's and C_2's positive inputs. C_2, biased from a potential derived from the 5V supply, goes high 30 nsec after the ramp begins, providing the "trigger output" (Trace C) via its output network. C_1 goes high when the ramp crosses the

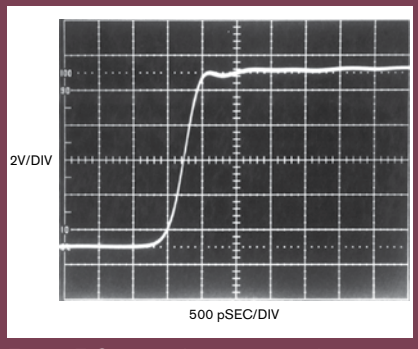


Figure F Optimal damping retards pulse-top ringing while preserving rise time.

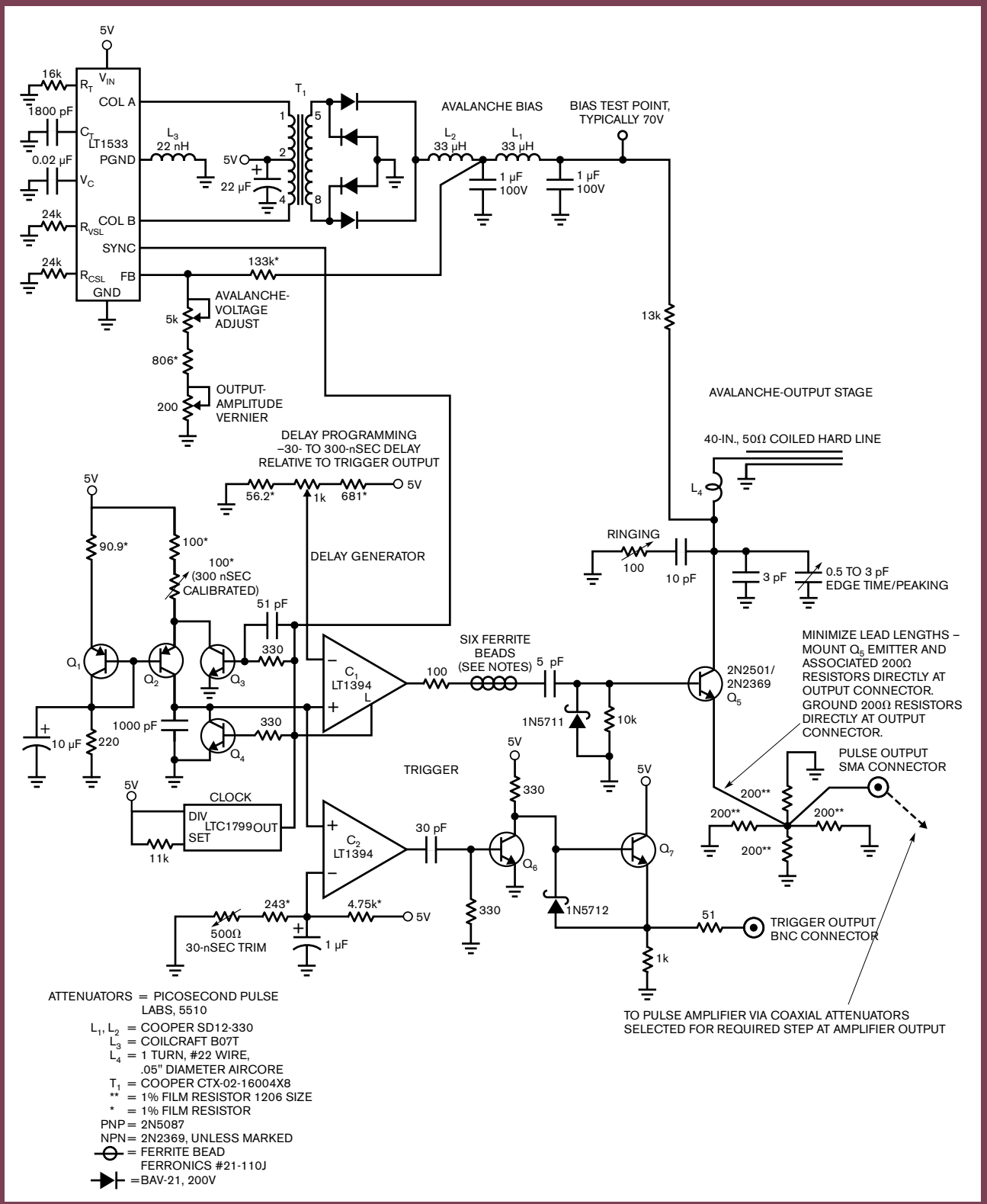


Figure A Variable delay triggers a less-than-1-nsec-rise-time pulse generator. The charge line at Q_5's collector determines an approximately 10-nsec output width. The output-pulse occurrence is settable from before to after the trigger output.

potentiometer-programmed delay at its negative input, in this case, about 170 nsec. C_1 goes high, triggering the avalanche-based output pulse (Trace D). This arrangement permits the delay programming control to vary output-pulse occurrence from 30 nsec before to 300 nsec after the trigger output. Figure C shows the output pulse (Trace D) occurring 25 nsec before the trigger output. All other waveforms are identical to those in Figure B.

When you apply C_1's output pulse to Q_5's base, it avalanches. The result is a quickly rising pulse across Q_5's emitter-termination resistor. The collector capacitors and the charge line discharge, Q_5's collector voltage falls, and breakdown ceases. The collector capacitors and the charge line then recharge. At C_1's next pulse, this action repeats. The capacitors supply initial pulse response, with the charge lines' prolonged discharge contributing the pulse body. The 40-in. charge line forms an output pulse width about 12 nsec in duration.

Avalanche operation requires high voltage bias. The LT1533 low-noise switching regulator and associated components supply this high voltage. The LT1533 is a push-pull output switching regulator with controllable transition times. Output harmonic content, or "noise," is notably reduced with slower switch transitions. Resistors at the R_{CSL} and R_{VSL} pins, respectively, control switch current and voltage-transition times. In all other respects, the circuit behaves as a classical push-pull, step-up converter.

Circuit optimization begins by setting the output-amplitude vernier to maximum and grounding Q_4's collector. Next, set the avalanche-voltage adjust so free-running pulses appear only at Q_5's emitter, noting the bias test points' voltage. Readjust the avalanche-voltage adjust 5V below this voltage and unground Q_4's collector. Set the 30-nsec trim so the trigger output goes low 30 nsec after the clock goes low. Adjust the delay-programming control to maximum and set the 300-nsec calibration, so C_1 goes high 300 nsec after the clock goes low. Slight interaction between the 30- and 300-nsec trims may require repeating their adjustments until both points are calibrated.

Q_5 requires selection for optimal avalanche behavior. The manufacturer does not guarantee such behavior, although characteristic of the device specified. A sample of 30 2N2501s, over a 17-year date-code span, yielded approximately 90%. All good devices switched in less than 475 psec, with some switching in less than 300 psec. In practice, you should select Q_5 for in-circuit rise time less than 400 psec. Then, optimize the output-pulse shape by adjusting Q_5's collector damping trims, including edge time/peaking and ringing.

The trims are somewhat interactive but not unduly so, and optimal adjustment converges nicely. The pulse edge is carefully adjusted so that the design attains maximum transition speed with minimal sacrifice of pulse purity. Figure D through Figure F detail the optimization procedure. In Figure D, the trims are set for significant effect, resulting in a reasonably clean pulse but sacrificing rise time. Figure E represents the opposite extreme. Minimal trim effect accentuates rise time but promotes post-transition ring. Figure F's compromise trimming is more desirable. This approach only slightly reduces edge rate but significantly slows post-transition ring, resulting in a 400-psec rise time with high pulse purity.

ABOUT LOW-IMPEDANCE PROBES: WHEN TO ROLL YOUR OWN AND WHEN TO PAY THE MONEY

Z_0 (low-impedance) probes provide the most faithful high-speed-probing mechanism available for low source impedances. Their less-than-1-pf input capacitance and near ideal transmission characteristic make them the first choice for high-bandwidth oscilloscope measurement. Their deceptively simple operation invites do-it-yourself construction, but numerous subtleties mandate difficulty for prospective constructors. Arcane parasitic effects introduce errors as speed increases beyond about 100 MHz with a rise time of 3.5 nsec. The selection and integration of probe materials and the probes' physical incarnation require extreme care to obtain high fidelity at high speed. Additionally, the probe must include some form of adjustment to compensate for small, residual parasitics. Finally, the design must maintain true coaxiality when fixturing the probe at the measurement point, implying a high-grade, readily disconnectable, coaxial connection capability.

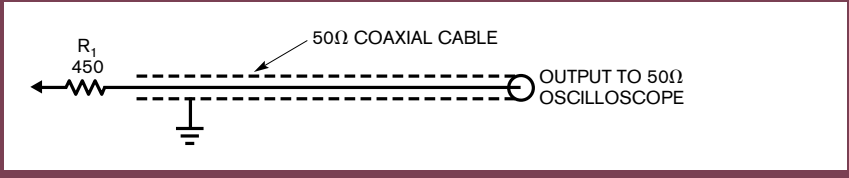


Figure A A conceptual, 500Ω, Z_0, 10× oscilloscope probe. If $R_1 = 4950\Omega$, 5-kΩ input resistance with 100× signal attenuation results. Terminated into 50Ω, the probe theoretically constitutes a distortionless transmission line. The do-it-yourself probes suffer uncompensated parasitics, causing unfaithful response above approximately 100 MHz.

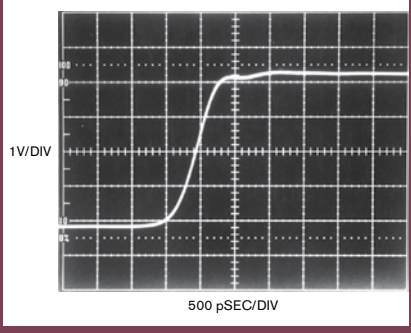


Figure B A 700-psec-rise-time pulse observed via a 50Ω line and coaxial attenuator has good pulse-edge fidelity with controlled post-transition events.

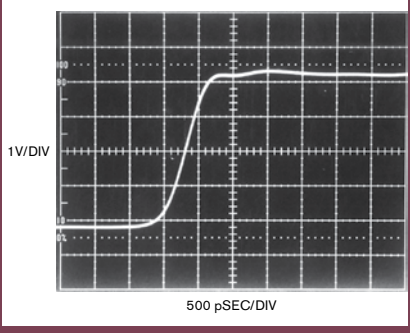


Figure C **Figure B**'s pulse viewed with a Tektronix low-impedance 500Ω P-6056 probe introduces barely discernible error.

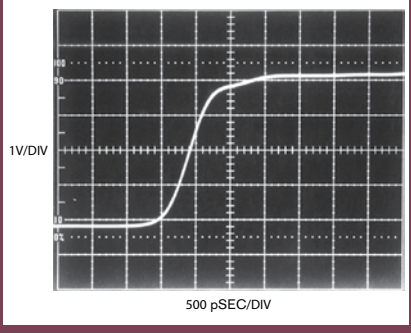


Figure D Do-it-yourself Z_0 Probe 1 introduces pulse-corner rounding, likely due to resistor/cable parasitic terms or incomplete coaxiality. Probes of this type typically manifest this type of error at rise times of less than 2 nsec.

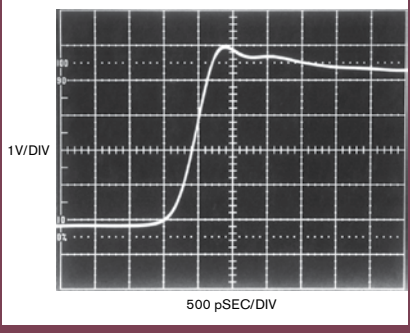


Figure E Do-it-yourself Z_0 Probe 2 has overshoot, again likely due to resistor/cable parasitic terms or incomplete coaxiality. At these speeds, don't do it yourself.

Figure A shows that a Z_0 probe is basically a voltage-divided-input 50Ω transmission line. If R_1 equals 450Ω, 10× attenuation and 500Ω input resistance result. R_1 with a value of 4950Ω causes a 100× attenuation with 5-kΩ input resistance. The 50Ω line theoretically constitutes a distortioness transmission environment. The apparent simplicity seemingly permits do-it-yourself construction, but this section's remaining figures demonstrate a need for caution.

Figure B establishes a fidelity reference by measuring a clean 700-psec-rise-time pulse using a 50Ω line terminated via a coaxial attenuator, with no probe employed. The waveform is singularly clean and crisp with minimal edge and post-transition aberrations. Figure C depicts the same pulse with a commercially produced 10× Z_0 probe in use. The probe is faithful, and there is barely discernible error in the presentation. Figures D and E, taken with two separately constructed do-it-yourself Z_0 probes, show errors. In Figure D, Probe 1 introduces pulse front-corner rounding; probe 2 in Figure E causes pronounced corner peaking. In each case, some combination of resistor/cable parasitics and incomplete coaxiality are likely responsible for the errors. In general, do-it-yourself Z_0 probes cause these types of errors beyond about 100 MHz. At higher speeds, if waveform fidelity is critical, it's best to pay the money.

VERIFYING RISE-TIME-MEASUREMENT INTEGRITY

Any measurement requires the experimenter to ensure measurement confidence. Some form of calibration check is always in order. High-speed time-domain measurement is particularly prone to error, and various techniques can promote measurement integrity.

Figure A's battery-powered 200-MHz crystal oscillator produces 5-nsec markers, useful for verifying oscilloscope-time-base accuracy. A 1.5V AA cell supplies the LTC3400 boost regulator, which produces 5V to run the oscillator. The device delivers the oscillator output to the 50Ω load via a peaked attenuation network, which provides well-defined 5-nsec markers (Figure B) and prevents overdriving low-level sampling-oscilloscope inputs.

Once you confirm time-base accuracy, it is necessary to check rise time. This measurement should include the lumped signal-path rise time, including attenuators, connections, cables, probes, and oscilloscope. Such end-to-end rise-time checking is an effective way to promote meaningful results. A guideline for ensuring accuracy is to have a four-times-faster measurement-path rise time than the rise time of interest. Thus, the 400-psec-rise-time measurement in Figure F from the sidebar, "Less-than-1-nsec-rise-time pulse generators for

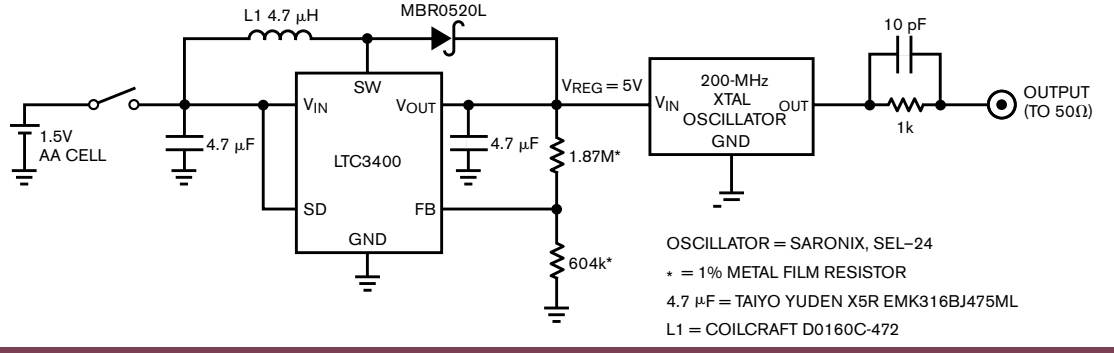


Figure A A 1.5V-powered, 200-MHz crystal oscillator provides 5-nsec time markers. A switching regulator converts 1.5 to 5V to the power oscillator.

TABLE A PICOSECOND EDGE GENERATORS ARE SUITABLE FOR RISE-TIME VERIFICATION

MANUFACTURER	MODEL	RISE TIME	AMPLITUDE	AVAILABILITY	COMMENTS
Avtech	AVP2S	40	0 to 2V	Current production	Free-running or triggered operation, 0 to 1 MHz
Hewlett-Packard	213B	100	≈175 mV	Secondary market	Free-running or triggered operation to 100 kHz
Hewlett-Packard	1105A/ 1108A	60	≈200 mV	Secondary market	Free-running or triggered operation to 100 kHz
Hewlett-Packard	1105A/ 1106A	20	≈200 mV	Secondary market	Free-running or triggered operation to 100 kHz
Picosecond Pulse Labs	TD1110C/ TD1107C	20	≈230 mV	Current production	Similar to discontinued HP1105/1106/8A
Stanford Research Systems	DG535 OPT 04A	100	0.5 to 2V	Current production	Must be driven with stand-alone pulse generator
Tektronix	284	70ps	≈200 mV	Secondary market	50-kHz repetition rate, pretrigger 75 to 150 nsec before main output, calibrated 100-MHz and 1-GHz sine-wave auxiliary outputs.
Tektronix	111	500	≈±10V	Secondary market	Outputs 30 to 250 nsec, pretrigger output, external-trigger input, pulse width set with charge lines
Tektronix	067-0513-00	30	≈400 mV	Secondary market	60-nsec pretrigger putput, 100-kHz repetition rate
Tektronix	109	250	0V to ±55V	Secondary market	≈600-Hz repetition rate, positive or negative outputs, pulse width set by charge lines

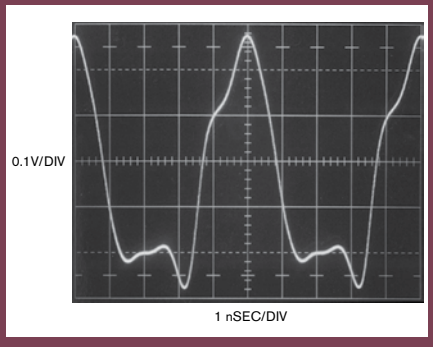


Figure B A time-mark generator output terminates into 50Ω. A peaked waveform is optimal for verifying time-base calibration.

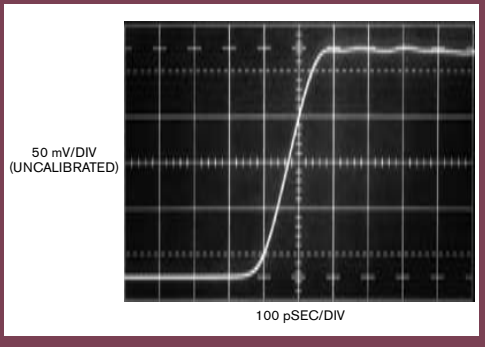


Figure C A 20-psec step produces an approximately 140-psec probe/oscilloscope rise time.

the rich and poor" requires a verified 100-psec-measurement-path rise time to support it. Verifying the 100-psec-measurement-path rise time, in turn, necessitates a 25-psec-rise-time test step. Table A lists some very fast edge generators for rise-time checking.

The Hewlett-Packard 1105A/1106A, specified at 20-psec rise time, verified the measurement signal path in Figure C from the sidebar, "How much bandwidth is enough?" Figure D indicates a 140-psec rise time, promoting measurement confidence.

ANOTHER WAY TO DO IT

An elegantly simple alternative method for generating the fast-rise 1A pulse is available. The Tektronix type 109 mercury-wetted reed-relay-based pulse generator puts a 50V pulse into 50Ω (1A) in 250 psec. An externally connected charge line with an approximate scale factor of 2 nsec/ft sets the pulse width. Figure A, a simplified schematic, shows type 109 operation. When the relay contacts close, the charge line discharges via the 50Ω-diode path. The pulse extends until the line depletes; depletion time depends on line length. The relay structure is arranged to assume wideband, 50Ω characteristics. Figure B shows the result. The 109 drives the monitoring 1-GHz oscilloscope to its 350-psec-rise-time limit with a 50V high-fidelity pulse.

Operating restrictions include finite relay life of approximately 200 hours; obtaining the instrument, which has been out of production for more than 20 years; difficulty in observing its low-frequency output on some oscilloscopes; and test-fixture-layout sensitivity due to the 250-psec rise time. Additionally, the faster rise time may not approximate actual circuit operating conditions as closely as the main article's 2-nsec circuit.

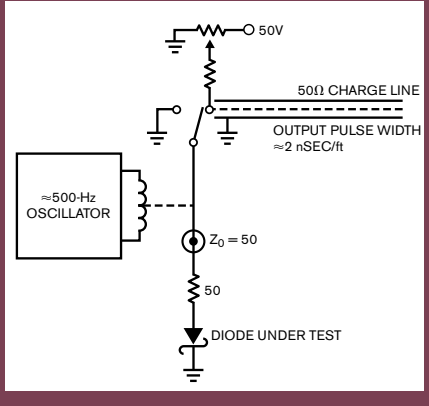


Figure A When right-side contacts close, the charge line discharges into a 50Ω diode load. Strict attention to construction allows wideband, 50Ω characteristics, permitting a 250-psec rise time and a high-purity output pulse.

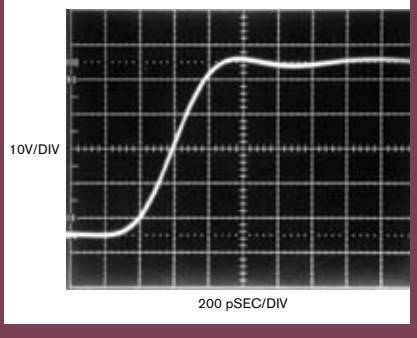


Figure B Tektronix type 109 produces a high-purity, 50V, 1A pulse, driving the monitoring 1-GHz oscilloscope to its 350-psec-rise-time limit.

BY JIM WILLIAMS • LINEAR TECHNOLOGY

MEASURING WIDEBAND-AMPLIFIER SETTLING TIME

A NOVEL CIRCUIT LETS YOU MEASURE OUTPUT SETTLING TO 0.1% IN 2 nSEC.

You use wideband amplifiers in instrumentation, waveform-synthesis, data-acquisition, and feedback-control systems. To ensure a robust design for these systems, you must verify precision operation at high speeds. This requirement presents a difficult measurement challenge. Wideband operational amplifiers feature dc precision of 0.2-mV offset voltage with gain-bandwidth products of 400 MHz and slew rates of 2500V/µsec (**Reference 1**). IC designers face a trade-off between fast slew rates and short ring times. Fast-slewing amplifiers generally have extended ring times. This combination complicates your amplifier choice and the frequency compensation you use (see **sidebar** "Practical considerations for amplifier compensation"). Additionally, the architecture of very fast amplifiers usually dictates trade-offs, which degrade dc-error terms.

SETTLING TIME DEFINED

It is relatively easy for you to verify amplifier dc specifications. Literature defines the measurement techniques you use. You need to use more sophisticated approaches to produce reliable ac specifications. Measuring anything at any speed requires care. Dynamic measurements are particularly challenging, and amplifier settling time is difficult to determine (**references 2** through **7**).

Settling time is the elapsed time from an input application until the output arrives at and remains within a specified error band around the final value. Amplifier manufacturers usually specify it over a full-scale transition.

Settling time has three distinct components (**Figure 1**). The delay time is small and almost entirely due to the amplifier's propagation delay. No output movement occurs during this in-

terval. During slew time, the amplifier moves at its highest speed toward the final value. Ring time defines the region during which the amplifier recovers from slewing and ceases movement within some defined error band. Measuring settling times of nanoseconds requires a careful approach and experimental technique.

The traditional way for measuring settling time is with a circuit that uses the false-sum-node technique (**Figure 2**). The resistors and amplifier form a bridge network. The amplifier output steps to the input voltage when you drive the input, assuming that the circuit is using ideal resistors. During the slew period, the diodes bound the settle node, limiting the voltage excursion. When settling occurs, the oscilloscope's probe voltage should be 0V. The resistor divider's attenuation causes the probe's output to be one-half of the settled voltage.

In theory, this circuit should allow you to observe fast settling to small amplitudes. In practice, you cannot rely on it to produce useful measurements. The circuit has several flaws, including a requirement for the input pulse to have a flat top within the required measurement limits. Typically, you are interested in settling of less than 5 mV for a 5V step. No general-purpose pulse generator holds the output amplitude and noise within these limits. You cannot distinguish between generator-caused aberrations and amplifier-related ones.

The oscilloscope connection also presents problems. As probe capacitance rises, the ac loading of the resistor junction influences the observed settling waveforms. The excessive input capacitance of 1× probes makes them unsuitable for this measurement. A 10× probe's attenuation sacrifices oscilloscope gain, yet its 10-pF input capacitance still introduces a significant lag at nanosecond speeds. If you use an active 1×, 1-pF FET (field-effect-transistor) probe, it largely alleviates this problem, but a more serious issue remains.

You use clamp diodes at the settle node to reduce the voltage swing during amplifier slewing. This approach is intended to prevent the circuit from overdriving the oscilloscope input. Unfortunately, the 400-mV drop across the Schottky diodes means that the oscilloscope will undergo an unacceptable overload (**Reference 8**). Oscilloscopes' overdrive-recovery characteristics vary widely among models and brands, and manufacturers typically do not specify it. At 0.1% resolution, the oscilloscope typically undergoes a 10-times overdrive at 10 mV/division, making the desired 2.5-mV baseline unattainable.

AT A GLANCE

- It is difficult to measure the settling time of fast amplifiers.
- One method of measurement is to use an old analog sampling oscilloscope.
- This circuit uses a current-steering bridge and an analog multiplier IC.
- The two methods correlate well.
- The measurement limits are 2 mV and 2 nsec.

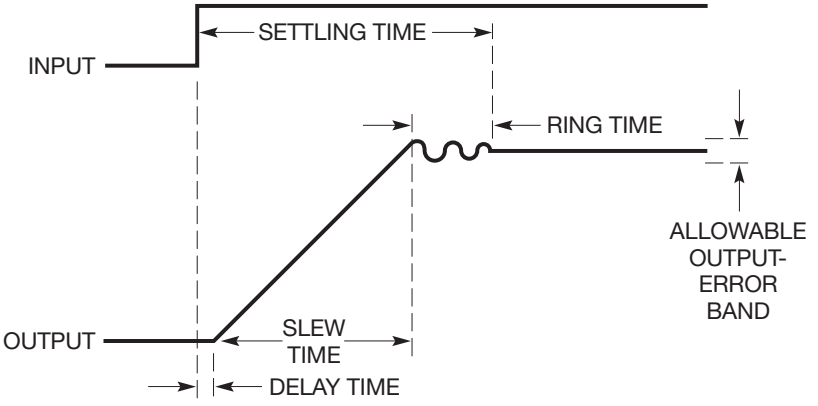


Figure 1 The components of settling time include delay, slew, and ring times. Using fast amplifiers reduces slew time, although longer ring time usually results.

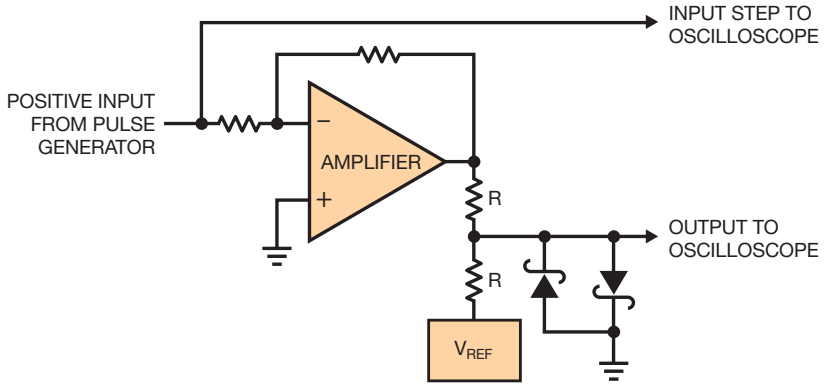


Figure 2 A popular summing scheme for settling-time measurement provides misleading results with fast amplifiers.

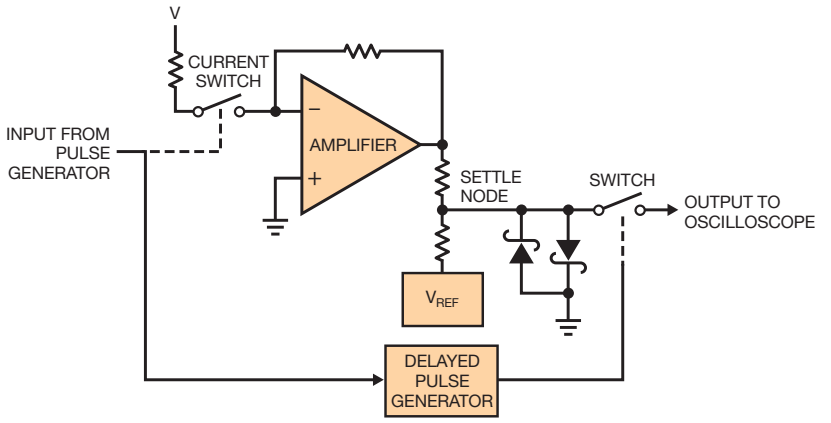


Figure 3 The proposed circuit's conceptual arrangement is insensitive to pulse-generator aberrations and eliminates oscilloscope overdrive. The input switch gates a current step to the amplifier under test. A delayed-pulse generator controls a second switch, which prevents the oscilloscope from monitoring the settle node until settling is nearly complete.

With this arrangement, the measurement becomes hopeless at nanosecond speeds.

Thus, your measuring wideband amplifier settling time requires an oscilloscope that is somehow immune to overdrive as well as a flat-top pulse generator. The only oscilloscope technology that offers inherent overdrive immunity is the classic analog sampling oscilloscope. Do not confuse these scopes with modern digital sampling oscilloscopes that have overdrive restrictions (**Reference 8**). Several documents explain the operation of classic sampling oscilloscopes (**references 9** through **13**). Although you can buy these instruments used, their manufacturers no longer make them. You can, however, construct a circuit that borrows the overload advantages of classic analog-sampling-oscilloscope technology. You can also endow the circuit with features for measuring nanosecond settling times.

You can avoid the flat-top-pulse-generator requirement by switching current rather than voltage. It is easier to gate a quickly settling current into the amplifier's summing node than to control a voltage. This approach eases the input pulse generator's job, although it still must have a rise time of approximately 1 nsec to avoid measurement errors.

PRACTICAL MEASUREMENT

A circuit that can measure wideband-amplifier settling time shares attributes

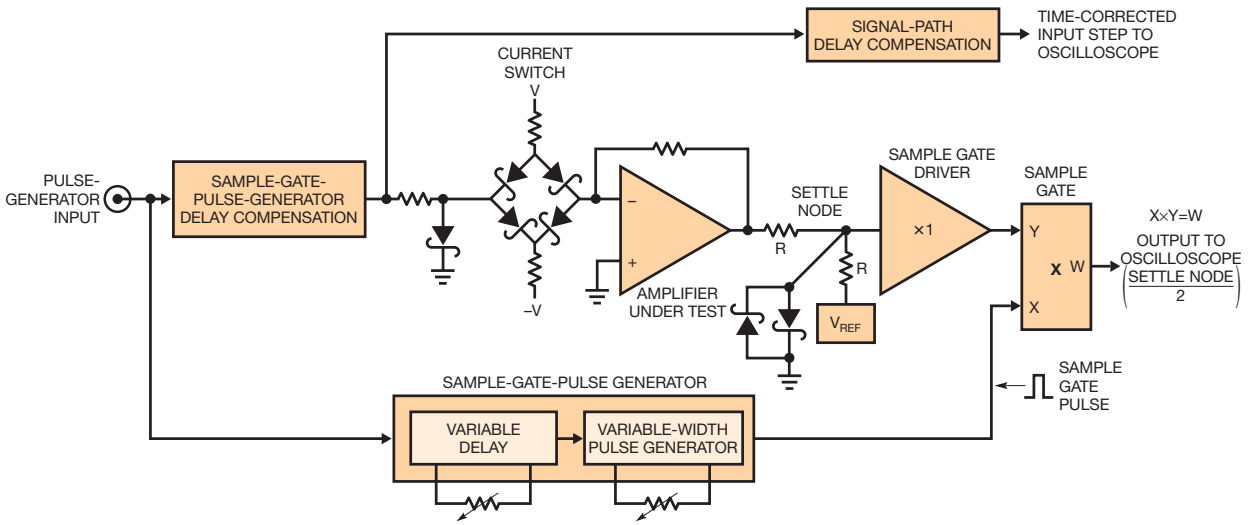


Figure 4 The diode bridge cleanly switches input current to the amplifier. A multiplier-based sampling switch eliminates the signal's presettling excursion. You compensate the input-step time reference and sample-gate-pulse generator for any circuit delays.

with the classic method, although some new features appear (**Figure 3**). The oscilloscope connects to the settle point by a switch. You determine the switch's state by triggering a delaying pulse generator from the input pulse. You arrange the delayed pulse generator's timing so that the switch does not close until settling is nearly complete. In this way, you sample the incoming waveform in both time and amplitude. No off-screen activity occurs on the oscilloscope; hence, you never subject the oscilloscope to overdrive.

You control the switch at the amplifier's summing junction with the input pulse. This switch gates current to the amplifier through a voltage-driven resistor. This approach eliminates the requirement for a flat-top pulse generator, although the switch must be fast and devoid of drive artifacts.

THE SAMPLE-GATE MULTIPLIER IC MUST PASS WIDEBAND-SIGNAL-PATH INFORMATION WITHOUT INTRODUCING ALIEN COMPONENTS.

For more detail, you split the delayed pulse generator into a delay block and a pulse generator, which you can vary independently (**Figure 4**). The input step to the oscilloscope runs through a section that compensates for the propagation delay of the settling time's measurement path. Similarly, another delay compensates the sample gate's pulse-generator propagation delay. This delay causes a phase-advanced version of the pulse that triggers the amplifier under test to drive the sample gate's pulse generator. This approach improves minimum measurable settling time by making irrelevant the sample gate's pulse-generator propagation delay.

The most striking new aspects of **Figure 4**'s circuit are the diode bridge switch and the multiplier IC. The diode bridge's balance combines with matched, low-capacitance Schottky diodes and high-speed drive to yield clean switching. The bridge quickly switches current into the amplifier's summing point, with settling time within 1 nsec. The diode clamp to ground prevents excessive bridge-drive swings and ensures that nonideal input-pulse characteristics are nearly irrelevant.

The sample-gate multiplier IC has stringent requirements. It must faithfully pass wideband-signal-path information without introducing alien components, particularly those deriving from the switch-command channel that provides the sample-gate pulse. Conventional choices for the sample-gate switch would include FETs or a sampling diode bridge. But FETs' parasitic gate-to-channel capacitances would result in large gate-drive-originated feedthrough into the signal path. For almost all FETs, this feedthrough is many times larger than the signal you are observing and would induce oscilloscope overload and obviate the switch's purpose. The diode bridge is better; its small parasitic capacitances tend to cancel, and its symmetrical, differential structure results in low feedthrough. Practically, however, the bridge requires dc and ac trims and complex drive and support circuitry (**references 3**, **4**, **7**, and **14**).

To avoid these problems, the sample-gate multiplier IC functions as a wideband high-resolution switch with low feedthrough. The great advantage of this approach is that you can maintain the switch-control channel inband. You hold the transition rate within the multiplier IC's 250-MHz bandpass. The multiplier's wide bandwidth means that you always control the switch command's transition. There are no out-of-band responses, greatly reducing feedthrough and parasitic artifacts.

SETTLING-TIME CIRCUITRY

You let the input pulse switch the input bridge through a delay network of inverters, A, and a driver stage comprising similar inverters, C (**Figure 5**). The delay compensates the sample-gate pulse generator's delayed response. This step ensures that the sample gate's pulse can occur immediately after the end of the amplifier under test's slew time. You choose the delay range so that the sample-gate pulse can occur before the amplifier slews. This capability is unused in normal operation, although it guarantees that you will always be able to

capture the settling interval.

The C inverters form a noninverting driver stage you use to switch the diode bridge. You adjust various trims to optimize the driver output pulse shape (see **sidebar** "Settling-time circuit-trimming procedures" with the Web version of this article at www.edn.com/100812df). This approach provides a clean, fast impulse to the diode bridge. This high-fidelity pulse is devoid of undamped components. It prevents radiation and disruptive ground currents from degrading the measurement noise floor. The driver also activates the B inverters, which supply a time-corrected input step to the oscilloscope.

THE PULSE IS DEVOID OF UNDAMPED COMPONENTS AND PREVENTS RADIATION FROM DEGRADING THE MEASUREMENT NOISE FLOOR.

The driver's output pulse transitions through the 1N5712 diode clamp's forward-voltage potential in less than 1 nsec. This transition causes an essentially instantaneous switching of the diode bridge. The cleanly settling current into the amplifier under test's sum-

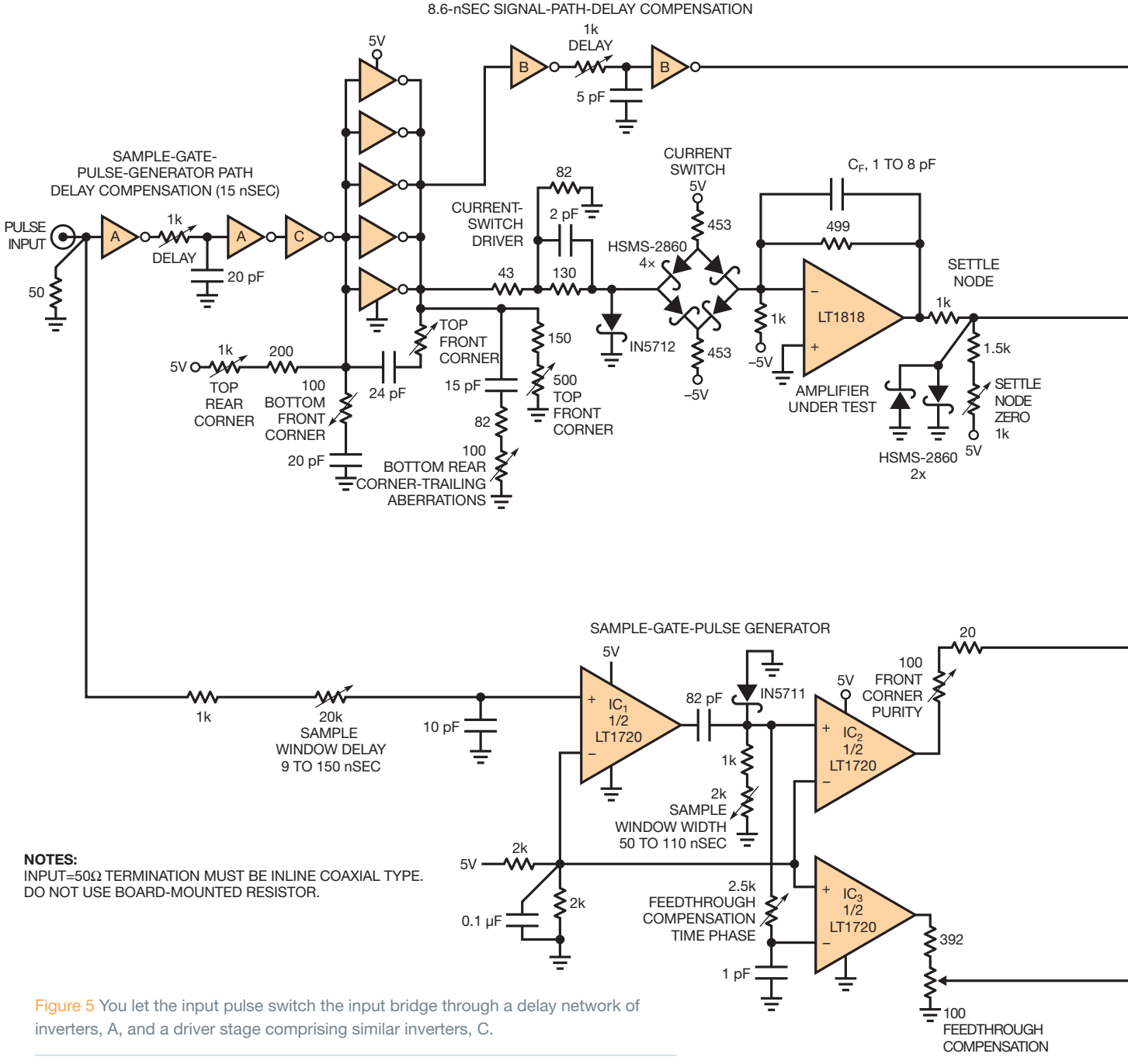
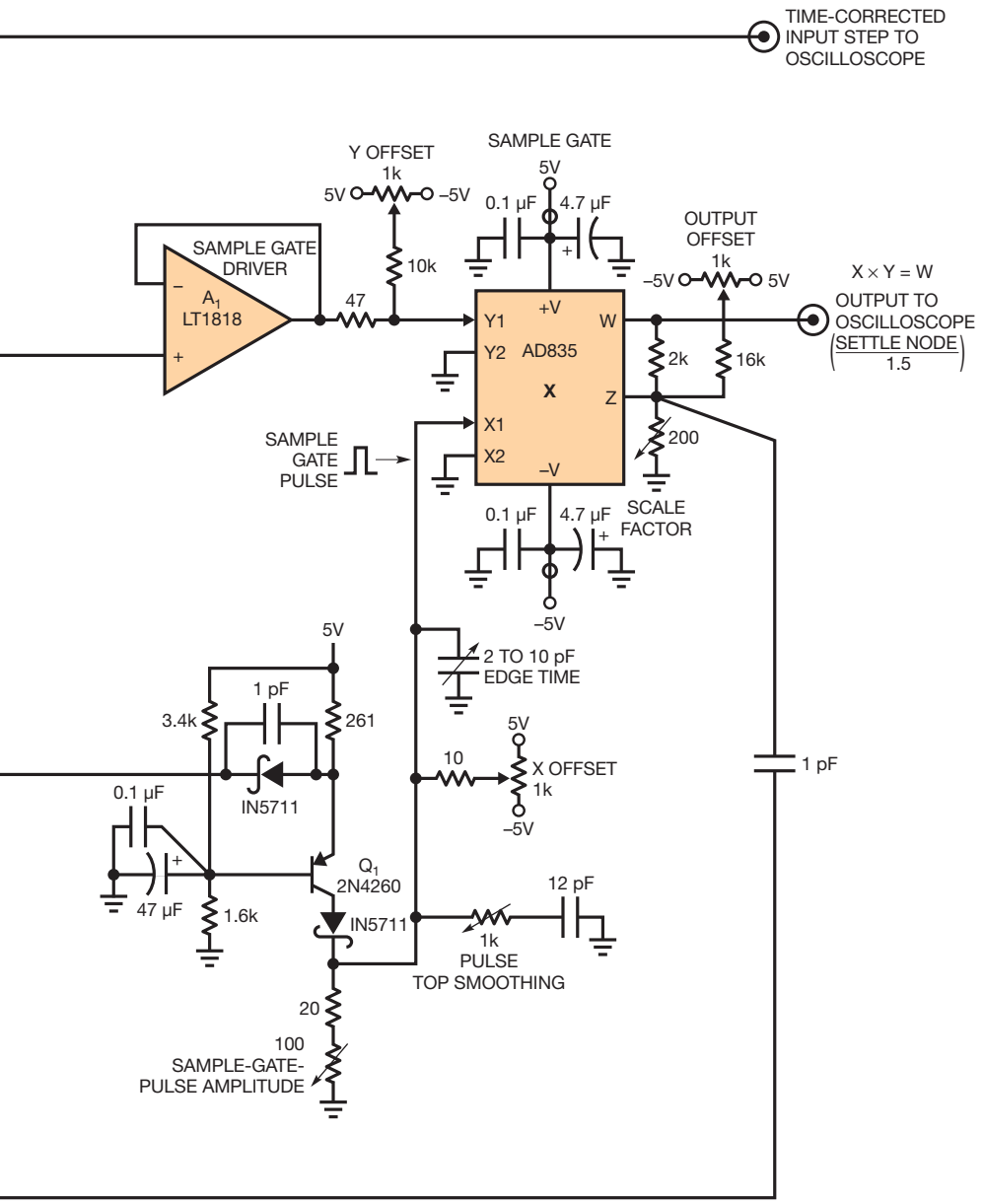


Figure 5 You let the input pulse switch the input bridge through a delay network of inverters, A, and a driver stage comprising similar inverters, C.

ming point causes a proportionate amplifier output movement. You set up a negative bias current at the amplifier's summing point with a 1-kΩ resistor pulled to −5V. That current combines with the input current step to produce a −2.5 to +2.5V amplifier output transition. You feed this amplifier's output to a voltage divider biased to 5V. You adjust the potentiometer to a nominal 500Ω so that when the amplifier under test transitions to −2.5V, the node clamped by the two Schottky diodes transitions to 0V. Buffer amplifier A_1 unloads this clamped settle node and provides the settling-time signal to the AD835 multiplier IC.

The other signal path to the multiplier IC uses a 20-kΩ potentiometer to set a delay time of the input pulse. This potentiometer feeds three comparators, and you use a 2-kΩ potentiometer to set the delayed pulse width. This step sets the sample gate's on-time. The Q_1 stage forms the sample gate's pulse into a clean, fast rise time. This technique furnishes pure, calibrated-amplitude, on/off switching instructions to the sample gate's multiplier IC. Appropriate setting of the sample gate's pulse delay means that the oscilloscope will not see any input until settling is nearly complete, eliminating oscilloscope overdrive. You adjust the sample window's pulse width so that you can observe all the remaining settling activity. In this way, the oscilloscope's output is reliable, and you can take meaningful data.



PERFORMANCE RESULTS

The circuit performs admirably (**Figure 6**). Trace A is the time-corrected input pulse, Trace B is the amplifier's output, Trace C is the sample gate's pulse, and Trace D is the settling-time output. When you interpret the waveform placement, note that Trace B appears time-skewed relative to time-corrected Trace A. This skew accounts for Trace B's false movement before Trace

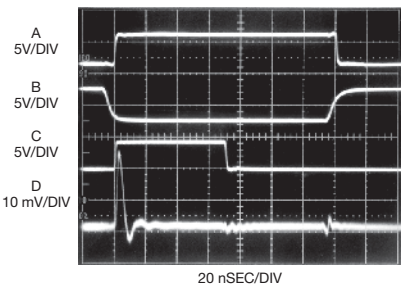


Figure 6 The settling-time circuit's waveforms include the time-corrected input pulse (Trace A), amplifier under test's output (Trace B), sample gate's trace (Trace C), and settling-time output (Trace D). You can vary the sample-gate window's delay and width. Trace B appears time-skewed relative to the time-corrected Trace A.

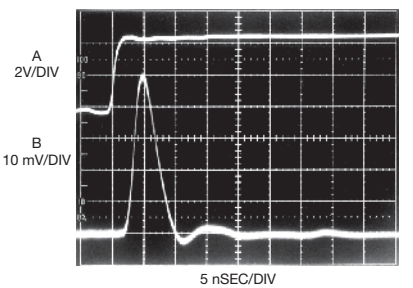


Figure 7 By expanding the vertical and horizontal scales, you can see the 9-nsec amplifier settling to within 5 mV (Trace B). Trace A is the time-corrected input step.

A's ascent. When the sample gate's pulse goes high, the sample gate switches cleanly. You can easily observe the last 20 mV of the amplifier's slewing. You can also see the entire ring time and the amplifier settling nicely to a final value. When the sample gate's pulse goes low, the sample gate switches off with only 2 mV of feedthrough. No off-screen activity occurs at any time, and you never subject the oscilloscope to overdrive.

You can adjust the vertical and horizontal scales of the oscilloscope to make the settling details more visible (**Figure 7**). You measure settling time from the onset of the time-corrected input pulse. Additionally, you calibrate the settling signal's amplitude with respect to the

PRACTICAL CONSIDERATIONS FOR AMPLIFIER COMPENSATION

There are a number of practical considerations when you compensate the amplifier to get the fastest settling time (see Figure 1 in the main text). Once you choose an amplifier, the only settling variable you can change is the ring time by changing the amplifier's compensation network. Because slew time is usually the dominant lag, it is tempting to select the fastest-slewing amplifier available. Unfortunately, fast-slewing amplifiers usually have extended ring times, which negate their speed advantage. If you damp out the ringing with large compensation capacitors, it results in protracted settling times.

The key to good settling times is to choose an amplifier with the right balance of slew rate and recovery characteristics and then properly compensate it. This is harder than it sounds because you can't predict amplifier settling time or extrapolate it from any combination of data-sheet specifications. You must measure settling time in the intended configuration.

A number of terms combine to influence settling time. They include amplifier slew rate and ac dynamics, layout capacitance, source resistance and capacitance, and the compensation capacitor. These terms interact in a complex manner, making predictions hazardous. Spice aficionados should take notice. If you replace the parasitic components with a purely resistive source, you still can't readily predict amplifier settling time. The parasitic-impedance terms make a difficult problem messier.

The only way to deal with the parasitic terms is to adjust the feedback compensation capacitor, C_F. When you properly adjust the value of C_F, it rolls off the amplifier's gain at the frequency that permits the best dynamic response. You achieve the best settling results when you select the capacitor to functionally compensate for all the terms (Figure A).

Trace A is the time-corrected input pulse, and Trace B is the amplifier's settle signal. The amplifier comes cleanly out of slew and settles to 5 mV in 9 nsec. The sample gate opens just after the second vertical division. The waveform signature is tight and nearly critically damped. When you use too large a feedback capacitor the settling is smooth, although overdamped (Figure B), giving you a 13-nsec penalty that results in a 22-nsec settling time. Eliminating the feedback capacitor results in a severely underdamped response with resultant excessive ring-time excursions (Figure C). Settling time goes out to 33 nsec. Using a feedback capacitor that is too small results in an underdamped response requiring

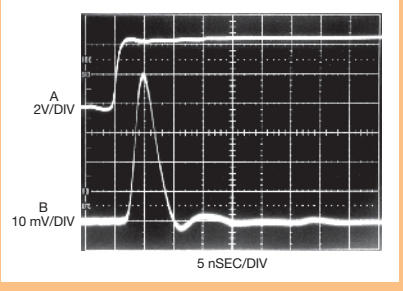


Figure A Optimizing the compensation capacitor permits a tight waveform signature, a nearly critically damped response, and a 9-nsec settling time. Trace A is the time-corrected input step. Trace B is the settle signal.

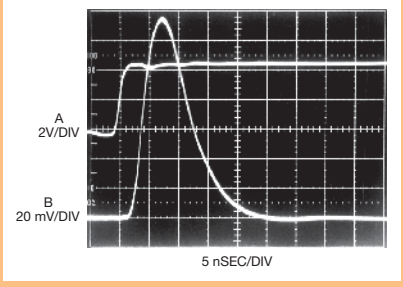


Figure B This overdamped response ensures freedom from ringing, even with component variations in production. The penalty is a 22-nsec settling time. Note the two-times vertical-scale change versus that of Figure A.

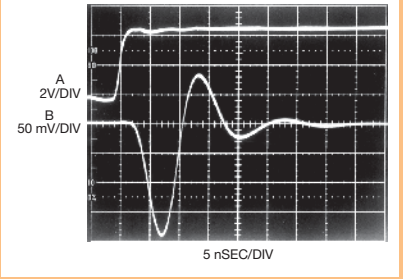


Figure C This severely underdamped response is due to the lack of a feedback capacitor. Note the five-times vertical-scale change versus that of Figure A. Settling time is 33 nsec.

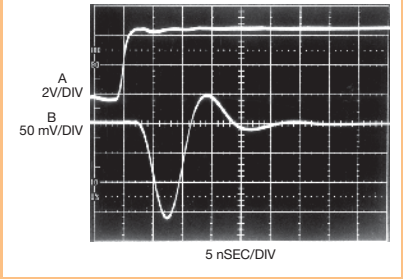


Figure D An underdamped response results from an undersized capacitor. Component-tolerance budgeting prevents this behavior. Note the five-times vertical-scale change versus that of Figure A. Settling time is 27 nsec.

amplifier, not the settle node. This approach eliminates ambiguity due to the settle node's resistor ratio. Trace A is the time-corrected input pulse, and Trace B is the settling output. You can easily observe the last 50 mV of slew. The amplifier settles within 5 mV, or 0.1%, in 9 nsec after you optimize the amplifier under test's feedback capacitor, C_F, (see **sidebar** "Practical considerations for amplifier compensation").

It is good practice to adjust the sampling window backward to the last 50 mV or so of amplifier slewing. This step allows you to observe the onset of ring time without encountering oscilloscope overdrive. The sampling-based approach provides this capability, and it is a powerful measurement tool. Slower amplifiers may require extended delay, sampling-window times, or both. You can use larger capacitor values in the delayed pulse-generator timing networks to meet these requirements.

TO ENSURE CONFIDENCE, MAKE THE SAME MEASUREMENT WITH AN ALTERNATIVE METHOD AND SEE WHETHER RESULTS AGREE.

VERIFYING RESULTS

The sampling-based settling-time circuit appears to be a useful measurement approach. A good way to ensure confidence is to make the same measurement with an alternative method and see whether results agree.

Classic sampling oscilloscopes are inherently immune to overdrive (**Reference 8**). You can use this feature and attempt a settling-time measurement directly at the clamped settle node (**Figure 8**). The circuit heavily overdrives a Tektronix type 661 with 4S1 vertical and 5T3 timing plug-ins, but the instrument is ostensibly immune to the insult (**Figure 9**). Trace A is the time-corrected input pulse, and

27 nsec to settle (Figure D). Note that figures B, C, and D require you to reduce the vertical scale to capture the nonoptimal responses.

When you trim the feedback capacitor for optimal response, the source, stray, amplifier, and compensation-capacitor tolerances are irrelevant. If you don't use individual trimming, you must consider these tolerances to determine the feedback capacitor's production value. Stray and source capacitance and output loading, as well as the feedback capacitor's value, affect ring time. The relationship is nonlinear, although some guidelines are possible. The stray and source terms can vary by ±10%, and the feedback capacitor is typically a ±5% component. These figures assume a resistive source. If the source has substantial parasitic capacitance, such as a photodiode or a DAC, this number can easily reach ±50%. Additionally, amplifier slew rate has a significant tolerance, which the data sheet states. To obtain a production-feedback-capacitor value, you determine the optimum value by individual trimming with the production-board layout. Remember that board-layout parasitic capacitance counts too. Then, factor in the worst-case percentage values for stray- and source-impedance terms, slew rate, and feedback-capacitor tolerance. Add this information to the trimmed capacitors' measured value to obtain the production value. This budgeting is perhaps unduly pessimistic. The errors should sum in an rms (root-mean-square) fashion, not a purely additive way.

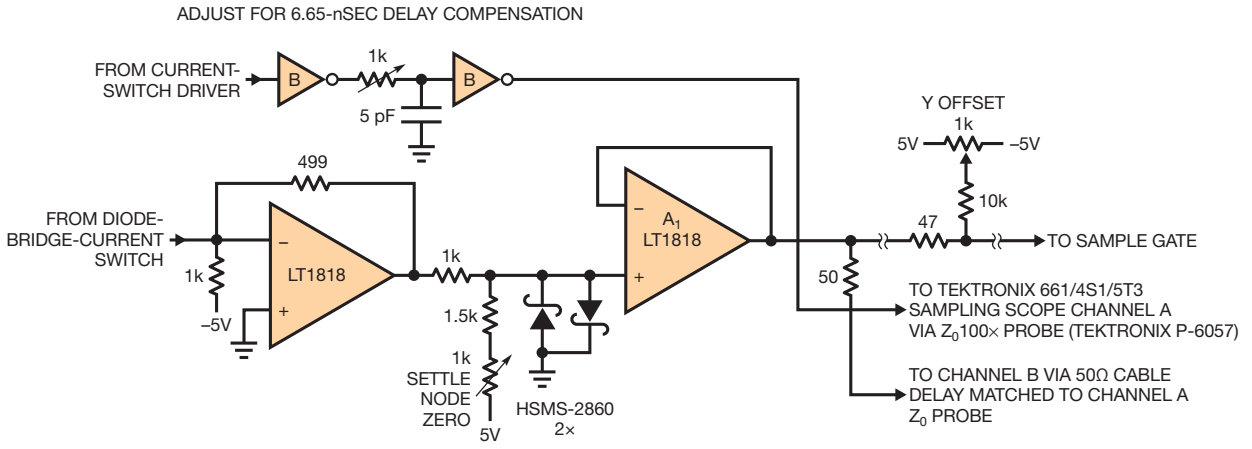


Figure 8 This alternative measurement method uses a 1-GHz Tektronix 661/4S1/5T3 sampling oscilloscope.

Trace B is the settle signal. Despite a brutal overdrive, the oscilloscope responds cleanly, giving a plausible settle signal.

You can compare the results visually (**figures 9** and **10**). Ideally, if both approaches represent good measurement technique and you properly construct them, the results should be identical. If this scenario occurs, the data produced by the two methods has a high probability of being valid.

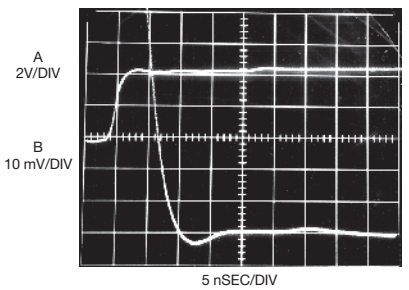


Figure 9 The measurement using a sampling oscilloscope shows a 9-nsec settling time and waveform profile, which are consistent with those of Figure 7.

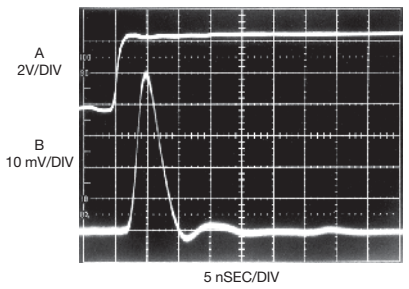


Figure 10 The settling-time measurement using the circuit of Figure 5 yields results that correlate well with those of Figure 9.

The two measurement methods do show nearly identical settling times and highly similar settling-waveform signatures. This agreement provides a high degree of credibility to the measured results. The noise floor and the signal feedthrough impose the 2-mV amplitude-resolution limit. The time resolution's limit is about 2-nsec to 5-mV settling. EDN

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AUTHOR'S BIOGRAPHY

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BY MULTIPLEXING A SMALL AC SIGNAL ON THE POWER WIRES, YOU CAN INFER WIRING LOSSES.

COMPENSATE FOR WIRING LOSSES WITH REMOTE SENSING

BY JIM WILLIAMS, JESUS ROSALES, KURK MATHEWS, AND TOM HACK • LINEAR TECHNOLOGY CORP

Wires and connectors have resistance. This simple, unavoidable truth dictates that a power source's remote load voltage is less than the source's output voltage (**Figure 1**). You could maintain the intended load voltage by raising the regulator output. Unfortunately, line resistance and load variations introduce uncertainties, thus limiting the correction accuracy. You could add a locally positioned regulator, but this approach is inefficient due to regulator losses (**Figure 2**). A classic approach uses "four-wire" remote sensing to eliminate line-drop effects (**Figure 3**). In this case, load-referred sense wires feed the power supply's sense inputs. The sense inputs' high impedance negates the sense-line-resistance effects. This scheme works well but requires dedicated sense wires, a significant disadvantage in many applications.

"VIRTUAL" REMOTE SENSING

You can eliminate the sense loads and still retain the advantages of classic four-wire remote sensing (**Figure 4**). In this case, a Linear Technology (www.linear.com) VRS (Virtual Remote Sense) IC alternates output current between 95 and 105% of the nominal required output current (**Reference 1**). The IC forces the power supply to provide a dc current plus a small square-wave current with peak-to-peak amplitude equal to 10% of the dc current. Typical systems generally require decoupling capacitor C_{LOAD} for low impedance under transient conditions. In this case, it takes on an additional role by filtering out the VRS square-wave excursions.

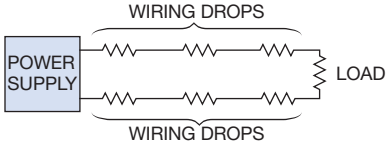


Figure 1 Wiring resistance causes output voltage to drop at the load.

You size C_{LOAD} to produce an ac short at the square-wave frequency. Thus, V_{OUTAC}, the square-wave voltage at the power supply, is equal to $0.1 \times I_{DC} \times R_W$ p-p, where I_{DC} is the square-wave current and R_W is the wire's resistance. Thus, the square-wave voltage at the power supply has a peak-to-peak amplitude equal to one-tenth the dc wiring drop. This figure represents a direct measurement—not an estimate—of wiring drop and is accurate over all load currents. The IC provides signal processing that produces a dc voltage from this ac signal. The IC introduces it into the power-supply feedback loop to provide accurate load regulation (see **sidebar** "A primer on VRS operation").

The power supply can be a linear or switching regulator, a module, or any other power source capable of variable output. You can also synchronize the power supply to the sense IC's operating frequency, which is adjustable over three decades. The sense IC has optional spread-spectrum operation to improve EMI (electromagnetic interference). The IC's 3 to 50V input range allows you to use it in many designs.

This technique employs an estimate—not a direct measurement—of load voltage, so the resultant correction is only an approximation—but a good one (**Figure 5**). In this example, load current increases from 0A until it produces a 2.5V wiring drop. Load voltage drops only 73 mV at maximum current. A voltage drop equivalent to 50% of load voltage results in only a 1.5% shift in load-voltage value. Smaller wiring drops produce even better results.

AT A GLANCE

- Wiring losses reduce the voltage at a load.
- You can add a local regulator to compensate for wiring loss, but efficiency suffers.
- By measuring the current of a small ac signal multiplexed on the output, an IC can correct for voltage drop without using sense wires.
- The technique is applicable to linear, switching, isolated, offline, and power-brick voltage regulators.

LINEAR REGULATORS

You can use VRS with a linear regulator. The IC senses current through a 0.2Ω shunt resistor (**Figure 6**). Feedback controls Q_1 with Q_2, completing a control loop. You design Q_2 in cascode to the IC's open-drain output to control a high voltage at Q_1's gate. Components at the IC's compensation pin furnish loop stability and provide good transient response. The design shows good response to load-step waveforms (**Figure 7**). Loop compensation, load capacitance, and the remote-sense IC's sampling rate determine the transient response (**Figure 8**).

You can also apply this technique to a monolithic regulator (see related **figure** in the Web version of this article at www.edn.com/101118df). This approach allows you to add current limiting and simplifies the loop compensation. The transient response is similar to that of the circuit in **Figure 6**. As before, the sense IC's low-voltage drain pin requires you to place a transistor in cascode to control the high voltage at the regulator's set pin.

SWITCHING REGULATORS

You can also design VRS into switching regulators. A flyback volt-

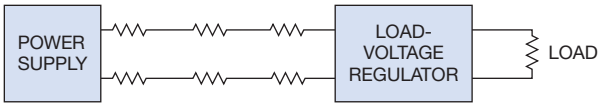


Figure 2 A local regulator solves the problem but is expensive and inefficient.

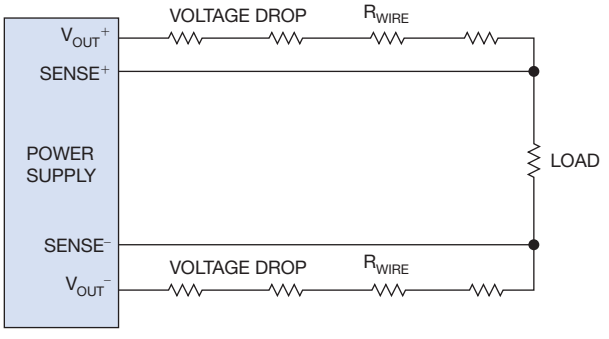
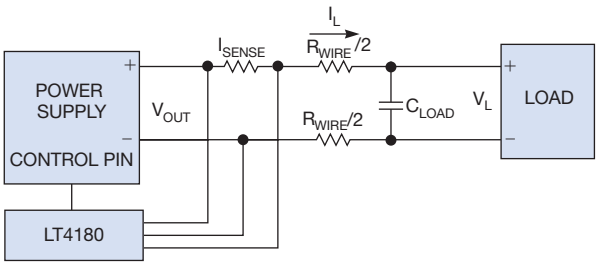


Figure 3 Sense wires can correct for the voltage drop but are complicated. Long sense wires may cause supply instability.



NOTES: THE OUTPUT VOLTAGE EQUALS DC PLUS THE SQUARE WAVE FROM THE WIRING-VOLTAGE DROP.
THE LOAD CAPACITANCE REMOVES THE SQUARE WAVE, SO THE LOAD VOLTAGE CONTAINS ONLY DC.
THE LOAD CURRENT EQUALS DC PLUS THE SQUARE WAVE.

Figure 4 A novel VRS IC compensates for the wiring-voltage drops. It multiplexes a small ac signal over the power wires so that it can calculate the wiring impedance.

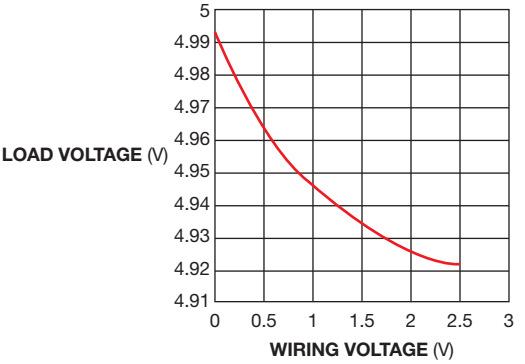


Figure 5 The IC can provide for 1.5% regulation at the load despite a 2.5V drop in the wires.

age-boost configuration has similar architecture to that of the linear examples, although the output voltage is higher than the input voltage (see related **figure** in the Web version of this article at www.edn.com/101118df). In this case, the sense IC's open-drain output is directly compatible with the boost regulator's low-voltage VC pin, so no cascode stage is necessary.

You can also design VRS into switching step-down, or buck, regulators (see related **figure** in the Web version of this article at www.edn.com/101118df). As before, you can control the VC pin of the regulator directly from the sense IC's open-drain output. You design a single-pole roll-off to stabilize the loop. The design maintains a 12V, 1.5A output from a 22 to 36V input despite a 0 to 2.5Ω wiring-drop loss.

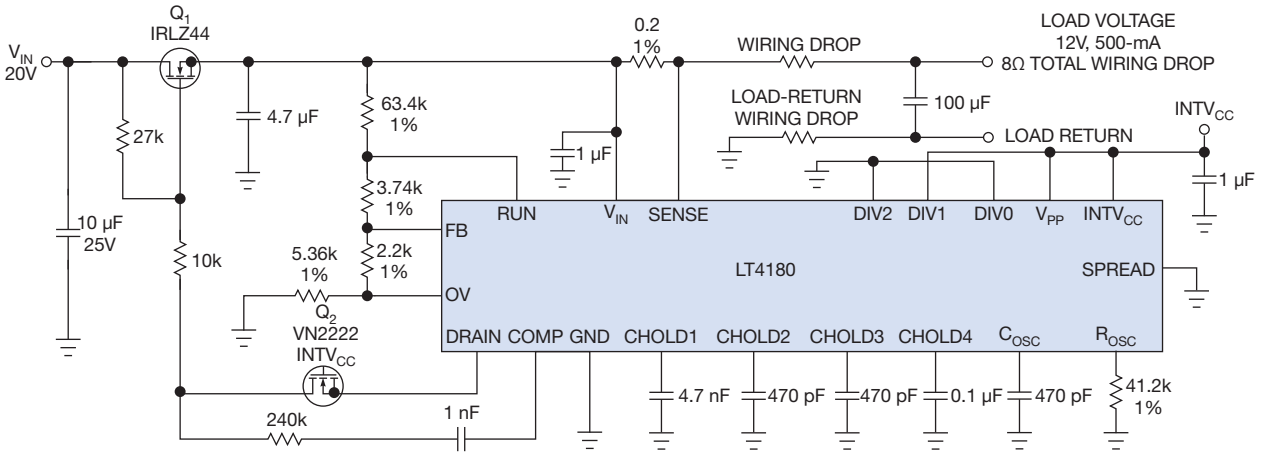
ISOLATED SUPPLIES

You can adapt the VRS approach to isolated output supplies (see related **figure** in the Web version of this article at www.edn.com/101118df). You use an approach similar to that in the previous examples to supply a fully isolated 24V output. The VRS feature accommodates a 10Ω wire resistance. The flyback-regulator IC and T_1 form a transformer-coupled power stage. You use optocoupled feedback to maintain output isolation.

You can design step-down isolated converters that incorporate remote virtual sensing (see related **figure** in the Web version of this article at www.edn.com/101118df). This 48V input to the 3.3V, 3A output has a fully isolated output. The regulator IC drives T_1 through Q_1. T_1's rectified and filtered secondary supplies output power, which the remote-sense IC corrects for line drops. You maintain isolation by transmitting the feedback signal with an optoisolator. The optoisolator's output collector ties back to the regulator IC's VC pin, closing the control loop.

VRS IS ADAPTABLE TO ISOLATED OUTPUT SUPPLIES AND ACCOMMODATES A 10Ω WIRE RESISTANCE.

You can also add VRS to a brick or half-brick isolated input module (**Figure 9**). You don't use the module's sense terminals. Instead, you introduce the sense IC's wiring-drop correction at the module's trim pin. The power-brick-module trim pin's transient response defines the available control bandwidth (**Figure 10a**). The trim pin's dynamics dictate your expectation for the loop response of this module (**Figure 10b**). The load-step response is less than 40 msec with this Vicor module. The module's trim-pin dynamics limit the clean and well-controlled response envelope. Turn-on dynamics into a 2.5A load are equally



NOTE: GUARD PINS NOT SHOWN.

Figure 6 The VRS IC can work with linear voltage regulators.

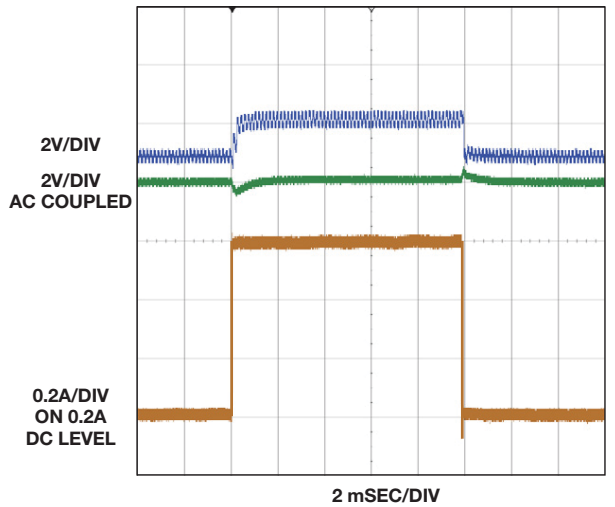


Figure 7 The voltage at the load (center trace) recovers from a load step (bottom trace) on the circuit of Figure 6. The sense-pin waveform shows the small ac excitation voltage (top trace).

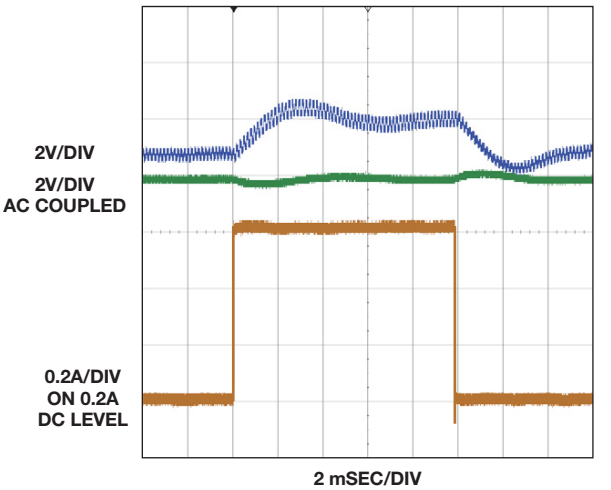
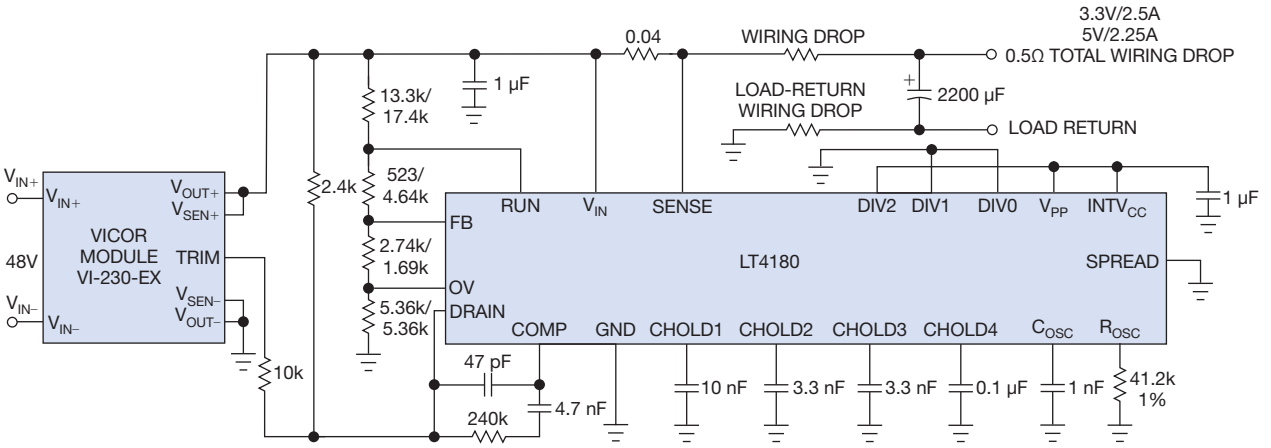


Figure 8 Increasing the load capacitance from 100 to 1000 mF improves transient response.



NOTE: GUARD PINS NOT SHOWN.

Figure 9 The sense IC can control the trim pin of a brick-type power module to correct for wiring losses.

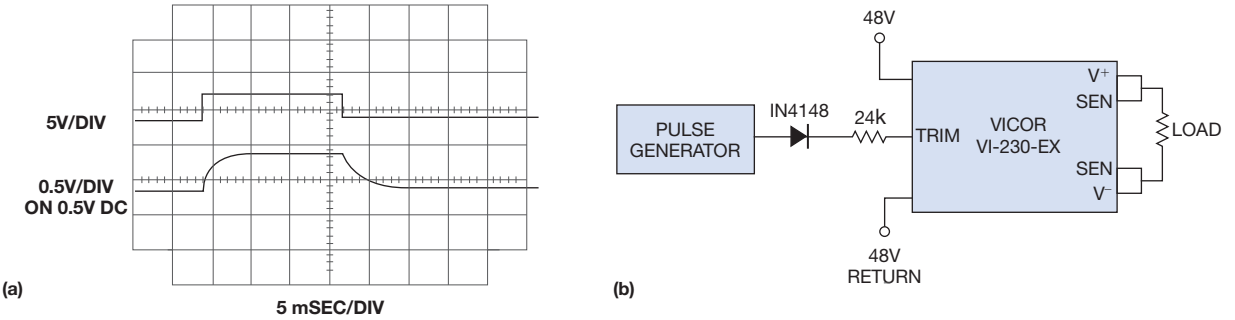


Figure 10 The power-brick-module trim pin's transient response defines the available control bandwidth (a). The trim pin's dynamics dictate your expectation for the loop response of this module (b).

well-behaved (**Figure 11**). The sense IC's operation arrests the initial abrupt rise at the third vertical division (**Figure 12**). The sense IC controls the output ascent's conclusion to the regulation point in a damped fashion. You can barely discern the sense IC's sampling square wave in the output waveform's settled portion.

You can also apply VRS to offline power supplies (see related **figure** in the Web version of this article at www.edn.com/101118df). A typical VRS-aided offline isolated output supply has a 5V output with 2A capacity. The schemat-

A PRIMER ON VRS OPERATION

Voltage drops in wiring can produce considerable load-regulation errors in electrical systems (Figure A). As load current, I_L, increases, voltage drop in the wiring increases, and the load voltage decreases. The traditional approach to solving this problem, remote sensing, regulates the voltage at the load, increasing the power-supply voltage, V_{OUT}, to compensate for voltage drops in the wiring. Although remote sensing works well, it requires an additional pair of wires to measure at the load, which can sometimes be impractical.

The LT4180 eliminates the need for a pair of remote-sense wires by creating VRS (virtual remote sensing). The IC achieves VRS by measuring the incremental change in voltage that occurs with an incremental change in current in the wiring (Figure B). You can use this measurement to infer the total dc voltage drop in the wiring, which you can then compensate for. The VRS IC takes over control of the power supply through its feedback pin, V_{FB}, maintaining tight regulation of load voltage V_L.

Figure C shows that a new cycle begins when the power supply and VRS close the loop around the supply voltage. Both the supply voltage and the supply current slew and settle to a new value, and the VRS stores these values. The device opens a new supply-voltage feedback loop and sets up a new feedback loop that commands the power supply to deliver 90% of the previously measured current (0.9A). The supply voltage drops to a new value as the power supply reaches a new steady state, and the VRS IC also stores this information. At this point, the device has measured and stored the change in the output voltage for a –10% change in output current. The next VRS cycle uses this voltage to compensate for voltage drops due to wiring resistance.

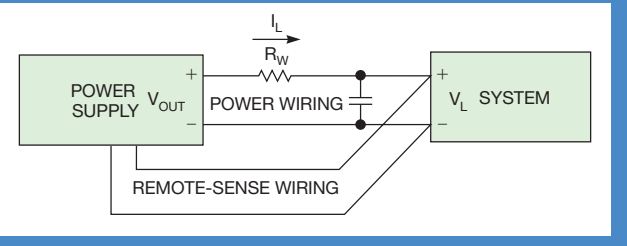


Figure A A four-wire system compensates for voltage drop but is complex.

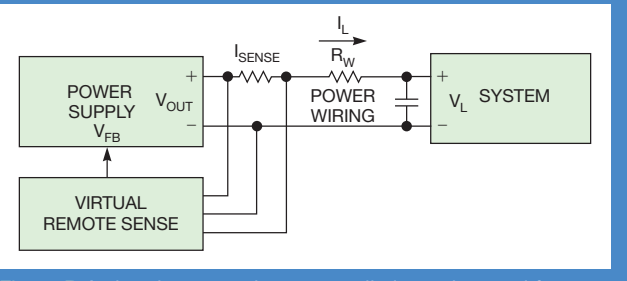


Figure B A virtual-sense scheme can eliminate the need for sensing wires.

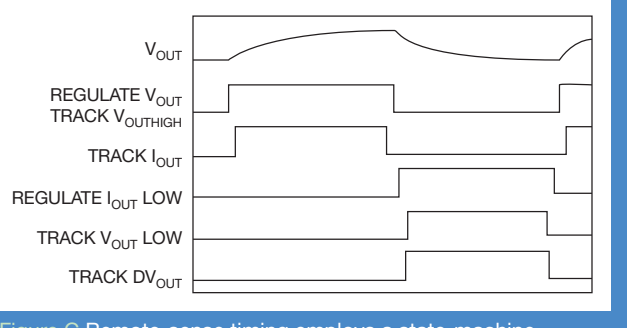


Figure C Remote-sense timing employs a state-machine sequence.

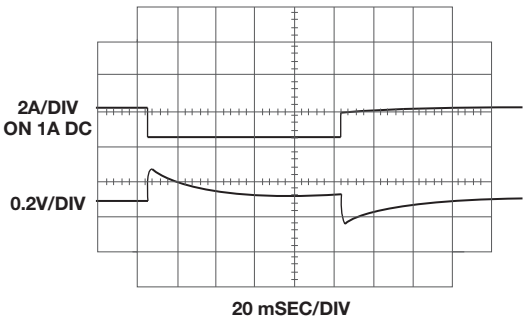


Figure 11 Applying a load step (top trace) to the circuit of Figure 9 yields a well-behaved voltage output (bottom trace).

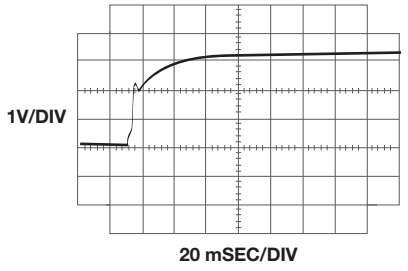


Figure 12 The sense IC also provides a slower turn-on as it begins working at the third vertical division.

ic appears complex, but inspection reveals it to be an ac-line-powered variant of an isolated approach. The sense IC provides remote sensing and closes an isolated feedback loop with optical transmission.

LAMP CIRCUIT

You can also use a VRS IC to stabilize the drive to a halogen lamp (see related **figure** in the Web version of this article at www.edn.com/101118df). The circuit is a buck-boost SEPIC (single-ended primary-inductance converter, **Reference 2**). This 12V, 30W automotive-lamp output remains constant despite a 9 to 15V input-voltage variation along with any line resistance or connection uncertainties (see related **figure** in the Web version of this article at www.edn.com/101118df). Additional benefits include a constant color output and an extended lamp life due to greatly reduced lamp turn-on current (see related **figure** in the Web version of this article at www.edn.com/101118df). The regulator reduces inrush current to 7A, one-third of the unregulated value. EDN

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1 "LT4180 Virtual Remote Sense Controller," Linear Technology Corp, 2010 http://bit.ly/dtBpsO.
2 Ridley, Ray, PhD, "Analyzing the Sepic Converter," *Power Systems Design Europe*, November 2006, http://bit.ly/csfFGz.

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An introduction to ACOUSTIC THERMOMETRY

USE AN ULTRASONIC TRANSDUCER TO MEASURE AIR TEMPERATURE IN AN OLIVE JAR.

BY JIM WILLIAMS AND OMAR SANCHEZ-FELIPE • LINEAR TECHNOLOGY

Acoustic thermometry is an arcane, elegant technique that measures temperature using the temperature-dependent transit time of sound in a medium (**references 1** through **4**). The medium can be a solid, a liquid, or a gas. Acoustic thermometers function in environments, including extreme temperatures, destructive physical abuse, and nuclear reactors, that conventional sensors cannot tolerate. Sonic speed in air varies predictably as the square root of temperature. The sonic transit time in a gas-path thermometer is almost entirely insensitive to pressure and humidity. Gas-path acoustic thermometers respond quickly to temperature changes. They have essentially no thermal mass or lag.

AT A GLANCE

- Acoustic thermometers function in environments that conventional sensors cannot tolerate.
- You can measure air temperature by the speed of sound.
- Barometric pressure is not a primary variable.
- The signal path requires careful design.
- Gating can be used to reduce noise and ignore spurious signals.
- A microprocessor calibrates the design to 0.1°F resolution.

IMAGE: THINKSTOCK

You take a measurement across the entire body of an acoustic thermometer. The measurement represents the total path-transit time. Conventional sensors, in contrast, measure at a single point. An acoustic thermometer is thus blind to temperature variations within the measurement path. It infers temperature from the isothermal or the nonisothermal measurement path's delay.

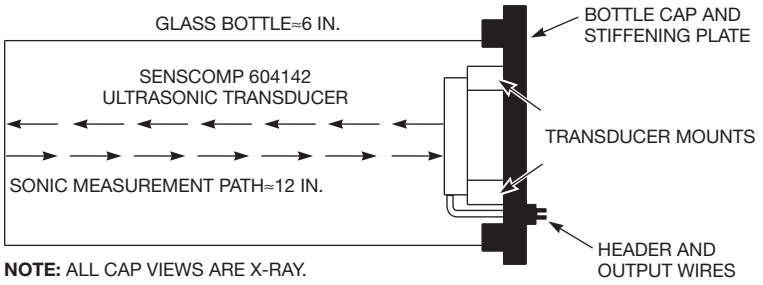

Figure 1 The ultrasonic transducer rigidly mounts within the stiffened cap you affix to a glass bottle.

PRACTICAL CONSIDERATIONS

A practical acoustic-thermometer demonstration begins with selecting a sonic transducer and a dimensionally stable measurement path. A wideband ultrasonic transducer promotes fast, low-jitter, high-fidelity response free of resonance and other parasitic losses. An electrostatic ultrasonic sensor (**Figure 1**) meets these requirements (**Reference 5**). An ultrasonic transducer serves as both transmitter and receiver. The device is rigidly mounted on the metal cap of a glass enclosure. You should stiffen the cap to ensure dimensional stability of the measurement path. This design uses the bottle and cap from Reese (http://reese.elsstore.com) Cannonball olives (**Figure 2**). Barometric pressure is not a major variable in transit time because it does not bow the stiffened cap, averting errors.

You should remove the olives and their residue, and bake out the bottle and cap at 100°C. Pass the transducer leads through the cap using a coaxial header. The glass enclosure has a relatively small thermal-expansion coefficient. This arrangement makes the path distance stable with temperature, pressure, and mechanical changes. The round-trip path length is approximately 12 in. The speed of sound in air is 1.1 feet/msec. Thus, the round-trip time is 900 µsec. The path's temperature-dependent variation is approximately 1 µsec/°F at 75°F. To achieve a 0.1°F resolution requires mechanical and electronic variations of less than 100 nsec, which in turn requires a 0.001-in. dimensional stability referred to the 12-in. path length. When you examine the likely error sources, you will see this stability as a realistic goal.

You bias the transducer, which acts

Figure 2 A plate of copper-clad PCB material stiffens the metal cap of the olive jar. The transducer mounts inside the jar, and an SMA header allows a coaxial cable to connect to the assembly.

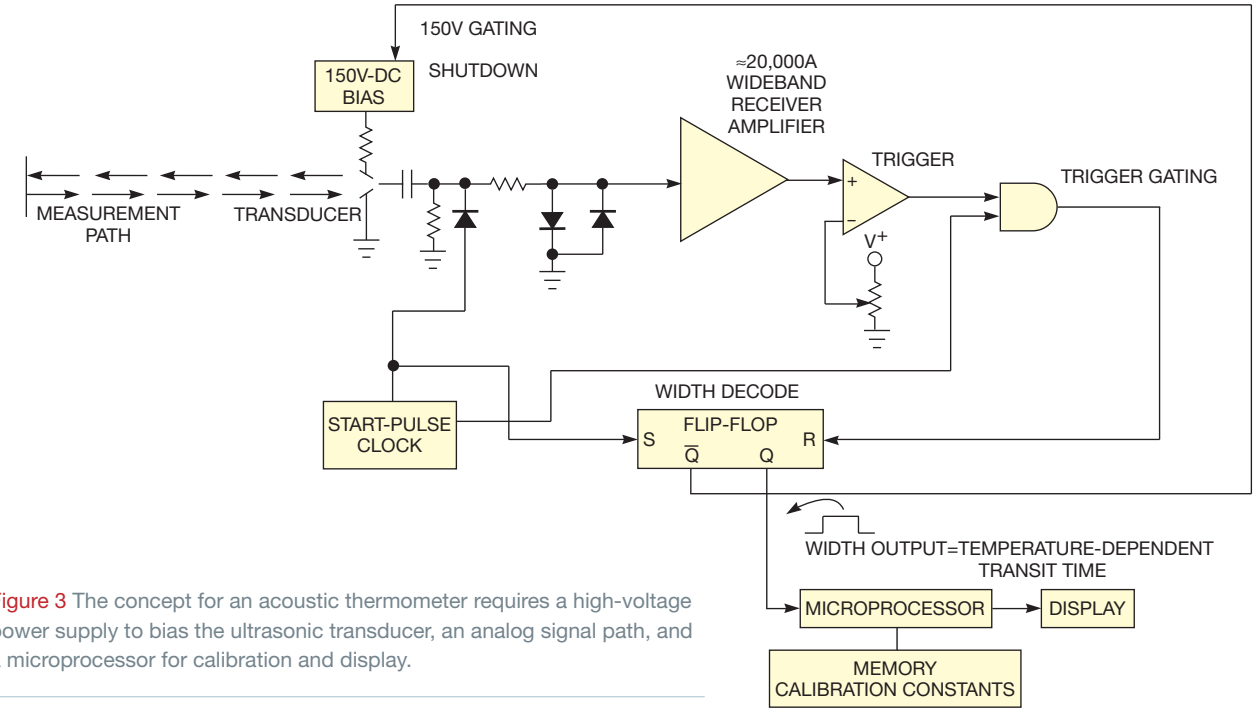

Figure 3 The concept for an acoustic thermometer requires a high-voltage power supply to bias the ultrasonic transducer, an analog signal path, and a microprocessor for calibration and display.

as a capacitor, at 150V dc (**Figure 3**). The start-pulse clock drives the transducer with a short impulse, launching an ultrasonic event into the measurement path. The start-pulse clock simultaneously sets the width-decoding flip-flop high. The sonic impulse bounces off the enclosure's bottom, travels back, and impinges on the transducer, resulting in a minuscule mechanical displacement, which in turn changes the capacitance of the transducer. Based on the **equation** relating charge, Q, to capacitance and voltage, Q=C×V, the capacitance change creates a voltage change at the receiver amplifier's input.

The trigger comparator converts the amplifier's output excursion into a logic-compatible level, resetting the width-decoding flip-flop. The flip-flop's output width represents the measurement path's temperature-dependent

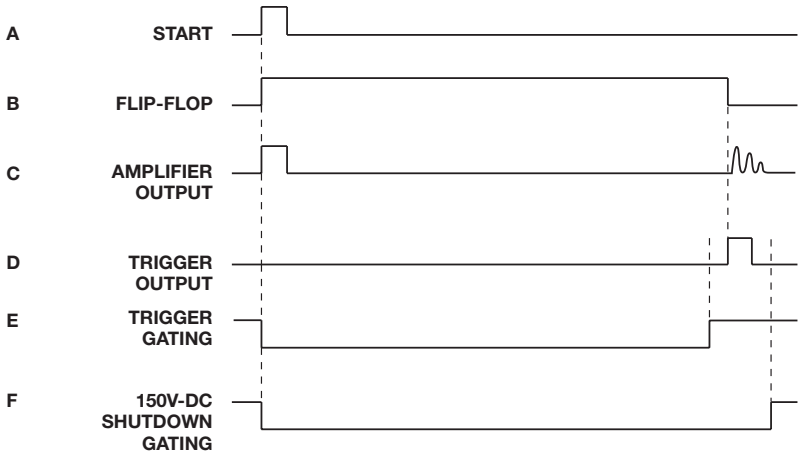

Figure 4 The acoustic thermometer uses a start pulse to drive the transducer (Trace A), setting the flip-flop high (Trace B). The sonic pulse returns (Trace C), activating the trigger output (Trace D) and resetting the flip-flop. You gate the trigger circuit to prevent an erroneous trigger response (Trace E). Another gate turns off the 150V switching converter during the measurement to prevent amplifier corruption (Trace F).

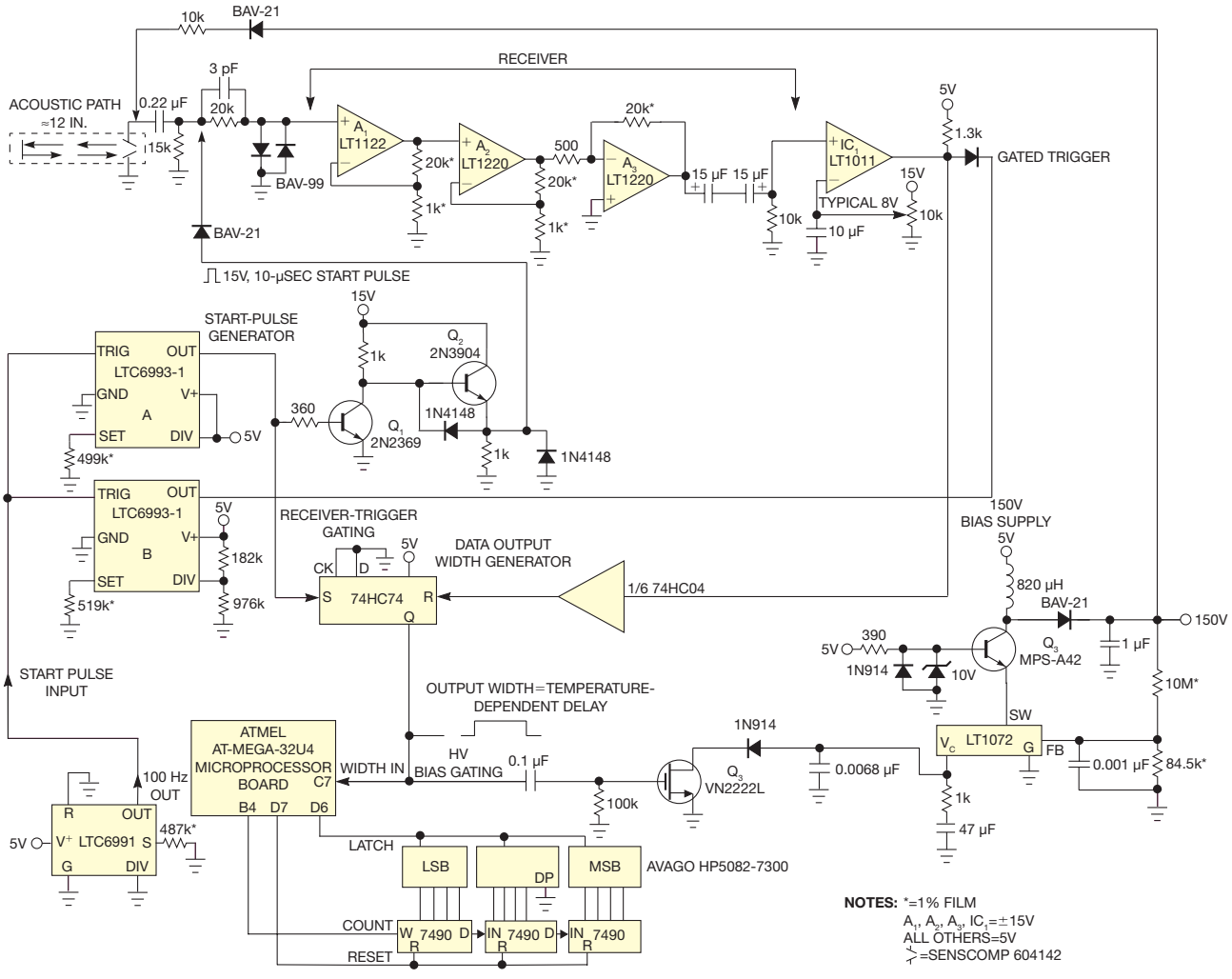

Figure 5 The detailed circuitry closely follows the concepts of those in Figure 3.

sonic transit time. You program the microprocessor with the measurement path's temperature and delay calibration constants (see **sidebar** "Measurement-path calibration"). The microprocessor can then calculate the temperature using the pulse width and supply this information to the display.

You derive a second output from the start-pulse generator, which gates off the trigger's output during most of the measurement cycle, enabling the trigger output only during the time when you expect a return pulse. This method eliminates false triggers by discriminating against unwanted sonic events that originate outside the measurement path. The transducer's return pulse amplitude is less than 2 mV. The high-gain, wideband receiver amplifier is vulnerable to parasitic inputs, so you must shut down the 150V bias supply during the measurement to prevent its switching harmonics from corrupting the amplifier. You derive a second gate from the width-decoding flip-flop. It shuts down the 150V bias supply during the measuring interval.

A measurement cycle begins with a start pulse driving the transducer (Trace A in **Figure 4**), setting the flip-flop (Trace B) high. After the sonic impulse's transit time, the amplifier responds (Trace C), tripping the trigger, which resets the flip-flop (Trace D). The gate signals protect the trigger from unwanted sonic events, start-pulse artifacts, and shut off the high-voltage regulator during measurement (traces E and F).

DETAILED CIRCUITRY

A silicon oscillator furnishes the 100-Hz clock (**Figure 5**). Monostable pulse generator IC_A provides a 10-µsec pulse to a driver you make with Q_1 and Q_2. You capacitively couple the driver output's start pulse into the ultrasonic transducer (Trace A in **Figure 6**). The monostable

MEASUREMENT-PATH CALIBRATION

Theoretically, you can calculate temperature-calibration constants from the measurement-path length. In practice, it is difficult to determine the path length to the required accuracy because of glass-jar, transducer, and mounting dimensional uncertainties. Instead, you must calibrate the device over known temperatures (Figure A). Place the enclosure in a controllable thermal chamber with an accurate thermometer and ensure that the thermometer is isothermal with the enclosure. Next, vary the chamber temperature over 10 evenly spaced points at 60 to 90°F. The enclosure has a 30-minute time constant to settle within 0.25°F. You must allow adequate time for each step to stabilize before taking readings. Note the pulse width at each temperature and record the data. You then load this information into the microprocessor memory.

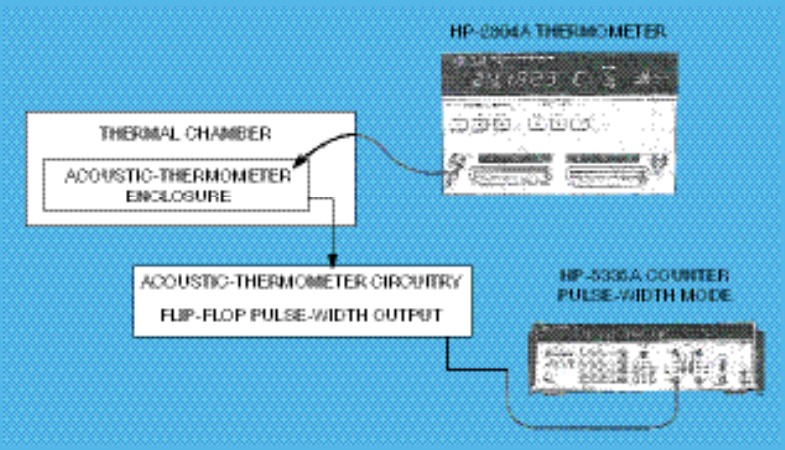

Figure A The calibration arrangement comprises a thermometer, a counter, acoustic-conditioning circuitry, and the glass-jar enclosure inside a thermal chamber.

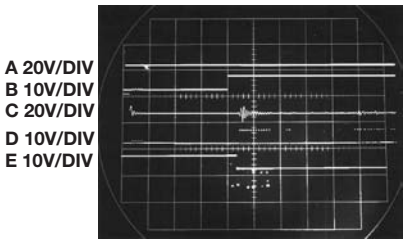

Figure 6 The schematic waveforms include the start pulse (Trace A), the trigger gate (Trace B), amplifier A_2's output (Trace C), the trigger output (Trace D), and the flip-flop's output (Trace E). The second acoustic bounce causes a second set of trigger outputs, which are inconsequential to the circuit's operation (Trace D).

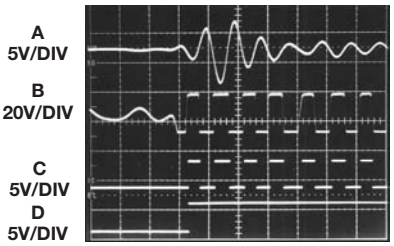

Figure 7 You monitor the amplifier's response at the output of A_2 (Trace A). Amplifier A_3 adds gain, which softly saturates the signal's leading-edge response (Trace B). Comparator IC_1's trigger output creates multiple triggers (Trace C). However, the flip-flop output remains high after the initial trigger, providing an accurate transit time (Trace D).

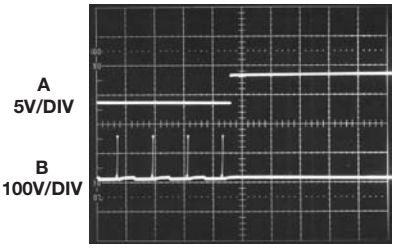

Figure 8 The high-voltage bias-supply-gate signal (Trace A) disables the 150V converter-flyback events (Trace B).

pulse generator simultaneously sets the flip-flop high (Trace E). The high output from the flip-flop shuts down the high-voltage switching regulator during the measurement. You set up the monostable pulse generator, IC_B, to produce a second pulse. This pulse gates off comparator IC_1's output for a time just shorter than the expected sonic return pulse (Trace B).

The sonic pulse travels down the measurement path, bounces, and returns to impinge on the transducer. The switching regulator biases the transducer at 150V dc. It operates as a cascode of the internal switching transistor in the IC and high-voltage transistor Q_3. This high voltage allows the small capacitance change that the diaphragm's motion creates to generate an appreciable voltage change. You send this voltage change to the receiver amplifier. Capacitive coupling isolates the high-voltage dc-transducer bias, and diode clamps prevent destructive overloads. The cascaded receiver amplifier has an overall gain of 17,600. You can monitor the amplifier at the low-impedance output of A_2 (Trace C). A_3, the last stage in the cascade, further amplifies the signal. You send the amplifier output to comparator IC_1, which creates an output trigger (Trace D) that occurs at the first event that exceeds its negative-input threshold. The trigger resets the width-decoding flip-flop. The flip-flop pulse width then represents the temperature-dependent acoustic transit time. You send this pulse to the microprocessor, which determines and displays the temperature (**Reference 6**). See **sidebar** "Software code" in the Web version of this article at www.edn.com/110421df for the complete processor-software code.

You can expand your oscilloscope's signals at the return impulse trip point (**Figure 7**). You monitor the amplifier's response at the output of A_2 (Trace A). Amplifier A_3 adds gain, which softly saturates the signal's leading-edge response (Trace B). Comparator IC_1's trigger output creates multiple triggers (Trace C). However, the flip-flop output remains high after the initial trigger, providing an accurate transit time (Trace D).

Gate the high-voltage supply to prevent switching harmonics from producing spurious amplifier outputs. The start pulse sets the flip-flop output high (Trace A in **Figure 8**), shutting down high-voltage switching at the onset of the measurement period (Trace B). This state persists during the entire transit time and prevents erroneous amplifier-trigger outputs. A return-pulse trigger resets the flip-flop (Trace A in **Figure 9**). You send the flip-flop output to a circuit that gates off the switching regulator by modulating its compensation pin, V_C, delaying the high-voltage turn-on until after the measurement period (Trace B) and ensuring a clean, noise-free trigger signal.

Gating the trigger output prevents interference from outside sources. Gating the 150V converter prevents its harmonics from corrupting the receiver's amplifier. The 150V supply value is a gain term. The higher it is, the more signal it returns. Gating off its regulation during the measurement is a potential concern. Practically, the 1-µF output capacitor decays only 30 mV, or approximately 0.02%, during this time. This small variation is constant and insignificant, and you can ignore it. You derive the trigger trip point and the start pulse from the same 15V supply, enhancing stability because it makes the trigger voltage vary ratiometrically with the received signal's amplitude. The wideband, highly sensitive, and resonance-free transducer descends from 1970s-era Polaroid (www.polaroid.com) SX-70 automatic-focus cameras, promoting repeatable, jitter-free operation. All of these attributes

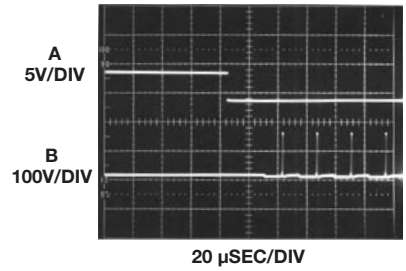

Figure 9 When the high-voltage bias-supply gate falls (Trace A), the supply resumes operation.

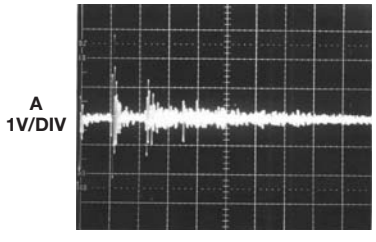

Figure 10 The circuit can detect multiple bounces of the original sonic pulse. By the fourth bounce, sonic dispersions in the jar cause almost total loss of the signal.

directly contribute to the 100-nsec, 0.1°F resolution of the circuit for a 1-msec travel time, representing less than 100-ppm uncertainty. Once you calibrate the circuit, the absolute accuracy at 60 to 90°F is within 1°F.

Further investigations might have you attempt to trigger the receiver after multiple bounces (**Figure 10**). This approach offers the benefit of easing timing tolerances. The return signals decay into noise that acoustic dispersion in the glass enclosure creates. Triggering on a later bounce would relax your timing margins but also gives you an unacceptable SNR (signal-to-noise ratio). Signal-processing techniques could overcome this problem, but the effort would have to justify the increased resolution. EDN

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